Effect of Statistical Clock Skew Variations on Chip Timing Yield

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ABSTRACT

Integrated circuit design with sub-100nm technology requires closer attention to the effect of process variations on circuit timing. In a previous work, we had developed a method of statistical timing analysis in which the effect of process variations on circuit timing is assessed, given a generic logic path in a target design technology. In this work, we extend that previous work in an important way, by incorporating into the analysis the effect of clock skew. The resulting model captures both die-to-die and within-die process variations, in both logic and clock paths, it handles within-die correlation using principal component analysis, and it leads to an expression for the resulting timing yield. Among other uses, this allows one to compute how much reduction one will see in the timing yield, for a given clock skew variance.

1. INTRODUCTION

With the scaling of integrated circuit (IC) technology, the control over process variations is becoming more difficult. The variations of circuit parameters (channel length, threshold voltage, wire length and width, doping, etc.) between different dies (chips), and within the same die, have a significant effect on circuit timing. In order to account for this variability, there is a need to model both gate and interconnect delays as statistical quantities and to study the impact on the timing yield using "statistical timing analysis" [1, 2].

The literature abounds with recent proposals for statistical timing analysis. As reviewed in our previous work [3], many of these proposed techniques suffer from a key problem that they assume the presence of various types of statistical process data (such as correlations and how they vary with placement) which is not available today. A key contribution of [3] was to propose a method for studying the impact of variations on the timing yield using minimal process data. Due to lack of space, the reader is referred to [3] for details; suffice it to say that the method operates by assuming that a *generic logic path* in a given technology is available, and provides an analytical technique for computing the chip timing yield given the variances of various circuit parameters. However, absent from [3] was the effect of variations in clock delay on the timing yield. This paper extends that previous work in an important direction: we show how one can take statistical variations in clock skew into account as we compute the chip timing yield. Previous work on statistical clock skew aimed to find its distribution [2]. However, to our knowledge, this is the first work that studies the effect of statistical clock skew on the chip timing yield.

In section 2, we present a parameter model that handles die-to-die and within-die variations, as well as spatial correlations using Principal Component Analysis (PCA) [3]. Section 3 shows how clock skew can fit in the parameter model, with slight modifications. The effect of statistical clock skew is also added to the Setup or Max timing constraint. The correlation between logic path delay and clock skew is taken care of by the PCA coefficients. As a result, a timing yield expression is computed, which takes into account the effects of logic path delay and clock skew on statistical timing analysis. In section 4, we conduct different simulations to check the effects of adding clock skew on the timing yield curve. We also perform a sweep over the clock skew variance and plot the different results. These plots show that as the skew variance increases, timing yield is reduced.

2. PARAMETER MODEL

We will briefly review the parameter model adopted in [3]. For a given circuit element or layout feature i, let its coordinates on the die (i.e., on the chip surface) be (x_i, y_i) and let $X(i)$, be a zero-mean Gaussian *random variable* (RV) that denotes the variation of a certain parameter of this element from its nominal (mean) value. Thus, for example, $X(i)$ may represent channel length variations of transistor i. It was shown in [3] that path delay can be considered as a parameter of this model. Correlation between values of $X(i)$ at different locations on the die may be expressed by means of an autocorrelation function, but this is not a practical approach. Instead, it is standard practice [4] to express the correlation by first breaking up the variations into *die-to-die* and *within-die* components, as follows:

$$X(i) = X_{dd} + X_{wd}(i) \tag{1}$$

The die-to-die component X_{dd} is an *independent* zero-mean Gaussian RV that takes the same value for all instances of this element on a given die, irrespective of location. The within-die component $X_{wd}(i)$ is a zero-mean Gaussian which can take different values for different instances of that element on the same die. This leads to the following relationship between the variances:

$$\sigma^2(i) = \sigma^2_{dd} + \sigma^2_{wd}(i) \tag{2}$$

Then, the within-die component is further broken down into two components, a *systematic* component and a "random" component:

$$X_{wd}(i) = X_{wds}(x_i, y_i) + X_{wdr}(i) \tag{3}$$

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where, for each i, the random component $X_{wdr}(i)$ is an *independent* zero-mean Gaussian. The systematic component $X_{wds}(x_i, y_i)$ contains an explicit dependence on location because it is usually taken to represent the extent of correlation across the die, and correlation is usually dependent on relative location. For simplicity, we will replace $X_{wds}(x_i, y_i)$ by $X_{wds}(i)$ keeping in mind that it is dependent on the location of feature i. A similar relationship follows for the variances:

$$\sigma^2_{wd}(i) = \sigma^2_{wds}(i) + \sigma^2_{wdr}(i) \tag{4}$$

One way to express the systematic component of the within-die variations is to use a *principal components analysis* [5] (PCA) and write:

$$X_{wds}(i) = \sum_{j=1}^{p} a_{ij} Z_j \tag{5}$$

where Z_j are independent *standard normal* RVs (Gaussians with zero mean and unity variance) and where the coefficients a_{ij} are such that:

$$\sigma^2_{wds}(i) = \sum_{j=1}^{p} a^2_{ij} \tag{6}$$

The RVs Z_j correspond to underlying independent unobservable factors. The value of p and the coefficients a_{ij} represent the extent of correlation across the die. For example, if $p = 1$, then the within-die spatial correlation coefficient is 1, there is perfect correlation; a single underlying RV Z_1 determines the value of the systematic component of X_{wd} all over the die. A $p > 1$ allows for less than perfect correlation.

We will adopt the PCA expansion (5) as our "correlation model" for the within-die component, as was done in [3], where the reader can find some discussion of the merits of this model and of how one may determine the value of p in practice. Using this parameter model to handle variations, a parametric yield lower bound is produced in [3]. It is then shown that path delay $D_N(i)$ can be considered a parameter with its own die-to-die and within-die (systematic and random) components. Therefore, a timing yield lower bound is produced using the parametric yield analysis. However, as defined in [3], the timing yield only took into account path delay variations. In other words, it was defined as the probability that all path delays are less than a margin τ.

In this paper, we extend that previous work by studying the effect of statistical clock skew on the timing yield. Our analysis is mainly suited for synchronous and clocked circuits. The next sections will discuss in detail the contribution of process variations induced clock skew to timing yield.

3. CLOCK SKEW EFFECT

3.1 Clock Skew Model

A Generic Logic Critical Path (GLCP) is defined as a logic path consisting of N gates. Any GLCP i between two flip-flops (FF-1 and FF-2) is subject to clock skew $S(i)$ between these flip-flops (Fig. 1). Assuming that $t_1(i)$ and $t_2(i)$ are the clock arrival times at FF-1 and FF-2 respectively, clock skew $S(i)$ would be defined as follows:

$$S(i) = t_2(i) - t_1(i) \tag{7}$$

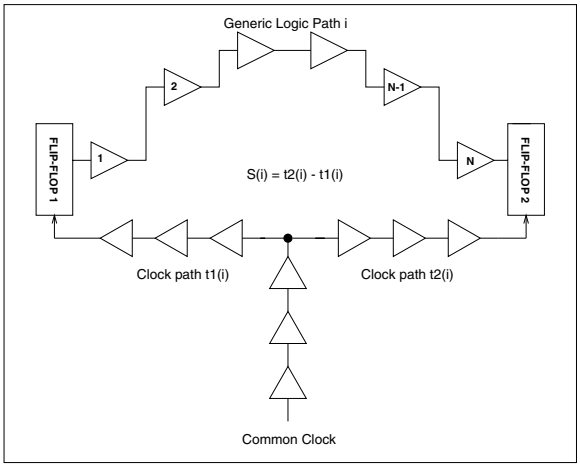

Figure 1: Generic Logic Critical Path GLCP subject to Clock Skew

Using the parameter model defined earlier, $t_1(i)$ and $t_2(i)$ are statistical timing quantities that we can decompose into three components: die-to-die, within-die systematic, and within-die random. As a result, clock skew $S(i)$ will have the same model, with a slight difference: since the die-to-die component is the same across the whole die, then it would drop out from $S(i)$ after the subtraction (7). The final clock skew model is the following:

$$S(i) = S_{wds}(i) + S_{wdr}(i) \tag{8}$$

where $S_{wds}(i)$ is the systematic within-die component, and $S_{wdr}(i)$ is the random within-die component. Assuming that designers aim for zero nominal clock skew, both components have zero mean. The random component $S_{wdr}(i)$ is an independent, zero mean, normally distributed random variable with variance $\gamma^2_{wdr}(i)$. Whereas the systematic component $S_{wds}(i)$ is modeled using PCA in the same way defined in section 2:

$$S_{wds}(i) = \sum_{j=1}^{p} s_{ij} Z_j \tag{9}$$

where Z_j are the same independent standard normal RVs defined earlier. In this way, correlations between logic path delay and clock skew are only attributed to systematic spatial correlations modeled using PCA. The coefficients s_{ij} are such that:

$$\gamma^2_{wds}(i) = \sum_{j=1}^{p} s^2_{ij} \tag{10}$$

where $\gamma^2_{wds}(i)$ is the systematic clock skew variance. The total variance of clock skew is the following:

$$\gamma^2(i) = \gamma^2_{wds}(i) + \gamma^2_{wdr}(i) \tag{11}$$

Having defined the model for clock skew, we will investigate its effects on timing yield.

3.2 Timing constraint with clock skew effect

In general, for a circuit to satisfy Setup time or Max timing constraint (neglecting clock skew), the delay of all the paths should satisfy the following:

$$D_N(i) \leq \tau\,,\ \forall\, i \tag{12}$$

where $D_N(i)$ is the delay RV for GLCP i, and τ is a deterministic quantity that bounds the delay. In [3], $D_N(i)$ was modeled in the following way, using the parameter model:

$$D_N(i) = D_{N_{dd}} + D_{N_{wds}}(i) + D_{N_{wdr}}(i) \tag{13}$$

The right hand side is the die-to-die, within-die systematic, and within-die random components respectively, with variances σ_{dd}, $\sigma_{wds}(i)$, and $\sigma_{wdr}(i)$.

However, adding clock skew model from (8) to the above equation would result in the following timing constraint:

$$D_N(i) \leq \tau + S(i)\,,\ \forall\, i \tag{14}$$

This is the main problem that we are trying to solve: Studying the effect of statistical clock skew on the timing constraint, and hence on the timing yield computed in [3].

3.3 Yield analysis

We will apply the timing yield analysis used in [3] with slight modifications to find the general expression for timing yield considering both logic path delay and clock skew. An expression for timing yield was derived in [3]:

$$Y(\tau) = P\,\{\, D_N(i) \leq \tau\,,\ \forall\, i\,\} \tag{15}$$

Let us define $Y_t(\tau)$ to be the total yield with added clock skew. Then we can write:

$$\begin{aligned} Y_t(\tau) &= P\,\{\, D_N(i) \leq \tau + S(i)\,,\ \forall\, i\,\} \\ &= P\,\{\, D_N(i) - S(i) \leq \tau\,,\ \forall\, i\,\} \end{aligned} \tag{16}$$

Replacing $D_N(i)$ and $S(i)$ by their expressions leads to the following:

$$Y_t(\tau) = P\,\{\, D_{N_{dd}} + A(i) + B(i) \leq \tau\,,\ \forall\, i\,\} \tag{17}$$

where:

$$\begin{aligned} A(i) &= D_{N_{wds}}(i) - S_{wds}(i) && (18)\\ &= \sum_{j=1}^{p} (a_{ij} - s_{ij})\, Z_j && (19)\\ B(i) &= D_{N_{wdr}}(i) - S_{wdr}(i) && (20)\\ &= \sqrt{\sigma^2_{wdr}(i) + \gamma^2_{wdr}(i)}\ Z_r(i) && (21) \end{aligned}$$

where (21) is the result of subtracting two independent RVs, $D_{N_{wdr}}(i)$ and $S_{wdr}(i)$, with variances $\sigma^2_{wdr}(i)$ and $\gamma^2_{wdr}(i)$ respectively, and $Z_r(i)$ are independent standard normal RVs.

Expression (17) of the yield is very similar to the one found in [3] with slight modifications; the die-to-die part is the same, since skew has no die-to-die component. The systematic within-die part is:

$$\sum_{j=1}^{p} (a_{ij} - s_{ij})\, Z_j \ \text{ instead of } \ \sum_{j=1}^{p} a_{ij}\, Z_j \tag{22}$$

the random within-die is:

$$\sqrt{\sigma^2_{wdr}(i) + \gamma^2_{wdr}(i)}\, Z_r(i) \ \text{ instead of } \ \sigma_{wdr}(i) Z_r(i) \tag{23}$$

To simplify notations, let

$$\sigma_r(i) = \sqrt{\sigma^2_{wdr}(i) + \gamma^2_{wdr}(i)} \tag{24}$$

be the total random standard deviation of the combined $\{D_{N_{wdr}}(i)$ - $S_{wdr}(i)\}$ quantity. As to the combined systematic within-die quantity $\{D_{N_{wds}}(i) - S_{wds}(i)\}$, it needs more work. The key point in [3] is the step that allowed to move from an expression dependent on all a_{ij} coefficients to one dependent only on the sum of a^2_{ij}, which is the variance. We will do the same here, by applying Cauchy's inequality twice. But first, recall from probability theory that if two RVs are such that $Z_1 \leq Z_2$, then $P\{Z_1 \leq a\} \geq P\{Z_2 \leq a\}$. Now taking the systematic part (19) and applying Cauchy's inequality, we can write:

$$\begin{aligned} \sum_{j=1}^{p} (a_{ij} - s_{ij})\, Z_j &\leq \left| \sum_{j=1}^{p} (a_{ij} - s_{ij})\, Z_j \right| && (25)\\ &\leq \sqrt{\sum_{j=1}^{p} (a_{ij} - s_{ij})^2}\ \sqrt{\sum_{j=1}^{p} Z_j^2} && (26)\\ &= \sqrt{\sum_{j=1}^{p} a_{ij}^2 + \sum_{j=1}^{p} s_{ij}^2 - 2 \sum_{j=1}^{p} a_{ij}\, s_{ij}}\ \sqrt{\sum_{j=1}^{p} Z_j^2} && (27) \end{aligned}$$

The transition from (25) to (26) is a direct application of Cauchy's Inequality. Equation (27) results from expanding the terms of (26).

Applying Cauchy's inequality a second time in the last part of the above equation result in:

$$\begin{aligned} -2 \sum_{j=1}^{p} a_{ij}\, s_{ij} \leq 2 \left| \sum_{j=1}^{p} a_{ij}\, s_{ij} \right| &\leq 2 \sqrt{\sum_{j=1}^{p} a_{ij}^2}\ \sqrt{\sum_{j=1}^{p} s_{ij}^2} \\ &= 2\, \sigma_{wds}(i)\, \gamma_{wds}(i) \end{aligned} \tag{28}$$

Combining (25) to (28) leads to:

$$\begin{aligned} &\sum_{j=1}^{p} (a_{ij} - s_{ij})\, Z_j \leq && (29)\\ &\qquad \sqrt{\sigma^2_{wds}(i) + \gamma^2_{wds}(i) + 2\, \sigma_{wds}(i)\, \gamma_{wds}(i)}\ \sqrt{\sum_{j=1}^{p} Z_j^2} && (30)\\ &\qquad = \sqrt{(\sigma_{wds}(i) + \gamma_{wds}(j))^2}\ \sqrt{\sum_{j=1}^{p} Z_j^2} && (31)\\ &\qquad = (\sigma_{wds}(i) + \sigma_{swds}(i))\ \sqrt{\sum_{j=1}^{p} Z_j^2} && (32) \end{aligned}$$

Substituting (29) and (24) in (17), and using the observation from probability theory, leads to the following lower bound on the total yield:

$$\begin{aligned} Y_t(\tau) \geq\ & \\ & P\Big\{ D_{N_{dd}} + (\sigma_{wds}(i) + \gamma_{wds}(i)) \sqrt{\sum_{j=1}^{p} Z_j^2} + \\ & \qquad \sigma_r(i) Z_r(i) \leq \tau,\ \forall\, i \Big\} \end{aligned} \tag{33}$$

The above expression is the yield lower bound for $p > 1$. However, if $p = 1$, then there's no need for Cauchy's inequality, and the yield expression would be equal to the

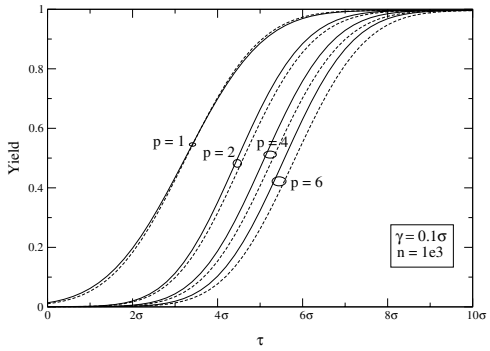

Figure 2: Timing Yield, $\gamma = 0.1\sigma$

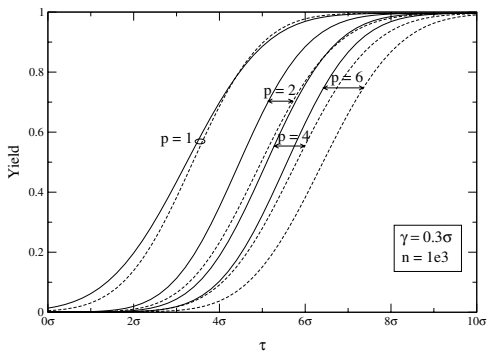

Figure 3: Timing Yield, $\gamma = 0.3\sigma$

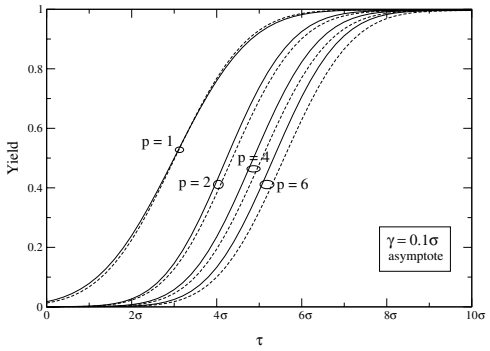

Figure 4: Yield asymptote, $\gamma = 0.1\sigma$

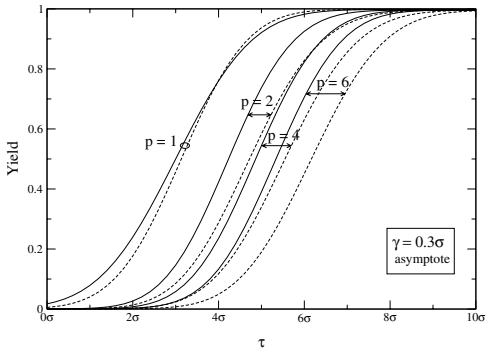

Figure 5: Yield asymptote, $\gamma = 0.3\sigma$

following:

$$Y_t(\tau) = P\left\{D_{N_{dd}} + (\sigma_{wds}(i) - \gamma_{wds}(i))\, Z_1 + \sigma_r(i) Z_r(i) \leq \tau,\ \forall\, i\right\} \quad (34)$$

These yield expressions are very similar to those found in [3], only differing in the values of systematic and random standard deviations. Instead of $\sigma_{wds}(i)$, we have $(\sigma_{wds}(i) + \gamma_{wds}(i))$ for $p > 1$ and $(\sigma_{wds}(i) - \gamma_{wds}(i))$ for $p = 1$. And instead of $\sigma_{wdr}(i)$, we have $\sigma_r(i) = \sqrt{\sigma^2_{wdr}(i) + \gamma^2_{wdr}(i)}$. Therefore, we can compute the total yield using the same algorithms derived in [3] after replacing the systematic and the random standard deviations by their new values above.

4. RESULTS

As an illustration, we will consider that all logic path delay standard deviations (die-to-die, systematic within-die, and random within-die) are equal to a constant σ, (i.e $\sigma_{dd} = \sigma_{wds}(i) = \sigma_{wdr}(i) = \sigma$, $\forall\, i$), and all clock skew standard deviations are equal to a constant γ, that is $\gamma_{wds}(i) = \gamma_{wdr}(i) = \gamma$, $\forall i$. We will plot the yield curves under statistical clock skew using the different analyses presented in [3]. We will also sweep the value of γ to investigate how skew variance affect the yield.

Assuming that $\gamma = 0.1\sigma$, Fig. 2 compares yield curves with and without clock skew, for $p = 1, 2, 4, 6$. Solid lines represent yield curves as computed in [3], for n = 1e3, and dotted lines represent yield curves with clock skew. As it was expected, adding clock skew has degraded the yield for $p > 1$. Moreover, as p increases, the effect of clock skew on the yield curve also increases. This is also due to the Cauchy lower bound. For $p = 1$, the yield curve plotted is not a lower bound but rather the exact timing yield, since we did not use Cauchy's Inequality for $p = 1$. Clock skew also degrades performance for $p = 1$. This shows better when its variance γ increases to 0.3σ as seen in Fig. 3. However it is worth noting that for small γ, clock skew degrades in parts and enhances in other parts. This is explained if we look at (14). When clock skew $S(i)$ is negative, it is less likely for the path delay to meet the constraint! Yield will decrease. However, when $S(i)$ is positive, we have more margin, and yield will increase. However as the skew variance increases, the skew will generally degrade the yield. In Figs. 2 and 3, the plots are computed using the *n dependent* equations from [3], where a value for n is needed to compute the yield.

Figs. 4 and 5 show same effects of clock skew on the yield curves as before, using however the lower bound analysis (asymptote). These plots result from equations derived in [3] as n goes to infinity, and do not require the value of n.

5. REFERENCES

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