

RÉSUMÉ

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EDUCATION :

1986-1989: University of Illinois at Urbana-Champaign Urbana, Illinois, USA

Ph.D. degree, Electrical Engineering. Thesis topic: "Probabilistic Simulation for Reliability Analysis of VLSI Circuits," supervised by Prof. Ibrahim N. Hajj and Dr. Ping Yang, of Texas Instruments Inc. Research conducted in-part at Texas Instruments in Dallas, Texas.

1985-1986: University of Illinois at Urbana-Champaign Urbana, Illinois, USA

M.S. degree, Electrical Engineering. Thesis topic: "Switch-Level Test Generation for MOS VLSI Circuits," supervised by Prof. Ibrahim N. Hajj.

1979-1983: American University of Beirut Beirut, Lebanon

B.E. degree (with distinction), Electrical Engineering. Employed as a part-time teaching assistant in the Electrical Engineering Department.

WORK EXPERIENCE :

Since 1999 : University of Toronto Toronto, Ontario, Canada

Professor (since 2001), served as Department Chair (2009-2019) and Vice-Chair (2004-2007), Associate Professor (1999-2001), with the Edward S. Rogers Sr. Department of Electrical and Computer Engineering (ECE). Research interests include Computer-Aided Design (CAD) techniques for integrated circuits, with the goal of contributing to design methodologies for power estimation and modeling, power supply integrity, timing verification under statistical variability, and reliability in metal lines.

1992-1999 : University of Illinois at Urbana-Champaign Urbana, Illinois, USA

Assistant Professor 1992-1997, then tenured Associate Professor 1997-1999, with the Electrical and Computer Engineering Department and the Coordinated Science Laboratory. Conducted research on power estimation and modeling for VLSI circuits, synthesis and optimization for low-power, ultra low-power circuits, and integrated circuits reliability.

1987-1992 : Texas Instruments Inc. Dallas, Texas, USA

Member of Technical Staff with the Semiconductor Process and Design Center (SPDC) at Texas Instruments. Worked with Dr. J.-H. Chern and Dr. Ping Yang, in the general areas of technology CAD, design for manufacturing, design-in reliability, and reliability analysis.

PERSONAL BACKGROUND :

Dual citizen of the US and Canada, originally from Lebanon.

HONOURS/AWARDS :

14. **IEEE/ACM William J. McCalla ICCAD Best Paper Award**, IEEE/ACM International Conference on Computer-Aided Design, November 2020.
13. **Safwat Zaky Research Leader Award**, Faculty of Applied Science & Engineering, University of Toronto, 2020.
12. **IEEE/ACM William J. McCalla ICCAD Best Paper Award**, IEEE/ACM International Conference on Computer-Aided Design, November 2019.
11. **IEEE/ACM William J. McCalla ICCAD Best Paper Award**, IEEE/ACM International Conference on Computer-Aided Design, November 2016.
10. **DAC Prolific Author Award**, for publishing over 30 papers at the Design Automation Conference (DAC), awarded June 5, 2013.
9. **Fellow of the Canadian Academy of Engineering (CAE)**, June 2010.
8. American University of Beirut (AUB), Faculty of Engineering and Architecture (FEA), **The FEA Distinguished Alumnus Award**, *in recognition of groundbreaking contributions to computer-aided design techniques for power management in integrated circuits*, May 2007.
7. Semiconductor Research Corporation (SRC) **Inventor Recognition Award**, 2005, for a patent submission on a low-leakage FPGA routing switch, with Navid Azizi.
6. **Fellow of the IEEE**, *for contributions to estimation and modeling of power dissipation in integrated circuits*, January 2003.
5. Semiconductor Research Corporation (SRC) **Inventor Recognition Award**, 2003, for a patent submission on a low-leakage asymmetric-cell SRAM, with Navid Azizi and Andreas Moshovos.
4. University of Illinois ECE Faculty **Outstanding Teaching Award**, 1999. Also, named, in 1997, to the “Incomplete list of teachers ranked excellent by their students.”
3. National Science Foundation (NSF) **Faculty Early Career Development Award (CAREER)**. Award of US\$200,000, in 1996, to fund work on reliability engineering for integrated circuits.
2. National Science Foundation (NSF) **Research Initiation Award (RIA)**. Award of US\$100,000, in 1993, to fund work on synthesis of reliable and low power VLSI circuits.
1. IEEE Transactions on CAD **Best Paper Award**, in 1992, for the paper “Probabilistic Simulation for Reliability Analysis of CMOS VLSI Circuits,” published in the April 1990 issue.

PATENTS :

Issued:

2. F. N. Najm, A. Moshovos, and N. Azizi, “Low Leakage Asymmetric SRAM Cell Devices,” *US Patent No. 7,307,905*, supported by the Semiconductor Research Corporation (SRC), December 11, 2007.
1. J. H. Anderson and F. N. Najm, “Leakage Power Optimization for Integrated Circuits,” *US Patent No. 6,993,737 B1*, supported by Xilinx Corp., January 31, 2006.

Other Disclosures:

3. F. N. Najm and S. Onaissi, “A Linear-Time Approach for Static Timing Analysis Covering All Process Corners,” *Invention Disclosure*, University of Toronto, April 2006.
2. N. Azizi, K. Pagiamtzis, and F. N. Najm, “A Soft-Error Tolerant Content-Addressable Memory (CAM) Using An Error-Correcting Match Scheme,” *Invention Disclosure*, University of Toronto, October 2005.
1. F. N. Najm, “A Logic Design Technique for Ultra Low-Power Logic Circuits based on Dynamic Control of the Standby Leakage Current,” *Invention Disclosure*, University of Illinois at Urbana-Champaign, June 1996.

INVITED TALKS :

19. F. N. Najm, "Efficient Simulation of Electromigration Damage in Large Chip Power Grids," *16th International Conference on Reliability and Stress-related Phenomena in Nano and Microelectronics*, San Jose, CA, November 4–6, 2019.
18. F. N. Najm, "Managing Design Challenges for Power-Constrained SOCs," *Cadence Speaker Series, Cadence Design Systems*, San Jose, CA, August 19, 2015.
17. F. N. Najm, "Verification and Design of the Power Delivery Network in VLSI Circuits," *CMOS Emerging Technologies Research Symposium*, Vancouver, BC, May 20-22, 2015.
16. F. N. Najm, "Physical Design Challenges in the Chip Power Distribution Network," *International Symposium on Physical Design*, Monterey, CA, March 29-April 1, 2015.
15. F. N. Najm, "Full Chip Statistical Electromigration Checking," *13th International Workshop on Stress-Induced Phenomena in Microelectronics*, Austin, TX, October 15-17, 2014.
14. F. N. Najm, "Verification of the Power Delivery Network in VLSI Circuits," *IEEE International Workshop on High-Performance Chip, Package and Systems*, (Keynote Address), Ottawa, Canada, November 16, 2013.
13. F. N. Najm, "Overview of Vectorless/Early Power Grid Verification," *ACM/IEEE International Conference on Computer-Aided Design*, San Jose, CA, pp. 670-677, November 5-8, 2012.
12. F. N. Najm, "Power Management for VLSI: The History and the Outlook," plenary talk, *IEEE 20th International Conference on Microelectronics*, Sharjah, UAE, Dec. 14–17, 2008.
11. F. N. Najm, "Power Management for VLSI Circuits and the Need for High-Level Power Modeling and Design Exploration," plenary talk, *IEEE/FMCA Formal Methods in Computer Aided Design*, Austin, TX, Nov. 11-14, 2007.
10. F. N. Najm, "Power Management for VLSI Circuits," *6th Faculty of Engineering and Architecture (FEA) Student Conference*, American University of Beirut, May 23–24, 2007.
9. F. N. Najm, "On the Need for Statistical Timing Analysis," panel discussion, *ACM/IEEE Design Automation Conference*, Anaheim, CA, June 13–17, 2005.
8. F. N. Najm, "Power Estimation and Modeling for VLSI Circuits," *Distinguished Lecture Colloquium*, Dept. of Electrical and Computer Engineering, University of Toronto, Feb. 2, 1999.
7. F. N. Najm, "High-Level Power Estimation and Modeling," Dept. of Electrical Engineering and Computer Science, University of California, Berkeley, April 23, 1998.
6. F. N. Najm, "High-Level Power Estimation and Modeling," *Dept. of Electrical Engineering/Systems*, University of Southern California, March 1998.
5. F. N. Najm, "Low-Power Design Methodology: Power Estimation and Optimization," *Great Lakes Symposium on VLSI*, March 1997.
4. F. N. Najm, "Power Estimation Techniques for Integrated Circuits," *IEEE International Conference on Computer-Aided Design*, San Jose, CA, November 5–9, 1995.
3. F. N. Najm, "Power Estimation Techniques for VLSI Circuits," *ECE Dept. Distinguished Lecture Series*, Carnegie Mellon University, October 1995.
2. F. N. Najm, "Feedback, correlation, and delay concerns in the power estimation of VLSI circuits," *Design Automation Conference*, San Francisco, CA, June 12–16, 1995.
1. F. N. Najm, "A Survey of Power Estimation Techniques in VLSI Circuits," *ECE Dept. Graduate Seminar*, University of Iowa, Feb. 1995.

SERVICE IN PROFESSIONAL SOCIETIES :

13. **Advisory Board Member**, International Conference on Reliability and Stress-Related Phenomena in Nano and Microelectronics (IRSP), 2019.
12. **Executive Committee Member**, International Symposium on Low-Power Electronics and Design (ISLPED), 1999-2013.
11. **Associate Editor**, IEEE Transactions on Computer-Aided Design, 2001–2009.
10. **Associate Editor**, IEEE Transactions on VLSI, 1997–2002.
9. **General Chairman**, International Symposium on Low-Power Electronics and Design, 1999.
8. **Technical Program Co-Chairman**, International Symposium on Low-Power Electronics and Design, 1998.
7. **Technical Committee Member of:**
 - Design Automation Conference (DAC 1998-99, 2006–08)
 - International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (the TAU Workshop) (TAU 2007–08)
 - International Conference on Computer-Aided Design (ICCAD 1995–97, 2001–2003)
 - International Symposium on Low-Power Electronics and Design (ISLPED 1995–2000)
 - International Symposium on Quality Electronic Design (ISQED 2000–2004)
 - Custom Integrated Circuits Conference (CICC 1994)
 - International Conference on Computer Design (ICCD 1999)
 - International Symposium on VLSI Technology, Systems, & Applications, Taiwan (VLSITSA 93)
 - International Workshop on Low Power Design (IWLDP 1994)
6. **Technical Program Chairman**, Great Lakes Symposium on VLSI, University of Illinois, 1997.
5. **Editor**, Simulation and Modeling Column, IEEE Circuits and Devices Magazine, 1995–1997.
4. **Guest Editor**, VLSI Design Journal, 1995.
3. **Guest Editor**, International Journal on High Speed Electronics and Systems, 1995.
2. **Workshop Co-chairman**, Illinois Computer Affiliates Program (ICAP) workshop, University of Illinois at Urbana-Champaign, 1993.
1. **Session Chairman**, on numerous occasions for ICCAD, VLSITSA, DAC, IWLDP, and ISLPED.

SERVICE IN THE UNIVERSITY :

At the University of Toronto

11. Chair, ECE Department, 2009-2019, including chairing the ECE Executive Committee, Advisory Committee, PTR Committee, and membership of the ECE Promotions Committee, the Faculty Chairs and Directors Committee, Executive Committee of Faculty Council, and the University Principals, Deans, Academic Directors and Chairs (PDAD&C) Committee.
10. Member, Examination Committee, Faculty of Applied Science and Engineering, 2008–2009.
9. Vice-Chair, ECE Dept., 2004–2007, including chairing the ECE Promotions Committee, member, Faculty Vice-Dean Search Committee, member, ECE PTR Committee, chair, ECE Computer Systems User Advisory Committee, chair, ECE Awards Committee, member, ECE Advisory Committee and member, ECE Executive Committee
8. Member, Faculty Senior Promotions Committee, 2003–2007
7. Chair, ECE Department Governance Committee, 2003–2004
6. Served on the Strategic Planning Organizing Committee, 2003–2004
5. Chairman of the Computer and Communications Faculty Search Committee, 2002–2003

4. Chairman of the Computer Faculty Search Committee, 2001–2002
3. Chairman of the Computer Engineering Group, 2000–2003
2. Served on the Group Review Committee, 1999–2000
1. Served on the Computer Engineering Group Search Committee, 1999–2000

At the University of Illinois

6. ECE Department Computer Resources and Education Committee, 1999
5. Circuits and Signal Processing Area Committee Chair, 1997–1998
4. ECE Department Curriculum Committee, 1996–1999
3. Served on the ECE Department ABET Accreditation Committee, 1994–1995
2. Served on the ECE Department Graduate Committee, 1994–1995
1. Chairman, CSL Black/Whiteboard Committee, 1992–1993

CONSULTING ACTIVITIES :

20. Mentor Graphics Corp., Fremont, CA, 2013.
19. Member, External Advisory Board for the Department of Electrical and Computer Engineering at the American University of Beirut, Dec. 2008 – Dec. 2010.
18. Nascentric Inc., Austin, TX, 2008.
17. Nascentric Inc., Austin, TX, 2007.
16. Intel Corp., (Visiting Faculty/Consultant) Hillsboro, OR, 2007.
15. Synopsys Inc., Mountain View, CA, 2006.
14. Nascentric Inc., Austin, TX, 2005.
13. Nascentric Inc., Austin, TX, 2004.
12. Intel Corp., (Visiting Faculty/Consultant) Hillsboro, OR, 2003.
11. Silicon Metrics Corporation, Austin, TX, 1999–2003.
10. ATI Technologies Inc., Unionville, ON, 2000.
9. Actel Corp., Sunnyvale, CA, 2000.
8. Taveren Technology, Austin, TX, 1998.
7. Synopsys Corporation, Mountain View, CA, 1997.
6. International Business Machines (IBM) Corporation, Fishkill, NY, 1996, 1997.
5. Synopsys Corporation, Mountain View, CA, 1996.
4. Intel Corp., (Visiting Faculty/Consultant) Folsom, CA, 1996.
3. Texas Instruments Incorporated, Dallas, TX, 1995.
2. Intel Corp., (Visiting Faculty/Consultant) Santa Clara, CA, 1994.
1. Dimensions in Quick Design Turnaround (DQDT), Carlsbad, CA, 1994.

TUTORIALS AND TECHNOLOGY TRANSFER :

5. Full-day tutorial, with B. Krauter (IBM), R. Panda (Freescale), and E. Chiprout (Intel), on “Design and Analysis of High-Performance Package and Die Power Delivery Networks,” *ACM/IEEE 44th Design Automation Conference (DAC-07)*, San Diego, CA, June 9, 2007.
4. Full-day tutorial, with A. Devgan (IBM), S. Narendra (Intel), and D. Blaauw (Michigan), on “Leakage Issues in IC Design,” *IEEE International Conference on Computer-Aided Design*, San Jose, CA, November 9–13, 2003.

3. Full-day tutorial, with A. Chandrakasan (MIT) and R. Panda (Freescale), on “Low Voltage/Low Power Design Methodologies and CAD,” IEEE International Conference on Computer-Aided Design, November 1999.
2. Technology Transfer Course, “Power Estimation Tools for VLSI Circuits,” for the Semiconductor Research Corporation (SRC), University of Illinois, Urbana, IL, June 1996.
1. Short course, “Dynamics of Physical Systems Under Noise,” for Texas Instruments Inc., Dallas, TX, March 1994.

UNIVERSITY COURSES TAUGHT :

At the University of Toronto

6. ECE-1777, Computer Methods for Circuit Simulation. A graduate course covering the theoretical and numerical techniques underlying standard circuit simulation, using my textbook on the subject.
5. ECE-451, VLSI Systems. This is a 4th year course. In my first offering of the course, I completely redid the lecture part, using my previous VLSI course at Illinois as a basis. In the 2nd offering, I upgraded the labs so that the students are now using custom IC design software, such as Mentor, Cadence, and Synopsys tools, instead of FPGAs.
4. ECE-1768, Reliability of Integrated Circuits. This is a new graduate course that I developed, along the lines of my reliability course at Illinois.

At the University of Illinois

3. ECE-325, Introduction to VLSI Systems Design. This is a 4th year course, but was also taken by some graduate students. In my first semester on campus, I did a major overhaul of this course, by updating the material and bringing in the latest material from my industrial practice.
2. ECE-342, Microelectronics. This is a 3rd year course taken by about 100 students. I was course director for this course; I was also responsible for selection of a new text and for restructuring the course material.
1. ECE-484, Reliability Engineering for Integrated Circuits. This is a graduate course which I created. My course notes have been incorporated into a textbook on this material, in collaboration with a colleague from Texas Instruments, published by John Wiley and Sons.

GRADUATE STUDENT SUPERVISION :

	Current	Graduated
Ph.D.	0	19
MASc.	2	33

CURRENTLY SUPERVISED :

2. Bijan Shahriari, since September 2020. Working on **MASc**.
1. Carl Chaanin, since September 2019. Working on **MASc**.

PREVIOUSLY SUPERVISED :

At the University of Toronto

40. Adam Issa, 2017–2019, **MASc August 2019** on “A Stochastic Approach to Electromigration Checking for Chip Power Grids.”

39. Zahi Moudallal, 2012–2019, **MASc August 2014** on “Generating Current Constraints for Power Grid Safety.” **PhD June 2019** on “Voltage-drop and Electromigration in Chip Power Grids.” Now at Tensortorrent, Inc. in Toronto.
38. Abdul-Amir Yassine, 2014–2016, **MASc July 2016** on “A Fast Metal Layer Elimination Approach for Power Grid Reduction in Integrated Circuits.” Now working on a PhD at the University of Toronto.
37. Mohammad Fawaz, 2011–2017, **MASc August 2013** on “Electromigration Reliability Analysis of Power Delivery Networks in Integrated Circuits.” **PhD September 2017** on “Power Grid Verification.” Now at Intel, Toronto.
36. Sandeep Chatterjee, 2011–2017, **MASc August 2013** on “Redundancy-Aware Electromigration Checking for Mesh Power Grids.” **PhD September 2017** on “Fast and Scalable Physics-Based Electromigration Checking for Power Grids in Integrated Circuits.” Worked for two years after graduation with Intel in Toronto; currently with Google in California.
35. Abhishek, 2010–2012, **MASc August 2012** on “Incremental Power Grid Verification.” Now at Synopsys in California.
34. Sari Onaissi, 2005–2011, **MASc June 2007** on “A Linear-Time Approach for Static Timing Analysis Covering All Process Corners.” **PhD June 2011** on “Circuit Performance Verification and Optimization in the Presence of Variability.” Now with Google in California.
33. Nahi Abdul Ghani, 2005–2011, **MASc June 2007** on “Handling Inductance in Early Power Grid Verification.” **PhD June 2011** on “Early Verification of the Power Delivery Network in Integrated Circuits.” Worked for three years after graduation at Altera, Toronto; currently with Google in California.
32. Pamela Al Haddad, 2009–2011, **MASc April 2011** on “Power Grid Correction using Sensitivity Analysis under an RC Model.”
31. Mehmet Avci, 2008–2010, **MASc August 2010** on “Early Dual Grid Voltage Integrity Verification.” Now at Altera in Toronto.
30. Meric Aydonat, 2008–2010, **MASc July 2010** on “Power Grid Correction Using Sensitivity Analysis.” Worked with Broadcom then IBM in California; currently with GE Healthcare.
29. Ankit Goyal, 2008–2010, **MASc June 2010** on “On-chip Power Grid Verification with Reduced Order Modeling.” Now at AMD in Toronto.
28. Khaled R. Heloue, 2003–2010, **MASc June 2005** on “Statistical Timing Analysis under Process Variations,” **PhD August 2010** on “Circuit Timing and Leakage Analysis in the Presence of Variability.” Now at AMD in Toronto.
27. Imad Ferzli, 2001–2009, **MASc Dec. 2003** on “Power Grid Statistical Analysis and Verification in Presence of Leakage Current Variations,” **PhD Feb. 2009** on “Verification and Planning of the Power Delivery Network in Integrated Circuits Under Design Uncertainties.” Now at CPPIB in Toronto.
26. Navid Azizi, 2001–2007, **MASc Dec. 2002** on “Low-Leakage Asymmetric-Cell SRAM”, **PhD May 2007** on “Challenges in Nanometre Digital Integrated Circuit Design.” Now at Altera Corp. in Toronto.
25. Bin Wu, 2001–2006, **PhD June 2006** on “Dynamic Range Estimation and Bitwidth Determination.” Now at Freescale Corp. in Phoenix, Arizona.
24. Denis Kouroussis, 2000–2006, **PhD January 2006** on “Power Grid Verification.” Now at ATI Technologies, Unionville, Ontario, Canada.
23. Kay Chan, 2003–2005, **MASc August 2005** on “Exploring Spatial Locality in VLSI On-Chip Power Grid.” Now at Intellon Corp. in Toronto.

22. Georges Nabaa, 2003–2005, **MASc July 2005** on “Minimization of Threshold-Voltage Variations and Their Impact in Circuits and FPGAs.” Now at Actel Corp. in San Jose, California.
21. David Ng, 2003–2005, **MASc July 2005** on “Modeling Circuit-Level Leakage Current Using Algebraic Decision Diagrams.” Went on to study law at the University of Toronto.
20. Jason Anderson, 2001–2005, **PhD June 2005** on “Power Optimization and Prediction Techniques for FPGAs.” Now at Xilinx Corp. in Toronto.
19. Maha Nizam, 2003–2005, **MASc June 2005** on “Power Grid Voltage Integrity Verification.” Graduated and left the country.
18. Rubil Ahmadi, 2001–2003, **MASc 2003** on “Timing Analysis in Presence of Power Supply and Ground Voltage Variations.” Now at ATI Technologies in Unionville, Ontario, Canada.
17. Roman Kordasiewicz, 2000–2002, **MASc 2002** on “Timing Verification of PD-SOI Circuits”. Went on to do a PhD at McMaster University in Hamilton, Ontario.
16. Mehrdad Shahriari, 2000–2001, **MASc 2001** on “A Gate-Level Timing Model for SOI Circuits”. Now at Genum Corp. in Oakville, Ontario, Canada.

At the University of Illinois

15. Kavel Buyuksahin, 1998–2003, **MS 1999** on “High-Level Interconnect Capacitance Estimation”, **PhD 2003** on “Early Power Estimation for VLSI Circuits”. At Intel Corp., in Portland, OR, USA.
14. Srinivas Bodapati, 1998–2003, **MS 1999** on “Pre-Layout Estimation of Individual Wire Lengths”, **PhD 2003** on “Bottom-up High-Level Current Macro-models for Logic Blocks”. At Intel Corp., in Santa Clara, CA, USA.
13. Joseph Kozhaya, 1996–2001, **MS 1997** on “Power Estimation for Sequential Circuits”, **PhD 2001** on “Analysis and Design of Power and Ground Networks for VLSI Circuits”. At IBM Corp., in Burlington, Vermont, USA.
12. Subodh Gupta, 1995–2000, **MS 1997** on “Power Macromodeling for High Level Power Estimation”, **PhD 2000** on “Bottom-up High-Level Power Modeling and Estimation”. At Cadence Design Systems, Inc., in California, USA.
11. Rouwaida Kanj, 1998–2000, **MS 2000** on “High Level Design Exploration and Optimization”. Went on to do a PhD with another Professor at Illinois, then took a position with IBM Austin Research Labs, in Austin, TX.
10. Xiaochun Tan (co-advised with E. Rosenbaum), 1998–2000, **MS 2000** on “Silicon-on-Insulator MOSFET Body Voltage Model for Application in a Timing Simulator”. At Freescale Corp. in Illinois.
9. Gilbert Yoh, 1997–1999, **MS 1999** on “A Statistical Model for Electromigration Failures”. At Agilent Technologies Inc., in Colorado, USA.
8. Mahadevamurthy Nemani, 1995–1998, **PhD 1998** on “High-Level Power Estimation”. At Intel Corp. in California, USA.
7. Luis Amaya (co-advised with P. Krein), 1995–1998, **PhD 1998** on “Simulation and Design of DC to DC Power Converters”.
6. Rajendran Panda, 1993–1996, **PhD 1996** on “Synthesis Techniques for VLSI Low-Power Circuits”. At Freescale Corp. in Austin, Texas, USA.
5. Jonathan Halter, 1995–1997, **MS 1997** on “A Gate-Level Leakage Power Reduction Method”. At Freescale Corp. in Austin, Texas, USA.
4. Vikram Saxena (co-advised with I. Hajj), 1995–1996, **MS 1996** on “Power Estimation for Sequential Circuits”. At Synopsys, Inc., in California, USA.

3. Michael Xakellis, 1993–1994, **MS 1994** on “Estimating Node Transition Densities with Statistical Simulation Techniques”. At Mercury Interactive Corp. in California, USA.
2. Yimin Zhang, 1993–1994, **MS 1994** on “Estimation of Node Maximum Transition Density”. At Intel Corp. in California, USA.
1. Harish Kriplani (co-advised with I. Hajj), 1991–1993, **PhD 1993** on “Worst Case Voltage Drops in Power and Ground Buses of CMOS VLSI Circuits”. At Cadence Design Systems, Inc., in California, USA.

PUBLICATIONS :

Books & Book Chapters

- [1] G. K. Yeap and F. N. Najm, Editors, *Low Power VLSI Design and Technology*. Singapore: World Scientific Publishing Co., 1996 (ISBN: 9-810-22518-0).
- [2] E. A. Amerasekera and F. N. Najm, *Failure Mechanisms in Semiconductor Devices*, 2nd Ed.. Chichester: John Wiley & Sons, 1997 (ISBN: 0-471-95482-9).
- [3] F. N. Najm, “Power Estimation and Optimization,” in *Encyclopedia of Electrical and Electronics Engineering*. New York, NY: John Wiley & Sons, February 1999.
- [4] F. N. Najm, *Circuit Simulation*. Hoboken, NJ: John Wiley & Sons, 2010 (ISBN: 978-0-470-53871-5).

Journal Papers

- [1] R. Burch, J. Hall, F. Najm, D. Hocesvar, P. Yang, and M. McGraw, “A CAD system for modeling voltage drop and electromigration in VLSI metallization patterns,” *Texas Instruments Technical Journal*, vol. 5, no. 3, pp. 74–84, May-June 1988.
- [2] F. Najm, R. Burch, P. Yang, and I. Hajj, “Probabilistic simulation for reliability analysis of CMOS VLSI circuits,” *IEEE Transactions on Computer-Aided Design*, vol. 9, no. 4, pp. 439–450, April 1990 (Errata in July 1990). (**Best Paper Award**)
- [3] F. Najm and I. Hajj, “The complexity of fault detection in MOS VLSI circuits,” *IEEE Transactions on Computer-Aided Design*, vol. 9, no. 8, pp. 995–1001, September 1990.
- [4] F. Najm, I. Hajj, and P. Yang, “An extension of probabilistic simulation for reliability analysis of CMOS VLSI circuits,” *IEEE Transactions on Computer-Aided Design*, vol. 10, no. 11, pp. 1372–1381, November 1991.
- [5] F. Najm, “Transition density: a new measure of activity in digital circuits,” *IEEE Transactions on Computer-Aided Design*, vol. 12, no. 2, pp. 310–323, February 1993.
- [6] R. Burch, F. Najm, P. Yang, and T. Trick, “A Monte Carlo approach for power estimation,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 1, no. 1, pp. 63–71, March 1993.
- [7] F. Najm, “Low-pass filter for computing the transition density in digital circuits,” *IEEE Transactions on Computer-Aided Design*, vol. 13, no. 9, pp. 1123–1131, September 1994.
- [8] F. Najm, “A survey of power estimation techniques in VLSI circuits,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 2, no. 4, pp. 446–455, Dec. 1994. (**Invited Paper**).
- [9] H. Kriplani, F. N. Najm, and I. Hajj, “Pattern independent maximum current estimation in power and ground buses of CMOS VLSI circuits: algorithms, signal correlations, and their resolution,” *IEEE Transactions on Computer-Aided Design*, vol. 14, no. 8, pp. 998–1012, August 1995.
- [10] M. Nemani and F. N. Najm, “Towards a high-level power estimation capability,” *IEEE Transactions on Computer-Aided Design*, vol. 15, no. 6, pp. 588–598, June 1996.
- [11] F. N. Najm and M. G. Xakellis, “Statistical estimation of the switching activity in VLSI circuits,” *VLSI Design*, vol. 7, no. 3, pp. 243–254, 1998.

- [12] R. Panda and F. N. Najm, "Post-mapping transformations for low-power synthesis," *VLSI Design*, vol. 7, no. 3, pp. 289–301, 1998.
- [13] M. Nemani and F. N. Najm, "High-level area and power estimation for VLSI circuits," *IEEE Transactions on Computer-Aided Design*, vol. 18, no. 6, pp. 697–713, June 1999.
- [14] S. Gupta and F. N. Najm, "Power modeling for high level power estimation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 8, no. 1, pp. 18–29, February 2000.
- [15] S. Gupta and F. N. Najm, "Analytical models for RTL power estimation of combinational and sequential circuits," *IEEE Transactions on Computer-Aided Design*, vol. 19, no. 7, pp. 808–814, July 2000.
- [16] J. N. Kozhaya and F. N. Najm, "Power estimation for large sequential circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 9, no. 2, pp. 400–407, April 2001.
- [17] S. Bodapati and F. N. Najm, "Pre-layout estimation of individual wire lengths," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 9, no. 6, pp. 943–958, December 2001.
- [18] V. Saxena, F. N. Najm, and I. N. Hajj, "Estimation of state line statistics in sequential circuits," *ACM Transactions on Design Automation of Electronic Systems*, vol. 7, no. 3, pp. 455–473, July 2002.
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