# The Prospects for Multivalued Logic: A Technology and Applications View

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*Abstract*—**Advances in multiple-valued logic (MVL) have been inspired, in large part, by advances in integrated circuit technology. Multiple-valued logic has matured to the point where four-valued logic is now part of commercially available VLSI IC's. Besides reduction in chip area, MVL offers other benefits such as the potential for circuit test. This paper describes the historical and technical background of MVL, and areas of present and future application. It is intended, as well, to serve as a tutorial for the nonspecialist.**

*Index Terms*—**Arithmetic, fault detection, logic circuits, multivalued logic, signal processing, VLSI.**

## I. Introduction

PROBLEMS of interconnection in digital systems [46] appear at two levels: Edge connection has long been recognized to be a basic limitation since, as larger chips become possible, the space for edge connection grows only linearly with edge length $n$, while the space for circuitry grows as $n^2$. Less well noted is the fact that on the chip itself, while the number of local modules grows as $n^2$, the number of interconnects in a generally connected network grows as $(n^2)!$ This latter observation has motivated an increasing use of on-chip buses and functional modularization. For example, in memory, buses in two dimensions provide the ultimate solution, reducing the interconnect dependency to a linear one. However, with this exception, there remains a serious problem whose minimization on a conventional basis is not clear. Note for example, that while one reduces the cost of global connections on a chip by combining basic operations into smaller numbers of separable and loosely connected functional modules, it is apparent that such a process leaves a new version of the old problem behind, hiding within each of the growing modules.

There is, however, a possibility of attacking this problem by passing more information on the interconnections between functional modules on a chip. For if more information can be conveyed, the number of interconnects can be reduced, increasing the space for modules and allowing their size and generality to increase. With generality would come the potential to resolve one of the major problems in VLSI system design today, namely the need for manageable and broadly-useable functional modules which can reduce the high cost of design. As we shall attempt to demonstrate, such an encoding may be available naturally in the form of multivalued logic.

Note that it is possible that problems in VLSI design are essentially problems of *binary* digital design alone. Consider, for example, the extreme situation in analog IC's, where interconnection complexity is not a problem. The reason is that the processing capability of each analog device is large in comparison with the number of signal and power leads it requires. In fact, it may be that conventional analog components are really too high level and perhaps overkill the interconnect problem. Certainly, with little impact on the number of interconnects, a much more basic set of analog elements than op amps and multipliers could be assembled.

While it is likely that analog devices have lost to digital in part on the basis of their focus on a limited subset of all problems, it is the precision and stability of analog devices which leaves something to be desired, and in this regard a digital system is clearly superior. But is the advantage sought to be found only in the binary domain? Does the exclusivity of binary in the field of digital VLSI design represent needless overcompensation? It is questions of this kind to which the present paper is addressed.

## II. A Prospectus

The historical development of circuits for multivalued logic was first summarized by Vranesic and Smith [76], [77], and subsequently by Smith [67], Vranesic and Smith [79], and Dao [15].

The development of circuitry for number bases larger than two has parallelled, with a time delay, the development of binary techniques. Base 3 received very early and continuing attention [23]. The early ternary designs were derivative of binary ones, emphasizing passive rather than active components, for example [76]. Consistent with the lack of implementation-oriented work on relevant switching theory [62] and a relative lack of appreciation of what had in fact been done, the base 3 designs were generally ad hoc particular cases. Several of these [23] exploited the inherent symmetry of ternary which is of great importance also in applications to arithmetic. In parallel with this activity was an interest in base 10 for computing systems, where implementation was in general on a binary-coded basis (for example, biquinary in the IBM 650). There was otherwise little interest in higher base circuitry with the possible exception of the design of accumulating "counters," some of which utilized capacitors to store a relatively large number of standardized charge packets.

Finally, in the late 1960's came a resurgence of interest in multivalued logic brought about by the dramatically increased accessibility to relatively complex but low-cost integrated circuitry, both binary and analog. And so in 1968 and 1970 appeared two of the major thrusts toward high radix multiple-valued logic. The first by Allen and Givone [1] introduced

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the literal gate and the use of thresholds and binary, while the second by Vranesic *et al.* [74] introduced cycling gates and the use of analog techniques in multivalued logic implementations.

## III. Directions for the Design of Multivalued Systems

Originally, digital design was a relatively ad hoc process incorporating all manner of available techniques. There were even some notable attempts in the late 1940's and early 1950's to venture to multivalued logic. Indeed, in early systems binary threshold logic was occasionally used, with the threshold chosen to perform a binary AND, OR, or a majority function. As applications grew, the need for some standardization became apparent.

At first, attention was directed to the most basic level, to the gate. Resistor-transistor-logic (RTL), a pseudoanalog (threshold) form of digital circuitry, was initially but temporarily popular. It was introduced as the need for standardization grew, and replaced by more sophisticated circuit families as the cost of active components fell. With standardization came increasing sophistication in logic design and the search for the ideal functionally-complete logic set. NOR/NAND logic began to dominate. Then as the cost of individual transistors dropped sharply, while wiring costs held steady, the digital IC appeared, incorporating a large number of active components. An intense activity in identifying and providing special gate combinations followed. As large numbers of IC packages appeared, the number and variety of flip-flops increased, in turn increasing the number of multiflip-flop composites suited to standard purposes–counters, shift registers, and the like.

Recently, the microprocessor chip has emerged, supported by and supporting the dramatic and significant VLSI technology. Now while the search for "truly universal" IC's continues, the development of anything more general than an increasingly-large general-purpose computer seems to elude us. Interestingly, this focus on more of the same has turned the attention of designers downward in functionality, and inward toward the chip itself, with evidence even that circuit-level design of complex systems is worthwhile [32], [48].

Meanwhile, the development of multivalued logic has proceeded since the pioneering work of Post [59] on many fronts, most notably philosophical, mathematical, and latterly technological. As already noted, some work in multivalued hardware can be identified in the 1950's, one example being the Russian design of a magnetics-based ternary computer called SETUN [23]. In the late 1960's, a major effort was directed at the formalization of the process, at the logic design of systems, and at the minimization of logic and related issues. Foremost among these considerations has been the concern for the ideal set of logic elements, a complete or overly-complete set which combines convenience of analysis and of implementation. It is apparent that such requirements are highly dependent on the evolution of technology. As a result, a very large number of such functions have been identified, with many conveniently available in several technologies.

## IV. Multivalued Logic

### A. Notation and Definitions

A multivalued signal in radix $R$ occurs conventionally as an ordered set of values of a signal variable, perhaps voltage, current, or charge. There are two major conventions for labeling values. The most common set extends binary notation in one direction only, to include 0, 1, 2, 3, $\cdots$ $(R-2)$, $(R-1)$, a set of $R$ values. A second called balanced [23], requires an odd radix $R = 2K + 1$, and values $(-K)$, $(1-K)\cdots -2, -1$, $0, 1, 2\cdots, (K-1), (K)$.

Any discussion of multivalued logic in a variety of radices and technologies requires an extensible notation. Accordingly, a system of signal-value labeling utilized by Dao [12] and others [20] will be followed. It is a positional notation, referenced to the standard logic-value ordering and a stated relationship between the values of the logical and physical variables. Usually, a positive logic notation is used in which more (or more positive) corresponds to a higher (logic) value. In this notation the reference set is conventionally $\langle 0, 1, 2, 3 \cdots, R-1\rangle$. When used at nodes other than the input of a single input device, such a label provides a list of corresponding values. For example, in a base 4 circuit in which the input is assumed (or stated) to be $\langle 0, 1, 2, 3\rangle$, the label $\langle 1, 2, 3, 0\rangle$ indicates that the labeled variable is always one logic value greater than the input, in a circularly-connected system in which 0 follows $(R-1)$. Such a circuit is called successor, suc $(x) = (x+1) \bmod R$, which in turn is a special case of a gate called (clockwise) cycle, $\overrightarrow{x}^{y} = (x+y) \bmod R$ for the variables $(y, R) = (1, 4)$, or counterclockwise cycle. $\overleftarrow{x}^{y} = (x-y) \bmod R$ for $(y, R) = (3, 4)$.

For circuits with two or more inputs, the notation can still be used if all inputs are labeled, in which case $R$ combinations of a total of $R^n$ in an $n$-input $R$-valued circuit can be notated. Otherwise, tables such as in Fig. 1 can be used.

Table I provides a summary of many (but not all) multivalued functions including a positional notated example. The functions listed can be placed in two sets: those which are convenient to implement, and those which are convenient for analysis and syntheses. Fortunately, these sets are not completely disjoint. However, their join is distinctly technology dependent, making some functions extremely easy to form in one technology and difficult in another. As the multivalued discipline evolves, work on algebra (and logic manipulation in general), proceeds at a rapid pace, with the continuing creation of technologically-basic yet functionally-tractable constructs. The paper by Davio and Deschamps [16] in this issue provides an excellent example of this process in action.

One can note that there are interesting relationships between the functions in Table I. For example, the two types of cycling gate, each considered as a function of two variables, are related as follows:

$$\overleftarrow{x}^{y} = \overrightarrow{x}^{z} \qquad \text{where } z = R - y.$$

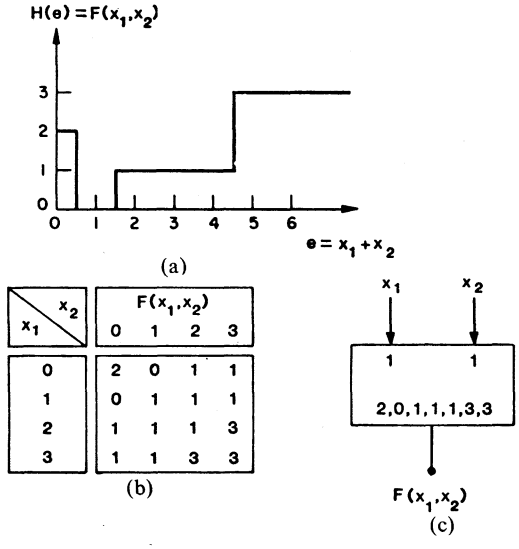



Fig. 1. A three-threshold two-input $MT(4)$ gate with unity weighting. (a) Truth table. (b) Transfer function. (c) symbol.

Likewise the interval and literal gates are related as follows:

$$\overset{a\,b}{x} = (R-1)\ \overset{[a\,b]}{x}$$

and

$$\overset{[a\,b]}{x} = \min\left(1, \overset{a\,b}{x}\right)$$

where the position of $(R-1)$ implies multiplication.

Note the elimination of redundancy in the notation for special cases, and the existence of understood convention. The latter is illustrated by the practice which simplifies the simple cycle, $\overset{\rightarrow 1}{x}$, to $\overset{\rightarrow}{x}$, corresponding to the successor function. The former can be noted with the delta literals and delta intervals. Here, $\overset{a\,a}{x}$ and $\overset{[a\,a]}{x}$ are each reduced to $\overset{a}{x}$, which is somewhat unfortunate since they are not equal. In context the situation is normally clear, however.

Two of the logic functions deserve special mention. Much the simpler conceptually is $T(x_0, x_1, \cdots, x_{R-1}, q)$ (no. 21), which defines a multiplexer or selector function under control of the multivalued variable $q$. In general, when $q$ has the value $k$, the $k$th input $x_k$ is selected for connection to the output. Although conceptually straightforward, and accordingly defined at an early date [49], the $T$ gate is not particularly easy to generate in some technologies nor noted for the simplicity of the networks it produces [37].

On the other end of the scale, the multithreshold radix-$R$ $MT(R)$ gate [18] is extremely versatile, capable of implementing a majority of other gates, but at some cost. In one technology, at least, that derived from ECL, it is relatively easy and straightforward to construct. In the $MT(R)$ gate shown in Fig. 1, each input is weighted and summed and the sum compared against a multivalued reference. For each value of the weighted sum, a particular output is defined. The process is akin to ROM table look-up with multivalued addressing and output. The output table (list) consists of $m$ entries ($H_1$–$H_m$), where $m$ is the number of values taken on by the weighted sum of inputs. This can be used as part of the name or label on a $MT(R)$ gate or provided as a graph. The input weights are provided in a second list, each item corresponding to an input by some convention, or, alternatively, labeled adjacent to each input on the logic symbol. It should be apparent that the $MT(R)$ gate is well suited to arithmetic operations (add, subtract), but less suited to lattice operations (max, min).

Finally, one should note that ease of algebraic manipulation is no longer of great concern, as shown by the trend toward table and pattern-oriented schemes [5] leading to the creation of good CAD tools.

### B. Complexity versus Radix

The circuit implementations of logic functions for low radix rely to a great degree on "natural" properties of devices: that a relay or vacuum tube or transistor can be easily arranged to be on or off underlies the importance of binary systems today.

Likewise, base 3 has some inherent advantages in an environment where one of two possibilities exist straightforwardly. The first of these is the ease with which a "middle" state between two outer ones can be found [53], [54] in which the outer devices are either both on or both off. The second of these is the more explicit combination of two radix-two elements at an upper and lower signal (voltage) level, with some means employed to suppress the fourth state [76].

Base 4 provides the most immediate example of the possibility of binary coding. It can be seen to be somewhat special since it uses two binary devices, a fact which can offer some advantage. However, generally speaking, while other radices of the form $R = 2^n$ have application advantages, their implementation is not particularly convenient.

With these exceptions, as the radix increases, multivalued circuits must utilize the most general techniques to be outlined in this paper. The extension of these common techniques to higher radices will be limited by a combination of processing uniformity and thus circuit yield, as well as by "confidence margin," the combination of noise margins and confidence of the user community.

## V. Categorization of MV Circuit Designs

### A. Representation of Signals in Multivalued Circuits

Available designs for multivalued circuits and systems use one or more of three electrical variables, namely charge, current or voltage.

Charge is the vehicle for information transfer in a variety of charge-coupled devices (CCD's) explicitly adapted to multivalued operation. These include the memory designs [83] and [70], the logic designs by Kerkhoff [42].

The availability of both memory and logic in a clocked sequential environment makes the possibility of continuous signal processing, filtering, etc., in CCD's [45] quite attractive. It has been demonstrated that a multivalued signal representation is a relatively natural one in an environment which is used both in analog and in binary digital modes. Multivalued signals offer

TABLE I
MULTIVALUED FUNCTION NOTATION AND DESCRIPTION

| No. | Common Name | Symbolic Notation: Primary | Symbolic Notation: Secondary | Positional Base 4 Example $a = 1, b = 2, y = \bar{x}$ | Value, Condition |
|---|---|---|---|---|---|
| 1 | Restoring Identity | $x$ | | ⟨0 1 2 3⟩ | $x$ standardized |
| 2 | (Diametrical) Inverse or Complement | $\bar{x}$ | | ⟨3 2 1 0⟩ | $(R-1)-x$ |
| 3 | Maximum | $\max(xy)$ | $x+y$<br>$x \vee y$ | ⟨3 2 2 3⟩ | $x$ if $x \geq y$, else $y$ |
| 4 | Minimum | $\min(xy)$ | $x \cdot y$<br>$x \wedge y$ | ⟨0 1 1 0⟩ | $x$ if $x \leq y$, else $y$ |
| 5 | Successor | $\tilde{x}$ | $\mathrm{suc}(x)$ | ⟨1 2 3 0⟩ | $(x+1) \bmod R$ |
| 6 | Cycle, (Clockwise Cycle) | $\tilde{x}^b$ | $\tilde{x}^1 = \tilde{x}$ (1 optional) | ⟨2 3 0 1⟩ | $(x+b) \bmod R$ |
| 7 | Counter Cycle | $\tilde{x}^b$ | $x^1 = \tilde{x}$ | ⟨2 3 0 1⟩ | $(x-b) \bmod R$ |
| 8 | Literal Function | $a_x b$ | $x(a,b)$ | ⟨0 3 3 0⟩ | $(R-1)$ if $a \leq x \leq b$, else 0 |
| 9 | Delta Literal $J$ Function | $\underset{x}{a}$ | $J(x)$<br>$a$ | ⟨0 3 0 0⟩ | $(R-1)$ if $x = a$, else 0 |
| 10 | Closed Interval | $\underset{x}{[a\ b]}$ | | ⟨0 1 1 0⟩ | 1 if $a \leq x \leq b$, else 0 |
| 11 | Open Interval | $\underset{x}{]a\ b[}$ | | ⟨0 0 0 0⟩ | 1 if $a < x < b$, else 0 |
| 12 | Delta Interval | $\underset{x}{a}$ | $\underset{x}{[a\ a]}$ | ⟨0 1 0 0⟩ | 1 if $a = x$, else 0 |
| 13 | Upper Closed Semi Interval | $\underset{x}{[a}$ | | ⟨0 1 1 1⟩ | 1 if $a \leq x$, else 0 |
| 14 | Lower Closed Semi-Interval | $\underset{x}{a]}$ | | ⟨1 1 0 0⟩ | 1 if $x \leq a$, else 0 |
| 15 | Lower Open Semi-Interval | $\underset{x}{a[}$ | | ⟨1 0 0 0⟩ | 1 if $x < a$, else 0 |
| 16 | Upper Open Semi-Interval | $\underset{x}{]a}$ | | ⟨0 0 1 1⟩ | 1 if $a < x$, else 0 |
| 17 | Threshold Literal (Up) | $U_a(x)$ | | ⟨0 1 1 1⟩ | 1 if $x \geq a$, else 0 |
| 18 | Step Literal (Down) | $D_a(x)$ | | ⟨1 1 0 0⟩ | 1 if $x \leq a$, else 0 |
| 19 | Truncated Difference | $x \boxminus a$ | | ⟨0 0 1 2⟩ | $x-a$ if $x \geq a$, else 0 |
| 20 | Limited Sum Truncated Sum | $x \boxplus a$ | | ⟨1 2 3 3⟩ | $x+a$ if $< R-1$, else $R-1$ |
| 21 | Multiplex, Selection, Transmission($T$), Tree | $T(x,y,q)$ | | ⟨0 1 2 3⟩<br>⟨3 2 1 0⟩ | $x$ if $q = 0$<br>$y$ if $q = 1$ |
| 22 | Multithreshold $MT(R)$ | $[H_1 - - - H_m]$<br>$(K_1 - - - K_n)$ | | ⟨$p$ $q$ $r$ $s$⟩ | Use a thresholded sum to look up a table of values. |
| 23 | MVNOR | $\overline{\max}(xy)$ | $\min(\bar{x}\,\bar{y})$ | ⟨0 1 1 0⟩ | $\bar{x}$ if $x \geq y$, else $\bar{y}$ |
| 24 | MVNAND | $\overline{\min}(xy)$ | $\max(\bar{x}\,\bar{y})$ | ⟨3 2 2 3⟩ | $\bar{x}$ if $x \leq y$, else $\bar{y}$ |

an opportunity to establish an economic balance between the quantized integrity of binary and the information density of analog signaling.

While charge is the dominant information carrier in multivalued CCD designs, voltage is also used internally as in coupling variable, and at the external input/output interface. In present near-commercial designs, the interface is usually binary-coded. Thus, the internal radix is most likely to remain some modest power of 2, quaternary being the simplest choice. CCD designs for radix 4 [70] and 32 [83] have been reported.

Current is used exclusively for the representation of multivalued variables in multivalued $I^2L$ ($MVI^2L$) introduced by Dao [21] and others [22], [67] around 1976 as a derivative of the binary $I^2L$ structure first announced in 1972 [2], [36]. Voltage, the dominant external variable in binary $I^2L$, plays an important role in $MVI^2L$, both at the external interface, and as an internal binary variable, controlled by the sign of a current difference.

A combination of current and voltage is used in a variety of multivalued, "current mode" logic (CML) designs based on binary emitter-coupled logic (ECL) [17], [5]. In these designs,

as in MVI$^2$L, currents are made available to be added (but not usually subtracted) under control of binary threshold devices. Such addition is followed immediately by conversion of current to a multivalued voltage on which binary multithreshold comparators operate directly. This approach may be contrasted with that in I$^2$L in which thresholding is performed by subtracting an accumulated signal current from a reference current. The net output current, being of one of two polarities, operates a single threshold binary switch (in voltage mode).

Although the charge-based and current-based designs presently show the greatest promise for high radix application ($R \geq 4$), designs using voltage exclusively have been important for radix 3 [54], [24], and show some potential for application to higher radices [26]. The voltage offset inherent in enhancement devices, the metal oxide semiconductor transistor (MOS(T)) and bipolar junction transistor (BJT), and diodes, have been used directly for thresholding at the input [52], while diode-connected field effect transistors (FET), as well as junctions themselves, have been used to establish output levels [52], [24]. The low resistance and zero offset of conducting MOS devices have been very important [55], while GaAs MESFET circuits show promise [71] of very high-speed operation.

### B. Value Quantization

In all realizable logic systems, whether binary or multivalued, the most important property is that of logic value integrity. There are three aspects of this integrity, namely generation, transmission and detection. Generation refers to all possible means by which acceptable standardized logic signals are produced within a logic network. Transmission refers to the properties of the media through which logic signals propagate including wiring and that type of logic, called nonrestoring or nonstandardizing, which does not provide a standardized output signal. Diode logic and some parts of MVI$^2$L [15] are examples of nonrestoring logic. Detection refers to the means by which a logic signal is interpreted such that its information content is correctly retrieved.

The range over which a logic value is correctly detected exceeds the range over which a value is generated and propagated by an amount called the noise margin. Here, "noise" refers to the uncertainty introduced by the environment including crosstalk from other elements, variation in power supplies, etc., which may allow one logic value to be interpreted as another. To minimize the effect of noise, the separation between signal levels should be made relatively large.

However, when a requirement for speed is added to a logic system, a conflicting requirement on logic value separation is added. This requirement implies that signal value separation be made as small as possible, particularly on generally distributed signal lines. Thus, high-speed logic families do not usually use nonrestoring logic components in a general way, but rather only within the boundaries of an identified logic gate. Such is the case in common binary families such as T$^2$L with diode-like logic at its multiemitter input, and ECL which includes the possibility of multiemitter logic at its output. Interestingly, while ISL, a later variant of I$^2$L [15] uses output diodes rather than multiple collectors, it does so primarily and intentionally to reduce signal value separation to obtain a benefit of speed at the expense of noise margin.

The situation is somewhat more complicated in multivalued logic as we shall see.

## VI. Steps Toward the Design of Multivalued Circuits

### A. Basic Elements

At the present state of technology there exists no simple inherently multivalued signal-restoring element. While such devices have been sought [79], and some potentially identified, they remain essentially laboratory curiosities. However, composite circuits of more basic linear and nonlinear components have been developed. One of these utilizes a multistep nonlinear resistor, called a step load resistor or SLR [77], as a load in a multistable feedback circuit in which linear gain is provided by a transconductance amplifier. An SLR suited to base 5 is shown in Fig. 2 with its transfer characteristics. For a modest improvement in the spacing of states, relative diode areas or current values can be tapered by design.

Although in a sense this SLR is fairly simple, appearances are deceiving. An IC implementation would necessitate a great many active devices employed as current generators. Thus, it is more reasonable to attack the problem directly, as shown in Fig. 3, which depicts a fairly large part of a functional device using the technology called $MT(R)$ by its originators [18]. Here, the voltage thresholding and amplification are combined in difference amplifier pairs acting as binary comparators with multiple reference thresholds. The input and output of the device as shown is current. Current directed toward the negative power supply is mirrored by $T_1$ and $T_2$ to flow from ground via $R$. This resistor acts as a voltage to current converter which provides a negative voltage version of the 5-valued signal at $S$. The voltage at $S$ is analyzed by a set of comparators referenced to a set of equally-spaced, ground-referenced voltages, $V_{T1}$–$V_{T4}$. Each comparator switches $I_o$, a unit value of current. As the voltage $S$ falls and reaches a threshold, the even numbered member of the pair switches $I_o$ to the output, increasing the output current by one unit. If the output is connected back to the input, the input current will also fall. Thus, providing the voltage reference thresholds are arranged to lie at $I_oR/2$, $3I_oR/2$, etc., such a connection produces a multiply-stable circuit.

Note that this basic circuit provides many other possibilities. While it has been presented as a current mode device in which current addition is straightforward, the inclusion of a resistor in series with the input provides a multivalued voltage signal. Each of several such resistors connected to the current node input provides a voltage input, and the collection, a voltage adder.

Furthermore, two (or more) output voltages may be combined nonlinearly using n-p-n emitter followers which provide current gain as well as a rectifying junction. The emitters of the followers, when connected to a single input resistor, provide it with the larger of the two source voltages, creating a multivalued maximum or max function. In a related manner, using biassed followers and diodes, the minimum of two or more voltages can he found, providing the min function.

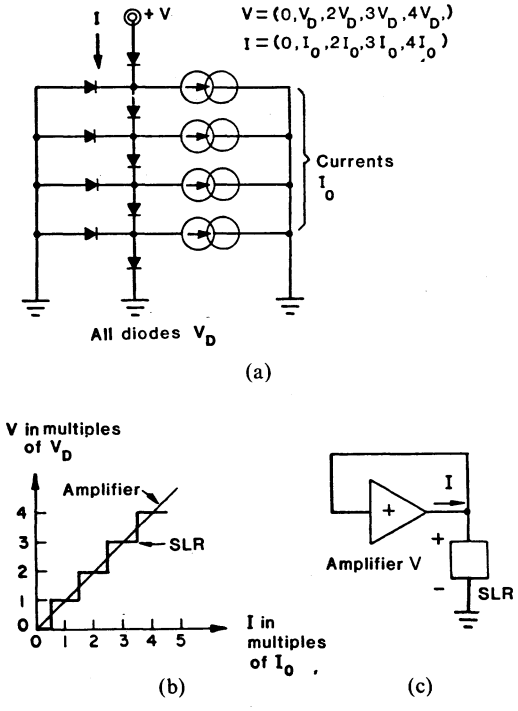



Fig. 2. The step load resistor (SLR). (a) Implementation. (b) Transfer characteristic. (c) Application environment.

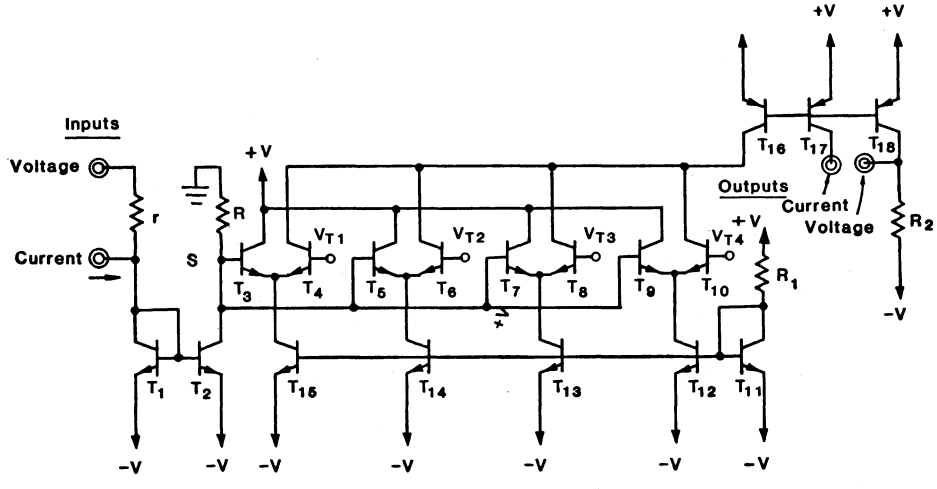



Fig. 3. A five-valued threshold element $MT(R)$ connectable as an equivalence, restorer, or identity gate.

### B. Memory Elements

We will return now to the closed-loop storage application since it raises an important issue, namely a question of the gating of memory circuits. One means of storing a signal (logic value) is to break the feedback loop, then connect the input to a signal whose value is to be stored, then quickly close the loop again while removing the signal. Such an idea is quite practical, being used for example in some CMOS binary storage devices.

There are, however, other approaches [77], [79]. For example, one of these, illustrated in Fig. 4, utilizes multivalued max and min. These can be viewed as being formed from diodes. A pair of diodes with cathodes joined provides (at the common cathode) a version of the larger of the two anode signals, a max function of its inputs. Conversely, a pair of diodes with anodes joined, provides (at the common anode) a version of the smaller of the two cathode signals, a min function of its inputs. One can see in Fig. 4 that the output $Y$ of the max gate will be the larger of $W$ or $X$, while the output of the min gate will be the smaller of $Y$ and $Z$, restored by $E$ to form $W$. Thus, if $W$ is initially low, raising $X$ will raise $W$, provided $Z$ is high. Correspondingly, while $X$ is low, lowering $Z$ will lower $W$. While $X$ is low and $Z$ is high, the results of the previous actions are sustained in the memory loop.

### C. A Binary Perspective

As the previous sections serve to illustrate, circuits for MVL may be seen to consist of optimal combinations of continuous and binary elements, with decision and control being essentially binary in nature. One approach to MVL circuit design which emphasizes the binary attributes of MVL has been highlighted recently [25], but used implicitly for some time by others [17]. It is to employ, immediately within the multivalued gate, a multiplicity of comparators to decompose the multivalued input signal into a multiwire binary code. Binary (pseudo) logic

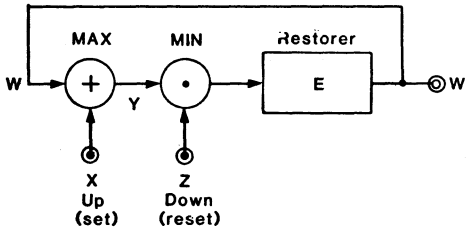



Fig. 4. A gateable storage element.

is used to implement the required logic functions and to control multivalued output circuitry connected to the output(s) from which multivalued signals are propagated. This idea is summarized in Fig. 5 which, although quite general, may be considered to represent a unary function such as complementation or cycling.

While at first encounter this idea may seem quite inefficient, apparently representing abandonment of the multivalued approach, the situation is somewhat more subtle. It is that the central part of Fig. 5, while binary, operates in an especially constrained environment in which many of the usual requirements on binary logic gates are reduced or removed entirely. Thus, although local information flow is very loosely coded, connections are short and represent a small layout burden. Furthermore, these short connections have low capacitance and well-defined fan-out. The consequence is that the cost of the binary part of the circuit is greatly reduced.

It is interesting to reflect on this situation in the light of observations made by VLSI designers [48] on the role of *circuit* minimization in large binary *logic* designs. For example, Forbes [72] has reported a considerable saving in the design of a CMOS single chip processor by judicious use of nonstandard logic. Viewed in this light, multivalued logic building blocks may be seen to provide a means to limit the scope over which circuit minimization must range. Such blocks of locally optimized, general-purpose logic are available for connection in the multivalued signal domain where information content of interconnects is greatly increased.

## VII. Characterization of Circuits by Physical Variable

### A. Charge Mode

The fundamental concept in charge mode devices [42] is that of a charge storage well whose capacity is under both geometric and voltage control. The maximum charge capacity of a well is

$$Q_{\max} = C \cdot (V_1 - V_2) \cdot A \qquad (1)$$

where $A$ is the storage gate area, $V_1$ its potential, $V_2$ the highest potential on adjacent (barrier) electrodes, and $C$ a (capacitive) constant. Charge is moved from well to well in a synchronous fashion by means of clocked gates and also can flow asynchronously under local control.

Voltage sensing is possible if the storage gate is allowed to float. A floating gate connected to a barrier gate can be used conditionally [via $V_2$ in (1)] to control the capacity of a well. If a charge packet propelled to a well by the clock system exceeds the well capacity [as defined by (1)], charge can spill

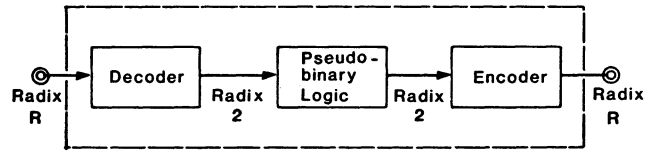



Fig. 5. A generalized radix $R$ (unary) functional block.

over to adjacent well(s). Since well capacity is under voltage (and thus charge) control, this skimming property implements both subtraction and thresholding. Rearrangement of the same idea allows charge to be divided in ratios which depend on the relative areas of adjacent wells.

Since the basic mechanism, being subject to leakage, is volatile, the clock, whose period is adjustable to suit the application, must maintain a minimum rate. Signal (charge) restoration is by means of conditionally gated sources. Floating gates needed for control of conditional transfers are used also at the output interface, connected directly to the gate electrode of a MOSFET output device. A companion paper in this issue [45] focuses on CCD techniques.

### B. Current Mode

The basic element in MVL current mode logic systems is a current generator, usually having a multiplicity of outputs. In the usual IC implementation, such a generator uses a current mirror, a simple current sink version [67] of which is shown in Fig. 6. Current forced externally to flow in diode-connected $T_1$ (from $R$) establishes a base emitter voltage at which each of $T_2$ to $T_n$ conduct the same current, extracting it from connected circuits. Multiples of the basic current $I$, that is $2I$, $3I$, etc., are easily created by parallelling collectors. The figure shows $T_n$ and $T_{n-1}$ parallelled to provide a current $2I$.

The MVI$^2$L logic family, a basic element of which is shown [11]–[13] in Fig. 7 uses several of these ideas. The single device with multiple collectors has many of the properties of the multiple device arrangement shown in Fig. 6, with the added benefit that the current in each collector is unaffected by loading of any other. Each of the multiple collectors is sized to carry the same current. One of these is "folded back" and connected to the base. Now if the input is open-circuited, and the $\beta$ of the composite device is reasonably high, the current $I$ (usually formed as part of a p-n-p mirror) is taken by the folded collector, causing all of the output currents to be $I$ (or less depending on load alone).

Now if a current $X$ is extracted from the input, only $(I\text{-}X)$ will flow in the folded collector to be replicated in each of the other collectors as $(I\text{-}X)$. When $X$ is made to exceed $I$, the device, lacking (a small) base current, turns off; its base voltage goes to zero and all of its collector currents go to zero. In this mode it can be seen to operate as a multiple output binary switch, providing currents of $I$ for input of 0 and currents of 0 for an input in excess of $I$. Thus, we see that the basic I$^2$L building block, as well as having direct input/output compatability, incorporates addition (joining of collectors), subtraction (for total input currents $<I$), as well as thresholding and binary switching (for total input current $>I$). It is this versatility which is likely to make I$^2$L the most powerful contender for high-radix MVL design.

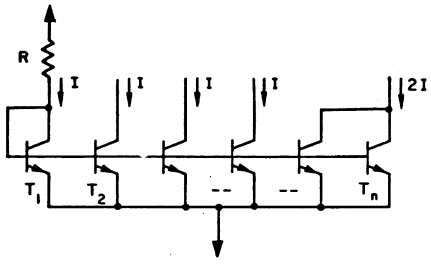



Fig. 6. A current mirror (current sink).

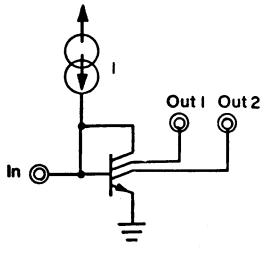



Fig. 7. The basic multivalued I²L building block.

The only basic feature which a simple MVI²L gate lacks is inherent multivalued restoration (see Fig. 8). The number of logic levels in I²L is limited only by fabrication tolerances. As reported in various ways [21], radix 4 is seen to produce reasonable yields.

Multivalued emitter-coupled logic [18], MVECL, exhibits some of the properties of MVI²L but with certain additional complexities. However, by virtue of nonsaturated operation, it can he made faster than conventional MVI²L.

Fig. 9 shows the basic component of ECL, the current switch. The input to this circuit is a voltage, which if lower (by about 120 mV) than $V_{REF}$, directs $I$ into $R_2$, and if higher (by the same amount) directs $I$ into $R_1$. Additional inputs allow considerable flexibility. For example, a third transistor with emitter and collector connected to those of $T_1$, and with base as input, forms the logic functions of the two inputs $x$ and $y$

$$\left.\begin{aligned} P &= \overline{\max}\,(x, y) = \overline{x + vy} \\ Q &= \max\,(x, y) = x + vy \end{aligned}\right\} x, y \in \{0, 1\}.$$

For multivalued applications, several currents can be combined at a collector node (and converted to voltage by the load resistor). The current $I$ may be provided by weighted current generators or other switches suitably biased. In all cases a multivalued output voltage can be created to appear at the collector of the upper switch (such as $T_1$ or $T_2$ above). To prevent saturation of $T_1$, for example, whose output and input are complementary, the highest input voltage must not go much above the lowest output voltage.

In order to make these barely overlapping ranges input–output compatible, it is necessary to use some level-shifting device. This may be a current mirror, such as shown at the right in Fig. 3, which processes the current-mode internal variable and supplies an equal current at a level compatible with the input. Alternatively, in voltage mode a level shifter must be applied at either input or output. This would consist typically of an emitter follower (alone for radix 2) at input *or* output, plus a number (which depends on the radix and choice of unit signal value) of resistors or diode-connected transistors and a current source supply [8]. Fig. 10 shows the basic idea suited

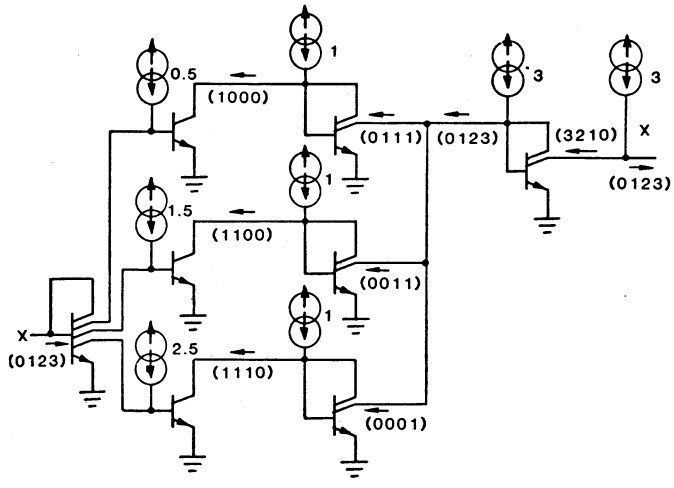



Fig. 8. An I²L quaternary restorer.

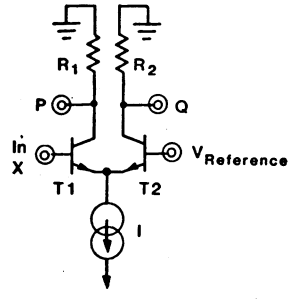



Fig. 9. The basic ECL current switch.

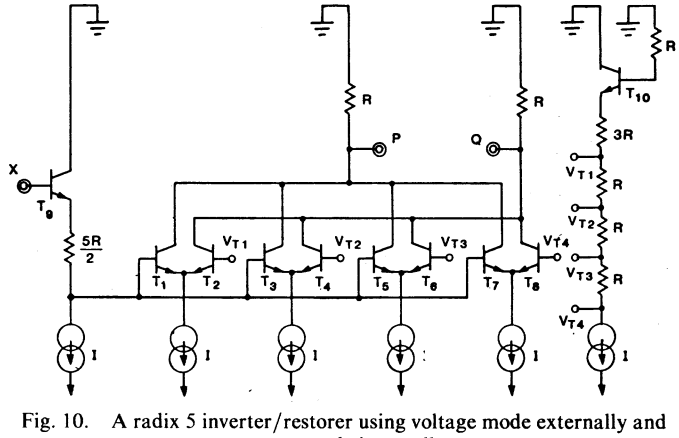



Fig. 10. A radix 5 inverter/restorer using voltage mode externally and current mode internally.

to a radix 5 inverter/restorer resembling Fig. 3 and having a unit value of 0.4 V. Here level shifting is done at the input of the circuit.

Note that this circuit is able to illustrate another option available in a mixed mode (current and voltage) MVL system, namely a choice of external variable. While the circuit shown obviously uses voltage as the MVL input–output variable, if one allows the load resistor $R$ (shown attached to $P$ and $Q$) to be attached instead to the input ($X$), then the communicated variable may be seen (technically) to be current. However, since the current-to-voltage conversion is done simply at the load with a resistor, and coupling is bilateral, the interconnect also contains a voltage version of the MVL signal [6]. Alternatively, if a current mirror is used at the input, very little voltage variation on the interconnect will be observed.

### C. Voltage Mode

There are two basic requirements of a restoring voltage mode MVL circuit, namely input thresholding and output level setting. As we have seen in other cases, a major limitation (in the voltage domain) remains the lack of a truly flexible threshold device. Basic components typically have a single fixed threshold. The most flexible device available thus far is the ECL current switch having an easily adjusted comparator point, and a relatively narrow switching band.

A modest breakthrough in this aspect of MVL was CMOS which can be viewed as having two thresholds, making it well-suited to ternary logic applications [53]. While development was assisted by the realization of the corresponding advantage of complementary junction transistors, the addition of the high impedance input property of MOS devices produced the key. Fig. 11 illustrates this point. Here, each CMOS enhancement device acts as a reasonably ideal binary switch with a threshold which ensures that with $X$ high (+3), $T_1$ is off while $T_2$ is on; with $X$ low (−3), $T_1$ is on while $T_2$ is off; with $X$ in the middle, both are on. When exactly one of the devices is on, all outputs are in a state opposite to the input. With both devices on (the middle input state), the centrally connected output is also in the middle, while the others fall to each side. Thus, $T$ provides a (diametrical) inverse of the input

$$T = \overline{X}$$

while $P$ and $Q$ provide literal functions

$$P = {}^{-1}X^{0}_{\bar{1}} = X \text{ and } Q = \overline{{}^{0}X^{1}} = X^{-1}$$

as shown in Fig. 11(b).

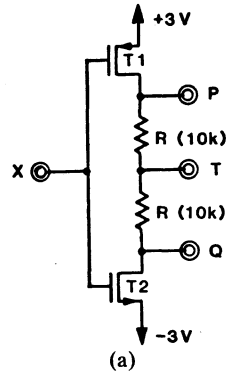
Note that the requirement for 3 stabilized output states is met by a combination of two standard approaches. Specifically, the outermost states are established by connection to the outer power rails, while the inner state is formed as a linear sum using a resistive voltage divider.

## VIII. Voltage Mode Circuit Principles

### A. Input Circuits

Input quantization in voltage mode circuits requires a set of standardized threshold comparators. The most general approach to their design involves the use of differential pairs and a set of references established by various means to be identified in a subsequent discussion. While this technique is appropriate in ECL (76) technology, where it brings the advantage of high speed and precise control, the overhead is quite high. Particularly for small bases, alternatives have been sought which utilize the thresholding porperties of single devices. Historically, several early base 3 designs using junction transistors were based on multiplication of the base emitter drop using input voltage dividers [79]. Another direction of attack involved the use of junction diode strings. Etiemble's schemes for radix three [24] and even radix four [26], based on modifications of TTL, are of this type. Fig. 12 provides an example of such circuits.

In the early 1970's another contribution to CMOS design




| X | P | T | Q |
|---|---|---|---|
| -3 | +3 | +3 | +3 |
| 0 | +3 | 0 | -3 |
| +3 | -3 | -3 | -3 |

(b)

Fig. 11. A CMOS ternary inverter. (a) Circuit. (b) Truth (voltage) table.

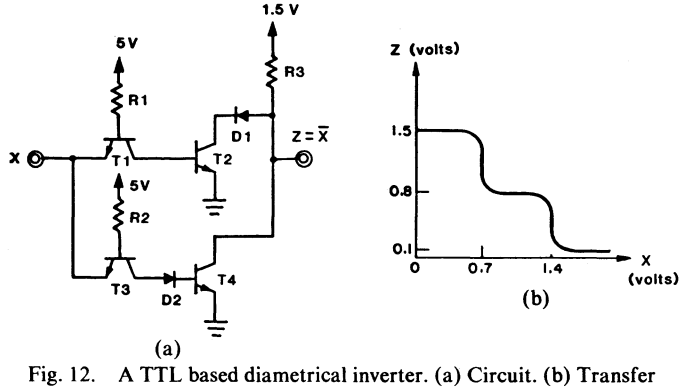



Fig. 12. A TTL based diametrical inverter. (a) Circuit. (b) Transfer characteristic.

was made by Mouftah [54], as shown in Fig. 11. As already noted, his original idea arranged, by the use of the output resistors, to split the single threshold of a binary CMOS gate. With thresholds of the individual matched complementary FET's separated, and two power rails to establish two input thresholds, the scheme is inherently limited to radix 3. Others, for example Huertas [39], introduced diode-connected FET's to offset the device threshold from the power rails. Fig. 13 shows his circuit for establishing the lower of three thresholds in a radix 4 circuit. The upper threshold is detected by a complement of this circuit, while the central threshold uses a conventional CMOS inverter. The major difficulty with this approach is that the binary output signal levels are seriously limited by the offset used at the input, necessitating relatively complex level shifting (as well as logic) to control the output of the multivalued gate.

This difficulty can be overcome if the threshold offset components are placed in the input lead of the comparator rather than the reference (source) lead which is shared by the output. This concept has been realized effectively by Russell [52] who introduced the all-NMOS circuit shown in Fig. 14 to implement the two-level detector required in ternary. All devices shown are NMOS, $T_2$, $T_4$, and $T_6$ being depletion devices and the remainder enhancement. Implementation of the lower threshold is conventional, using $T_5$ and $T_6$, where the threshold of $T_5$ is used directly. The upper threshold, also referenced to the negative supply rail, is formed by the sum of the thresholds of $T_1$ and $T_3$, $T_1$ acting as a follower biassed by $T_2$, and $T_3$ as a switch with $T_4$ as load. This idea is relatively general with additional thresholds available, as shown in Fig. 15, where, through the introduction of diode-connected device

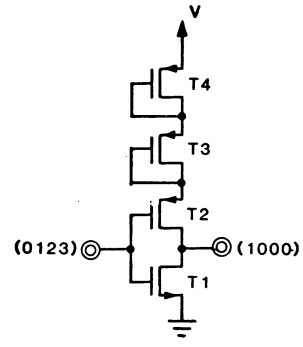



Fig. 13. A quaternary CMOS low threshold detector.

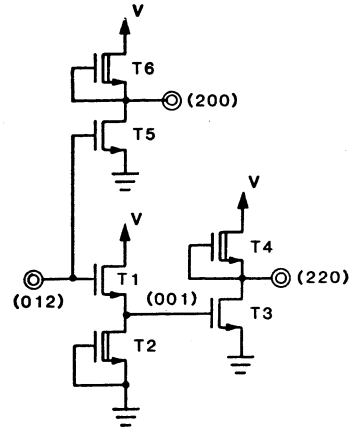



Fig. 14. A ternary NMOS high and low threshold detector.

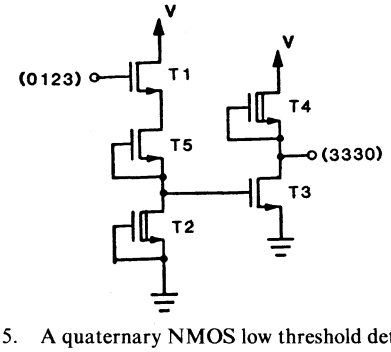



Fig. 15. A quaternary NMOS low threshold detector.

$T_5$, the switching threshold is raised to 3 device thresholds above the reference. Thus, this circuit is suitable for the upper threshold of a base 4 circuit, distinguishing between the two upper levels (2 and 3).

Such circuitry is suited to the addition of truly multivalued input signal conditioning. Fig. 16 depicts a quantizing max gate in which additional logic is provided by simply parallelling transistors $T_1$ and $T_5$. Incidentally, the output circuit is an interesting example of creating multivalued output levels through "diode" stacking [15]. Here, the lower level (0) is produced at the output when $T_7$ is on, the upper (2) when $T_7$ is off and $T_9$ is off, and the middle (1) when $T_7$ is off and $T_9$ is on. In the latter state, $T_9$ operates as an ideal switch allowing $T_8$ to be connected as a diode supplied with current from $T_{10}$.

With advances in technology, other possibilities exist. These include, for example, using ion implantation [15] to obtain devices having different thresholds. For example, if thresholds of 1 and of 2 were available, the circuit of Fig. 14 could be

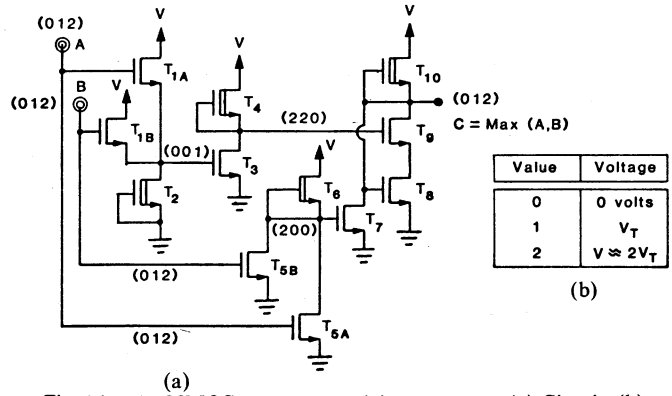



Fig. 16. An NMOS ternary quantizing max gate. (a) Circuit. (b) Equivalence table.

simplified, eliminating transistors $T_1$ and $T_2$ by using a threshold of 2 for device $T_3$ ($T_{3A}$ and $T_{3B}$ of the equivalent max gate).

The idea of variable threshold devices has been identified in the context of GaAs MESFET's by several authors [72], [73]. Here the complexities of GaAs at present limit reliable processing to metal-semiconductor junctions which provide depletion mode junction FET's and diodes. The circuits are potentially very fast, certainly in the subnanosecond range for binary applications. Tront [72] has suggested a family of circuits of which Fig. 17 illustrates various principles. It depicts a diammetrical inverter circuit which can be easily converted to a $\overline{\min}$ of 2 variables by parallelling $T_1$–$T_4$ with a set of similar devices having gates connected to a second input. Note that a negative logic notation is being used, 0 being most positive and 4 being most negative. The thresholds are indicated in logic value terms near each transistor, $T_4$ requiring the largest negative voltage for cutoff. Transistors $T_9$ and $T_{11}$ operate as current sources to bias diodes and the follower $T_{10}$. Diodes $D_1$–$D_4$ form a positive max on outputs generated by $T_5$–$T_8$. The latter transistors, which are smaller than the switches, are connected in a current limited mode when their corresponding switch closes, creating a "4 (low)" level. When the switch opens, the arrangement connects a logic level supply to the corresponding diode. The lowest level voltage supply needed is "3." It is apparent that the need for these signal reference supplies complicates the use of these circuits. However, they can be avoided using diode strings.

Such a circuit by Smith [68] is shown in Fig. 18. Here the transistor numbers and properties correspond to those in Fig. 17. In each case if $T_{11}$ and $T_{10}$ have identical $I_{DSS}$, the follower produces no offset, and the diode string $D_5$–$D_9$ serves to lower the output voltage to the range where the thresholds of FET's $T_1$–$T_4$ are distinguished.

The use of separate device thresholds, while simplifying the circuit topology, does complicate device processing by requiring locally controlled doping, unfortunately a nongeometric process. An alternative has been identified by Upadhyayula [73] which is based only upon geometric ratioing; it is simply to control the relative sizes of the switch and load channels. In the limit, either all switches or all load widths might be fixed, while the other width is used to establish the multivalued threshold. This idea can be applied directly to the circuit of Fig. 17 in which case the loads $T_5$–$T_8$ should be equal

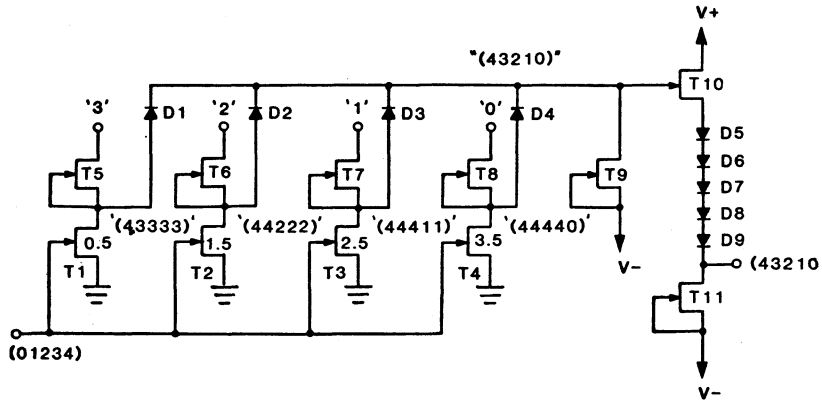



Fig. 17. A MESFET diametrical inverter for radix 5.

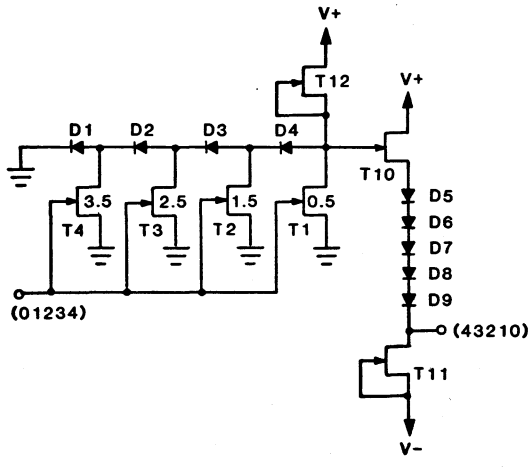



Fig. 18. A simpler MESFET inverter for radix 5.

(with $T_9$ smaller). Most recently, Durand [15] has utilized the idea in developing a family of relatively economic highspeed ternary circuits.

It is interesting to note that while the geometric ratioed switch and load idea is well suited to short channel GaAS MESFET's, since they exhibit a nearly linear relation between drain saturation current and gate to source voltage, it can be applied more generally. Thus, it appears to provide an attractive possibility for NMOS designs and indeed has been used in binary NMOS circuits. The most renowned example of its use in MVL is by Stark [69] in the Intel 8087 and 432 quaternary ROM designs. Here one of 4 NMOS devices is placed at the storage node, providing a radix 4 digit line signal, with a reduction by 2 of digit lines and for the entire memory of 30 percent or so.

### *B. Output Circuits*

Output quantization in voltage mode circuits requires a set of standardized values which may be: 1) externally supplied; 2) created from available supply rails by means of voltage divider(s); or 3) created from one (reference) supply rail and a constant current source supplying a stack of identical two-terminal devices.

The output may be formed by several means: 1) directly through 1 of $R$ switch selection of $R$ supplied values, or 2) directly through 1 of $(R-1)$ switch selection with one value by default through a resistor, or 3) indirectly through switch modification of the voltage divider or voltage stack.

Altogether, there are 5 distinct approaches to output quantization, and of course a larger number of potential combinations. Some of these are illustrated for radix 3 in Fig. 19(a)-(d).

Because of a need only for one additional level, ternary designs provide a rich variety [40] of examples of these approaches. For instance, in balanced ternary, using ground and a positive and negative supply, the cost of a third supply rail (ground) does not seem high, particularly when the middle state is established by a resistor to ground [Fig. 19(e)], as demonstrated by Kaniel [41] and Smith [67] in CMOS designs. Alternatively, Koanantakool [47] and Huertas [39] utilize a third CMOS switch to produce a low-impedance middle state (a).

The use of only two rails for ternary designs is also relatively straightforward. Mouftah's design (Fig. 11) using a resistive voltage divider (c) controlled by 2 CMOS switches is a classic example. Crist [4] in a TTL-based scheme uses a high impedance, open condition for the mid state ($b$ with $r = \infty$).

Etiemble [24] was first to use what in effect is a single rail radix 3 design using TTL-based circuitry in which the output levels are established by a switch-selected string of diodes (either 1 or 2) supplied with current (through a resistor) ($d$), ($e$). The advantage of this approach lies in the direct extension to higher radices. As illustrated for base 4 by Etiemble [26], Fig. 20 provides such an output stage in the context of a binary to quaternary converter. The IC's shown are TTL open-collector switches. The original design shown in (a) utilizes sep-

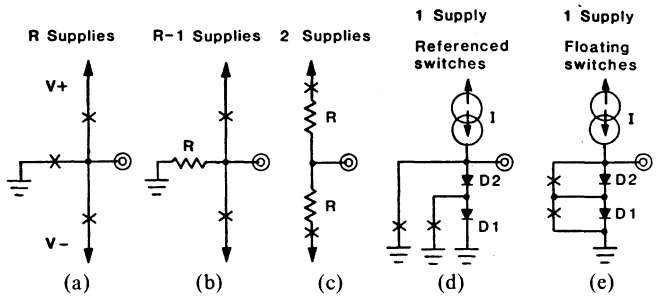



Fig. 19. Output switching schemes where switches are shown as $x$. Exactly one is closed in (a); at most one is closed in (b) and (d); at least one is closed in (c); any combination is allowed in (e).

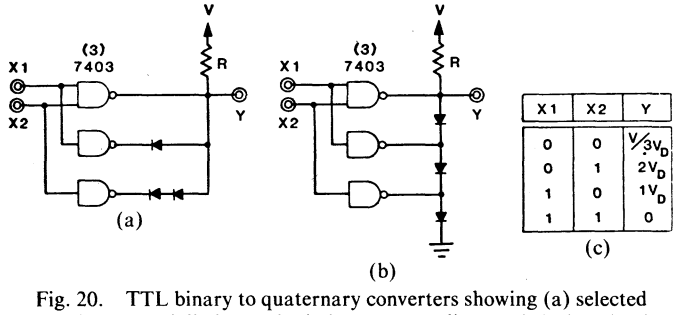



Fig. 20. TTL binary to quaternary converters showing (a) selected diodes, (b) stacked diodes, and (c) the corresponding truth (voltage) table.

arate diodes rather than a single string as illustrated in (b). The latter approach regulates each of the 4 levels one diode drop apart. For larger signal level spacing, two diodes can be used in place of each one shown.

The idea of a switched reference chain is easily extended to NMOS designs. Here, as shown for a binary to quaternary converter in Fig. 21, a depletion device (with the bar) serves as a current source, while enhancement devices are used both as low-resistance zero-offset switches and (with feedback from drain to gate) as offset diodes. Variations on this idea are discussed by McCluskey [52] and detailed by Russell [15]. Ternary versions of this type of circuit have been tested and higher base versions simulated.

## IX. Applications of Multiple-Valued Logic

### A. Augmentation of Binary Systems

The concept of using multivalued logic, particularly ternary, in a binary mode as a means to improve reliability, is a fairly old one [27], [37]. One general idea has been to use the third state, often the central one, as a means of signaling faulty operation. Another possibility is to apply the outer two values of a 4-valued system (or these and the innermost of a 5-valued system) to the detection of binary faults. More recently, in a generalization of these ideas. Druzeta and Vranesic [19] describe the possibility of extending a radix $R$ system, implemented by $MT(R)$ multithreshold current mode elements, to radix $(R+1)$ or $(R+2)$ for fault detection purposes, in which one or both of the edge states (0 or $(R-1)$ in radix $R$) are used in off-line testing.

For example, all single and multiple faults of a somewhat more general type, the s-a-$\overline{0}$ (stuck at anything but zero) and s-a-$\overline{R-1}$ (stuck at anything but $R-1$), can be tested with two simple input vectors if an $R$ value system is augmented by two additional states. While the application of the complete

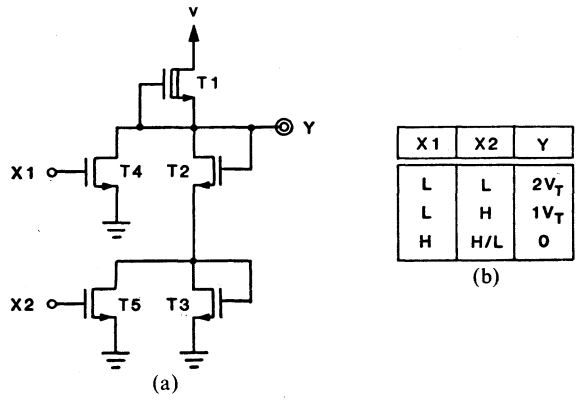



Fig. 21. An NMOS binary to ternary converter. (a) Circuit. (b) Truth (voltage) table.

scheme to reliable binary, requiring quaternary logic, brings large overhead, the testability is greatly enhanced. Even when the reduced $(R+1)$ scheme (i.e., ternary) is applied to a binary situation, examples indicate a 40 percent reduction in the number of tests required for multiple fault detection.

Etiemble [27], [28] has used $I^2L$ to implement a totally self-checking (TSC) comparator with two-wire complement binary outputs (1-of-2 coded), and demonstrated it to be useful in the role of TSC checker for a variety of binary and multivalued error-detecting codes including $m$ of $n$, Berger, and residue codes. In another paper, Etiemble [30] introduced the idea of a TTL-based radix-3 TSC circuit which can interface to 1-of-2 coded binary-paired lines, and which provides a self-checking single-wire logic system on which failure occurrences can be propagated and combined.

Another direction is represented in a recent paper by Wojcik [82] on the use of radix three in asynchronous, speed-independent combinatorial and sequential circuit design. Here the outside levels are used for binary operations while the middle level is used as a control to signal start and completion of information processing, and thus as a spacer in module interconnection. The resulting system can be designed on the basis of standard binary techniques.

### B. Memory

*1) Multiflops and Registers:* As demonstrated here and elsewhere [76], [77] single multivalued storage elements are relatively easily constructed and controlled [29]. In general, they consist of a feedback connection closed around a noninverting value-restoring element formed directly or as a cascade of other gates. One particularly convenient approach to the latter consists of a pair of (diametrical) inverters connected in a loop. Gating of either a single element or multielement loop can be done by means of one or two analog transmission gates feeding one of the connections and controlled by binary signals.

Another approach with the 2 inverter design shown in Fig. 22 involves connecting a 2 input max gate in each of the two connections. The free input of each max is connected to a separate 2 input min gate. One input of each min is connected to serve as a control supplied by a binary signal ranging from 0 to $(R-1)$. The second input of one min connects to the input signal and the second input of the other min connects to the

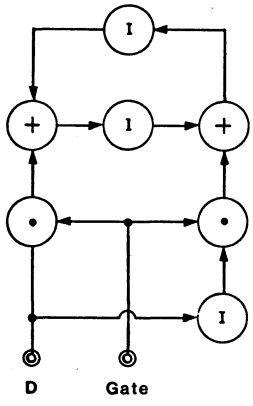



Fig. 22. A data type multiflop using diametrical inverters and min/max gating.

complement of the input. When the gate signal (connected to both min's) is held low, the min outputs remain low. Accordingly, the loop retains its previous state coupled through the max gate. Now when the control gate rises to $(R-1)$, the min outputs take on the values of the signal and its complement which are fed to the max gates. Whichever the previous stored state, the lower link in the multiflop is raised while at the same time the other link lowers, until the state of each link is the same as that from the gated mins, establishing a new state. When the control goes to zero, the gated state is held.

It is apparent, in analogy to traditional binary structures, that on basis of the gated multiflops just described, the usual (binary) repertoire of double-rank storage elements can be duplicated and that registers, shift registers, and counters [55], [56], [6] are relatively straightforward if one is willing to accept binary control.

*2) RAM:* It is apparent also that multiflops of the general structure shown in Fig. 4 or Fig. 22 can be combined in arrays with, for example, the input min gates provided with an additional input for two-dimensional selection, and the $D$ line available on a bus. However, the economics of the static storage element itself are not promising.

The lowest cost dynamic memory cell for multivalued charge storage is a capacitor. Certainly, it is this choice which underlies the present dramatic success of binary dynamic memory, where gating overhead has also been reduced to that of only a single MOSFET per cell. While this same access method, in which the selection transistor acts as (an analog) transmission gate, works also for multiple values, problems arise in the change to high-value sensing circuitry. In addition to requiring larger signal levels with increased power and reduced speed, there remains the problem of regenerating multiple-valued signals. It appears then that the overhead of sensing will be the limiting factor in multivalued RAM.

*3) Serial Memory:* Multivalued serial memory using CCD's [83] has been demonstrated from which block-random-access memory systems can be produced. Production devices having quaternary storage internally appear to be available [83], [70], while laboratory units up to radix 32 have been reported [44]. In a serial capacitive store such as CCD-the relative balance of cost of storage cells and of signal regeneration are such that multivalued storage is quite cost effective. While the choice of radix as a power of two makes the interface to conventional systems quite easy, there remains the possibility that increased reliability, testability, and error detection can be obtained economically through the use of additional states.

*4) ROM:* It is the area of ROM design that multivalued logic has made significant progress using techniques that may be extendible to the design of PLA's as well. In an early paper, Dao [13] suggested that the multiple collectors of MVI$^2$L could be applied to ROM design. Subsequently, Silio *et al.* [64] studied the potential application of this possibility to the control store of a PDP 9, demonstrating up to 50 percent saving in devices.

The Intel 8087 numeric coprocessor, announced in 1980, includes a quaternary ROM [60]. Subsequently, Stark [69] described this and a similar ROM with an equivalent capacity of 30 kbits used in the Intel 432 32-bit processor. In these designs each NMOS device can have one of four channel widths providing from 0–3 units of channel current. The resulting array, whose size is determined largely by the number of digit lines, is reduced by a factor of two over the standard binary design. On a per bit basis the area of thc required quaternary sensing circuitry is little greater than that required for sensing in the standard binary design. The overall area reduction in the ROM is about 30 percent, resulting in 8087 case in an important 8 percent reduction in die area, with a corresponding significant increase in die-per-wafer yield. An analysis by Stark on the basis of this experience indicates that a 3-bit per cell ROM shows promise, particularly for applications in which access time may be increased to allow parts of the sensing system to be time-shared and/or value-shared.

### C. Communications, Signaling

The topic of multivalued signaling is a very large one ranging from the straightforward interconnection between circuits and even gates, to the sophisticated realm of communications channel coding. Since enough has been said about local connection within gates and the somewhat more global interconnection of gates within IC's, the discussion will now focus on topics relevant to systems interconnection at modest distances.

Point-to-point link communications at intermediate distances (to 1 km) is an appropriate domain in which to apply multivalued signaling. Although this can be argued from many points of view, one supporting fact is the existence of the 20 mA current-loop industrial analog-signaling standard. Accordingly, current mode signaling on point-to-point links may be seen to be relatively straightforward. Such a link [20], using quaternary I$^2$L, is illustrated in Fig. 23.

If ground voltage offset is too great a problem, differential techniques are relatively easily included using ECL-based technologies. As noted by Etiemble [31], an existing commercial circuit, the Motorola ECL MC10194 dual line driver/receiver, uses ternary signaling to allow full duplex (simultaneous two-way) operation on a high-speed multiport single line bus. On the bus, communication is possible either between any two devices using 3-valued signaling, or from one to all others in a binary mode. A similar idea is described by Ross [63]. Etiemble [31] also describes the development of quaternary ECL IC's aimed at reducing the wiring cost be-

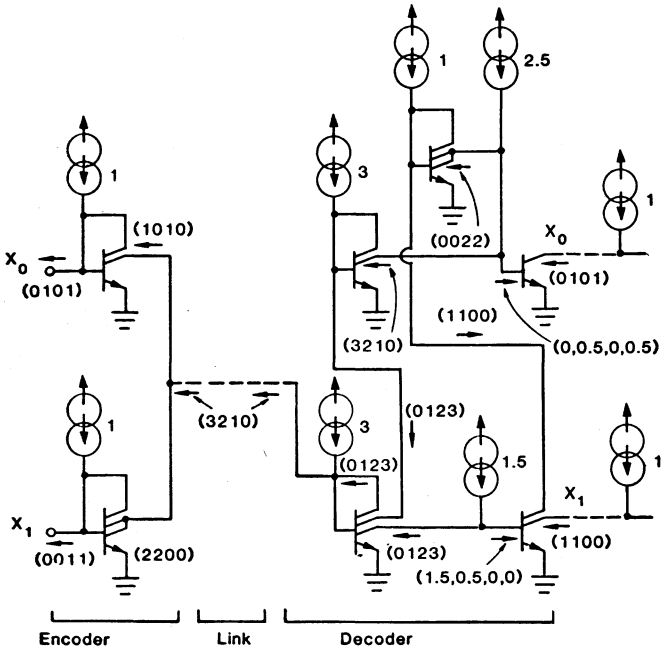



Fig. 23. Binary-to-binary coupler using a multivalued link.

tween multiprocessors and multimemories. The chips act as coders and decoders to interface between binary system components via a quaternary voltage-mode link using circuits which resemble that in Fig. 10, with voltage mode conversion at the front and rear.

On a more prosaic level, as D/A and A/D chips rise in speed and fall in cost, it is apparent that we are now at the stage where low-speed multivalued links are possible at low cost for relatively quiet environments [63]. With a current mode output driver having suitable compliance, even noisy environments can be tolerated.

While current is appropriate for direct link connections and even well suited to switched multiple source busing, it is unfortunately not easily applied if more than one isolated sink is required. All available solutions to this problem lead directly to the recognition of the need for conversion to voltage on a tapped bus [80], [81]. While the drivers could be (and perhaps should be) current devices, there is no way to share line current. Thus, the receivers must be voltage-value-sensitive and equipped with multiple voltage threshold devices. Another possibility is of course to voltage-to-current convert at each receiving sink tap by means of a high impedance receiving amplifier. The current so provided may be replicated in an MVI$^2$L mirror to supply appropriate current thresholding devices for conversion to binary if desired. Such a receiver is not complex, with the major part [20] (in radix 4) resembling the right side of Fig. 23. Furthermore, current drivers are extremely straightforward, consisting simply of weighted current sources switched onto the line. To allow multiple devices to act one at a time, they must be all capable of being disabled in the manner of a tristate gate in binary. In partial correspondence to the tristate idea in binary, in base $R$, a total of $(R + 1)$ values of current including zero may be useful in detecting that the bus is busy. However, this feature is not essential.

### D. Arithmetic

As has been observed earlier in various ways, one of the more obvious applications of multivalued logic is to arithmetic processing [75], [50]. Examples of high radix adders are commonplace [10], [33]. Studies of more complex designs are available. For example Hamacher and Vranesic [35] have demonstrated that for the multiplication of 24-bit numbers, ternary balanced coding with $MT(R)$ functions reduces the cost to $\frac{1}{3}$ or less, and gate input count to $\frac{1}{5}$ or less. However, for the particular implementation a doubling in time taken is estimated. Newton [58] has demonstrated a divider array in the same technology. Singh and Armstrong [65] have provided a quaternary I$^2$L design of a 32-bit multiplier which shows a marked cost and speed improvement over the base 2 design. Dao *et al.* [14] have demonstrated the advantage of an odd-valued radix in a complex number multiplier suitable for applications such as the discrete Fourier transform.

Thus, in view of both the demonstrated advantages of balanced ternary and the technological feasibility of ternary I$^2$L, it would seem that one should soon expect developments in arithmetic processor chips which exploit this combination internally.

### E. Signal Processing

Relatively recently, a great deal of work has been reported on a variety of multivalued signal processing applications including correlation [9], Fourier transformation [14], and digital filtering [44].

Of the technologies applied, the one which shows the greatest potential for commercialization at modest speeds is CCD [43], [45], which with integrated serial memory and logic adapts well to pipelined applications. In retrospect it is fitting that these devices for which both analog and binary operating modes are natural, have provided one of the earliest large-scale multivalued applications.

### F. Support Chips

A potential application for multivalued signaling is in the control of distributed devices where cost of wiring is of some concern. While in an ideal world one could conceive of the use of multivalued ports in future processor designs, it is possible now to use available relatively-high-speed D/A chips to convert processor-local binary to a distributable multivalued voltage.

Although existing A/D [63] chips can be used as receivers, the combination of low cost at high speed is at present limited. Moreover, the function performed by an analog-to-binary converter is not precisely what is needed.

An interesting and flexible alternative would be provided by the fabrication, on an IC chip, of an 8-way analog multiplexer with eight-value voltage control. Obviously, such a device could be used to serve as one pole of many in a local or distributed multiple-pole analog switch, where the overhead of the D/A (actually D/MV) converter is spread over many poles. However, if the cost of the D/A is seen to be a problem, a 3-bit converter using a combination of weighted resistors and a suitable binary logic family (e.g., CMOS) is probably adequate.

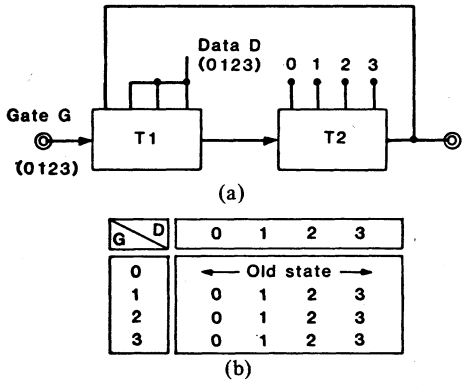



Fig. 24. Two $T$ gates used as a gated multiflop: $T_1$ under control of $G$ acts as two transmission gates, only one of which is closed.

However, there are more attractive digital possibilities. It is apparent that the new device could be used as a one of 8 decoder for address selection of distributed bus-driven devices, or to control up to 8 devices in a single location, or various combinations of these extremes. Note that for situations where the need for outputs does not exceed 4, and a need to raise noise margins is found, 4 levels can be used, the remaining 4 being reserved as guard bands, with a possible application to system noise-level alarming.

Finally, of interest to the multivalued community is the fact that such a device, which incorporates the selection function $T(x_1, x_2 \cdots x_n, q)$, provides a functionally complete building block. Note for example, as Fig. 24 demonstrates, that with a set of reference supplies [37] (or voltage divider), restoring and storage elements are easily created.

## X. Conclusion

It has been the intent of this review to place in perspective the opportunities offered by the extension of digital logic to multiple values. That some commercial products already enjoy the benefits of MVL is seen as a first step to recognition of the broader role of MVL in the economics of digital system design and manufacture in the VLSI age.

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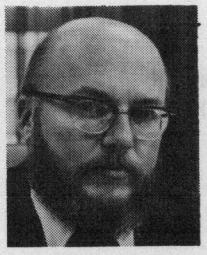

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