Laboratory Exercise 1

Building Circuits using 7400-Series Chips

The purpose of this lab is to illustrate the process of building logic circuits by using chips that contain individual logic gates. Although circuits are no longer built in this way in the industry, it is useful to see how the chips are connected together to understand the basic electrical connections.

Below is a description of the different pieces of equipment you will use: the protoboard, logic probe, wire strippers and digital switch/light board. **BEFORE the lab**, do the preparation. During your lab, read through these sections and do the actions.

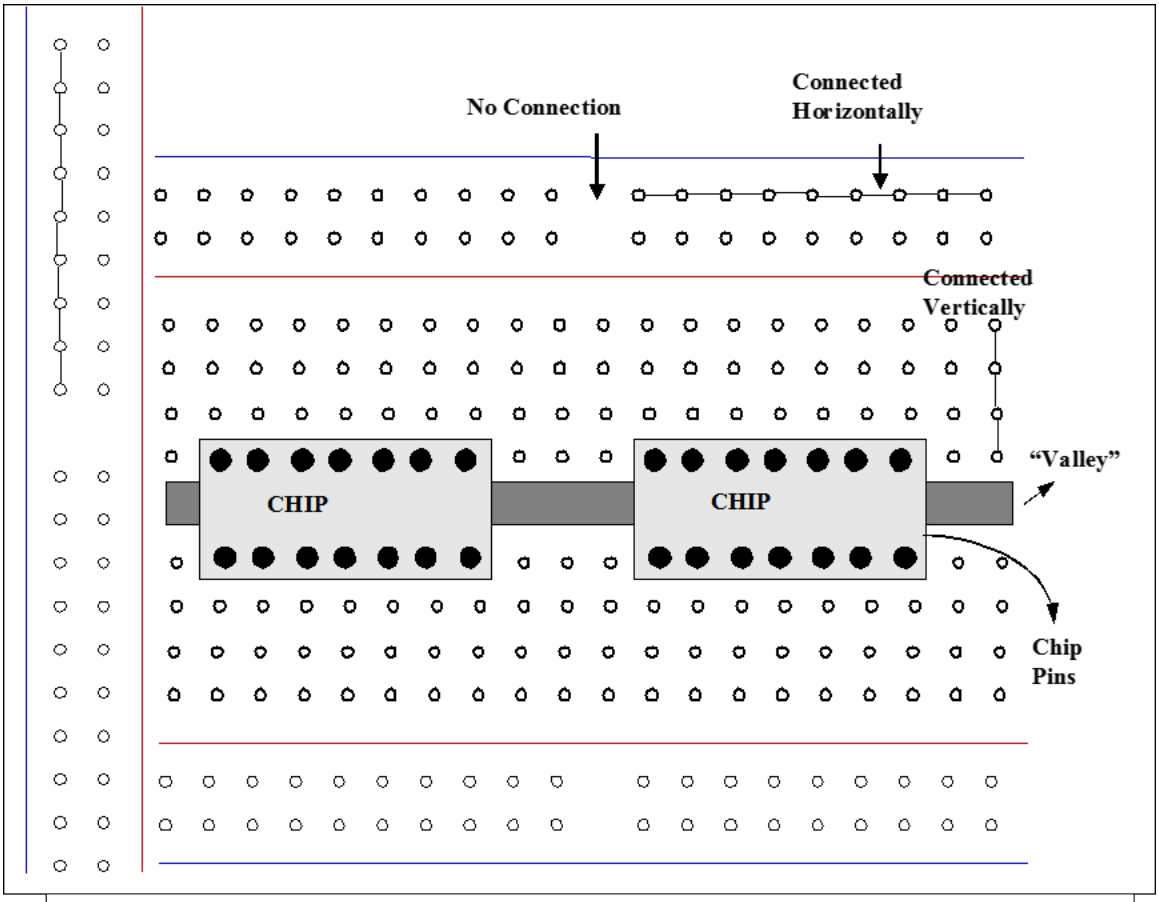


Figure 1 - Picture of the Protoboard

Protoboard:

The protoboard (breadboard) is for holding and connecting chips. As illustrated in Figure 1, chips are inserted across the middle valley in the protoboard. The set of holes in a vertical line above the valley are connected

electrically, as are the vertically aligned holes below the valley. So, each pin of the chip in the board is connected to the holes above (or below) the pin. To make a connection to a specific pin, you need only make connections between the holes by plugging the bare end of a wire into the holes above or below the pins.

In the figure the horizontal lines at the top and bottom of the board delineate holes that are connected horizontally; note that the space in the middle indicates a disconnection. The horizontally-connected holes at the top and the vertically connected holes at the side are usually connected to the power and ground provided by the external connector. The power and ground of the chips are then connected to these strips of holes. The first thing you should do in the lab is connect power and ground to these horizontal and vertical strips.

Digital Switch Board:

The digital switch board provides switches that have digital output **(5V = logic 1, 0V = logic 0)** and lights that can be driven by logic signals (logic 1 turns a light on, logic 0 turns it off). Test the board by connecting the switches to the lights. The board also provides a clock, which can have its frequency varied by inserting different capacitors into the holes next to it, and a seven-segment display.

Logic Probe:

The logic probe is used for measuring the logic values of signals on the board. Be sure that it has power attached, to the correct terminals. To test the probe, touch it to the +5V on the protoboard and ground, to ensure that it correctly indicates the values high (1) and low (0) respectively.

Wire Strippers and Chip Puller:

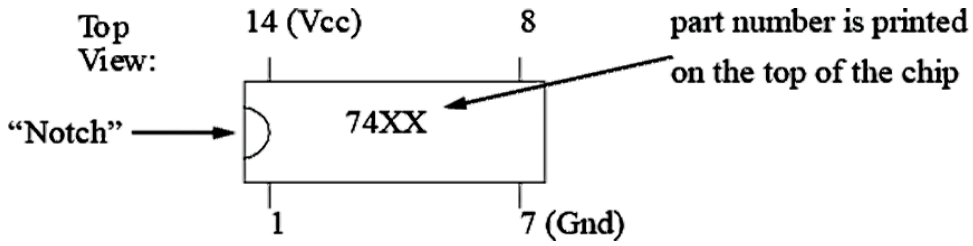
The wire strippers are attached to each workstation to make sure they dont get lost. If you havent ever stripped a wire, try it!

The chip puller should always be used to remove chips from the protoboard. Doing it with your fingers will bend the pins and ultimately break them, so dont!

7400-series Chip Packages:

The chips that you will use in this lab are Small Scale Integration (SSI - meaning theres not much logic on a single chip) 7400 series. Depending on exactly which chip you end up using in the lab you may have to set the logic probe to one of two settings: TTL or CMOS. This setting depends on the type of technology used for the transistors in the chips.

All of the chips you will use are Dual In-line Packages or DIPs. Most of the packages are 14 pins, and the pins are numbered from looking at the chip from the top: Below the notch is pin 1 to pin 7, and above the notch is pin 14 down to 8.



NOTE: Pin 14 must always be connected to VCC (+5V) and pin 7 to ground (0V).

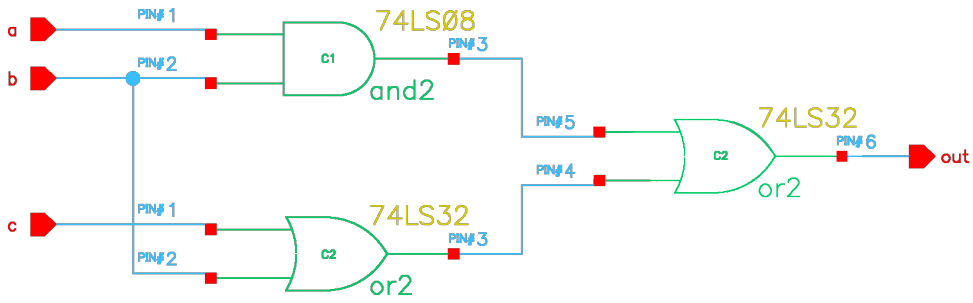
Preparation Before the Lab

Design all of the circuits in both Part I and II using **only 74LS04 (NOT), 74LS08 (AND) and 74LS32 (OR) series chips**, as given on the attached sheets. Choose the actual pin numbers of the chips that you will use when you build your circuit and show them on your circuit diagram - this will make the construction of your circuit easier.

For example, to implement the following function:

$$\mathbf{f} = ab + (c + b)$$

The schematic will look like this:



CHIPS USED:
C1 – 74LS08
C2 – 74LS32

CONNECTED TO ALL CHIPS:
PIN# 7 – GND
PIN# 14 – VDD

Note that you do not need to draw the entire chip; you only need to label which chip you used and which ~~port~~ number on the chip you used. Each chip has a unique label, C1 and C2 in this case, and there is a legend to say what type of chip. This will be handy when you have larger circuits where you will have several chips of the same type. We can see that the AND gate (C1) uses one **74LS08** chip using pins 1 to 3 and one OR gate (C2) **74LS32** chip using pins 1 to 6. The power and ground connections are shown separately.

In each case, show all of the steps required to go from the specification given below, to the final circuit, including: assigning variable names to inputs and outputs, deriving a truth table, the logic function, and then a schematic picture of the final circuit, with pin numbers and chip types.

Important: You are allowed to use only the following packages (see sheet attached): 74LS04 (NOT gates), 74LS08 (AND gates) and 74LS32 (OR gates).

Part I

The multiplexer is a device which selects one of multiple inputs to be outputted. The following boolean function is a 2 to 1 multiplexer.

$$\mathbf{f} = xs' + ys$$

As we can see, when the select signal 's' is 0, the signal 'x' is shown at the output. However, then 's' is a 1, the 'y' signal will show at the output. This is an extremely useful circuit with multiple applications such as in a datapath of a CPU which you will be implementing a part of in the future labs.

Perform the following steps.

1. Draw the 2 to 1 multiplexer design using the gates specified above. Indicate pin numbers on the chips. (You do not need to draw the entire chip, but you must specify which chip was used for which gate and which pins the inputs and outputs are connected to) Show this design to your TA as part of your prelab to verify that the design is correct.
2. Write out the truth table for the design and show it to the TA as another part of the prelab.
3. Wire your design on the protoboard and demonstrate the functionality to the TA. Your results should match your truth table from the prelab.
4. Is there a cheaper implementation for your design? (using less chips)

Part II

For following random boolean function given, provide the gate level implementation for the following expression:

$$\mathbf{f} = (a + b)' + cd'$$

Perform the following steps.

1. Draw the function shown above using the gates specified in the lab preparation. Indicate pin numbers on the chips. (You do not need to draw the entire chip, but you must specify which chip was used for which gate and which pins the inputs and outputs are connected to) Show this design to your TA as part of your prelab to verify that the design is correct.
2. Write out the truth table for the design and show it to the TA as another part of the prelab.
3. Wire your design on the protoboard and demonstrate the functionality to the TA. Your results should match your truth table from the prelab.
4. Is there a cheaper implementation for your design? (using less chips)

Part III

In this section, you will start on your first Quartus II project using the schematic builder. You are to design Parts I and II and compare it with the truth table from your prelab.

Perform the following steps.

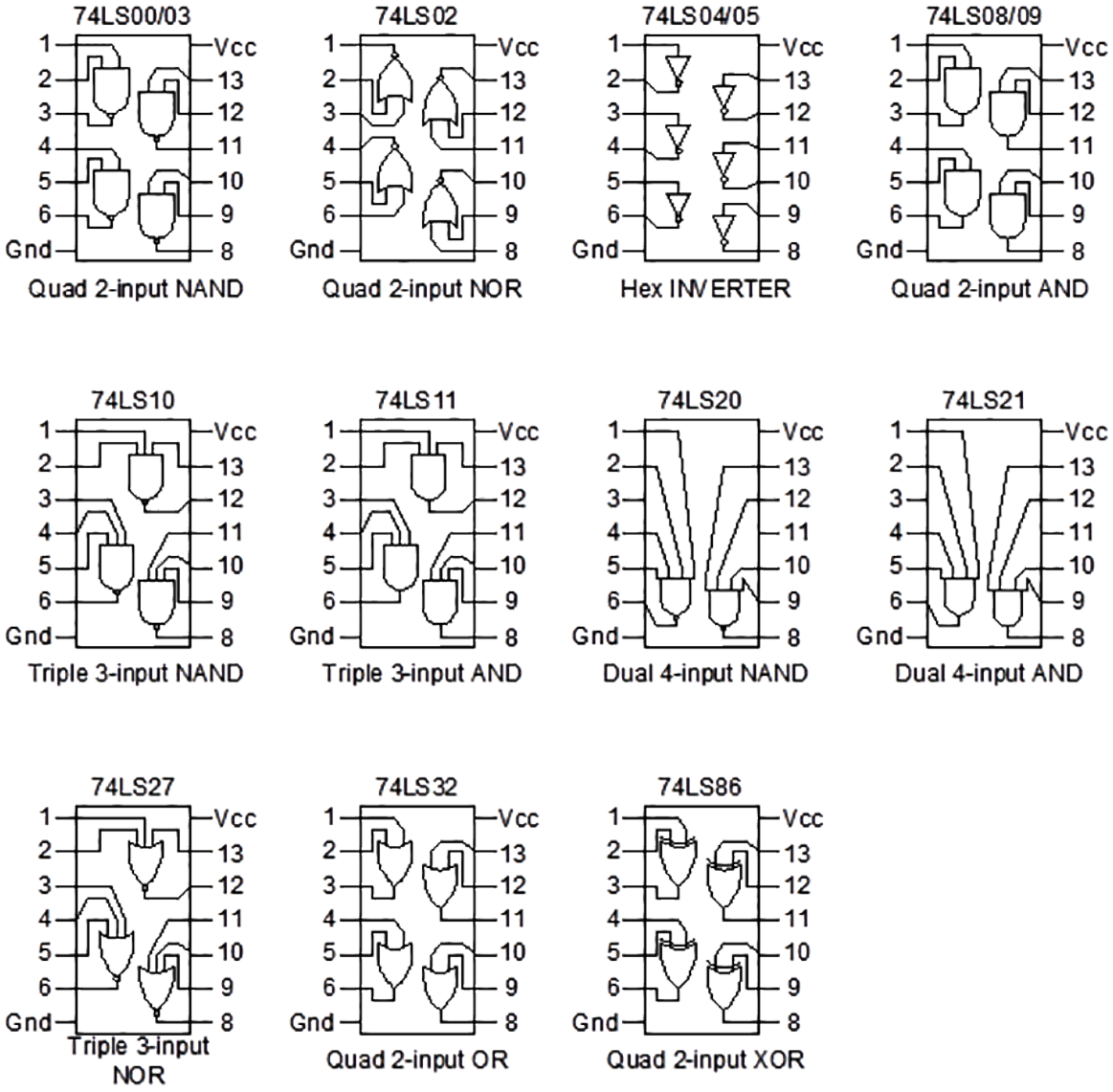
1. Open Quartus II and go to File > New... and select New Quartus II Project.
2. Click Next and under **Directory, Name, Top-Level Entity** select your working directory and type the name of your project. The top-level design will automatically fill out to be the same name as your project.
3. Click Next until you reach **Family & Device Settings** and select the chip 5CSEMA5F31C6 under Available Devices and then click Finish.
4. Click File > New... again and select Block Diagram/Schematic File. This should automatically open a schematic view window
5. To place an object click on Symbol Tool (shown as an AND gate) and under primitives > logic, you can find all of the gates you need.

6. To connect the devices together, use the Orthogonal Node Tool (shown as a thin 90 degree corner).
7. The inputs and outputs are set by the drop down Pin Tool. (Double click on the pins to rename them).
8. Before naming the pins, click on Assignments > Import Assignments... and import the *DE1_SoC.qsf* provided by your instructor.
9. If you open Assignments > Pin Planner, you can see all the pin assignments connecting the assignment name (eg. SW_0) to pin number (eg. PIN_AB12).
10. Name the inputs of your design with SW_0, SW_1, ..., SW_9 and your output as $LEDR_0$.
11. Once you have completed your design, click Processing > Start Compilation.
12. When compilation is done, click Tools > Programmer and a window will appear.
13. Go to Hardware Setup and ensure Currently Selected Hardware is DE-SoC [USB-x] and close the window.
14. Click Auto Detect and select *5CSEMA5* and click OK.
15. Double click <*none*> for device *5CSEMA5* and load SOF file (usually under folder "output_files") and device will change to *5CSEMA5F31*.
16. Ensure Program/Configure for device "*5CSEMA5F31* is checked and click Start.
17. Verify that your design is correct by matching it to the truth table from your prelab.
18. Perform instructions 1 to 17 for your design from Parts I and II.

Pin-Out Information for 7400-series Chips and Digital Board

Here are the Pin-out numbers and schematics for all of the chips used in Lab 1:

Pin-out of Selected TTL Chips



Here is the pin out connections for the header on the digital switch board:

Digital Board Header Pin Assignment					
Pin#	**Description**			**Description**	**Pin#**
1	Switch #1	o	o	Switch #2	2
3	Switch #3	o	o	Switch #4	4
5	Switch #5	o	o	Switch #6	6
7	Switch #7	o	o	Switch #8	8
9	Ground	o	o	NC	10
11	Ground	o	o	NC	12
13	Ground	o	o	NC	14
15	Ground	o	o	NC	16
17	LED #1	o	o	LED #2	18
19	LED #3	o	o	LED #4	20
21	LED #5	o	o	LED #6	22
23	LED #7	o	o	LED #8	24
25	Ground	o	o	NC	26
27	Ground	o	o	NC	28
29	Ground	o	o	NC	30
31	Ground	o	o	NC	32
33	Clock	o	o	NC	34
35	NC	o	o	NC	36
37	NC	o	o	Pulse Button	38
39	NC	o	o	NC	40