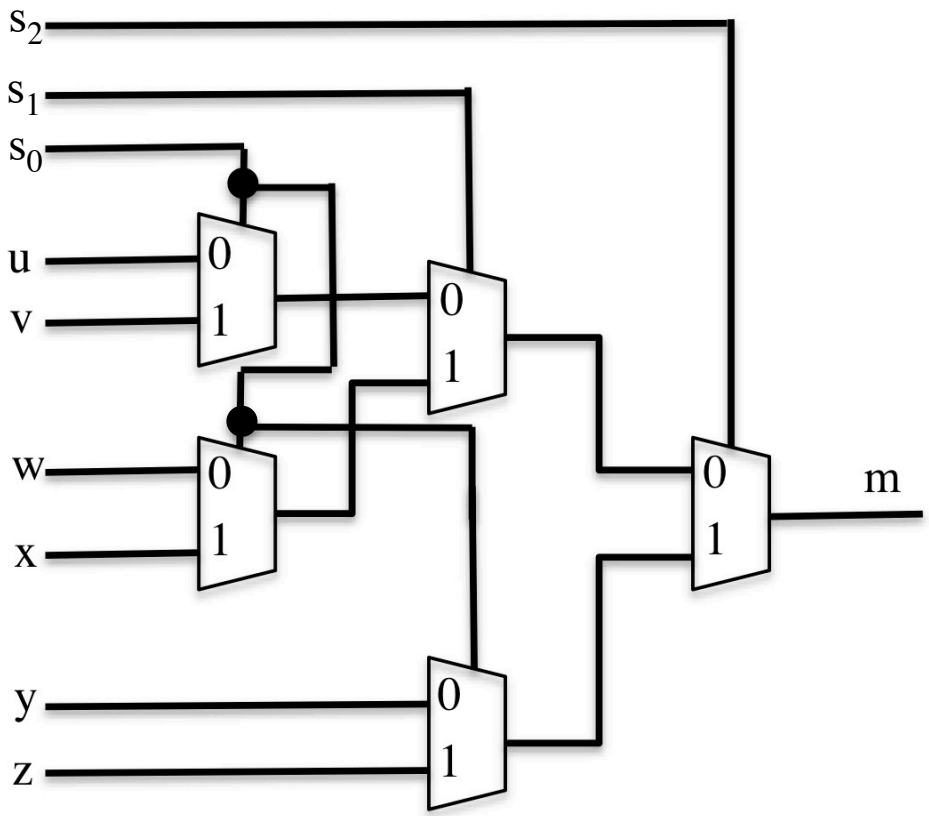
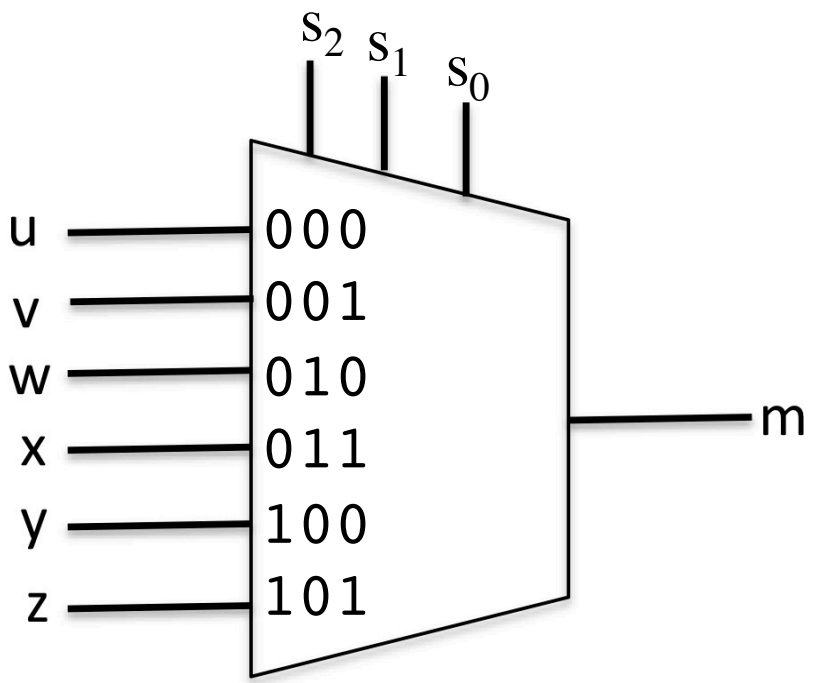


a) circuit

s_2	s_1	s_0	m
0	0	0	u
0	0	1	v
0	1	0	w
0	1	1	x
1	0	0	y
1	0	1	z
1	1	0	y
1	1	1	z

b) truth table



c) Symbol