Laboratory Exercise 3

Combinational Logic and Displays

This is an exercise in designing combinational circuits that can drive 7-segment displays, and perform a variety of different functions.

Preparation Before the Lab

You are required to complete Parts I to III of the lab by writing and testing Verilog code and compiling it with Quartus II. Show your Verilog, simulations and schematics for Parts I to III to the teaching assistants. You must simulate your circuit with ModelSim (using reasonable test vectors using the format shown in the previous lab).

In-lab Work

You are required to implement and test all of Parts I to III of the lab. You need to demonstrate both parts to the teaching assistants.

Part I

For this part of the lab, you will be learning how to use *always* blocks and *case* statements to design a 7 to 1 multiplexer.

```
always @(*)          // declare always block
begin
    case (select)    // start case statement
    begin
        0: ...       // case 0
        1: ...       // case 1
        2: ...       // case 2
        3: ...       // case 3
        4: ...       // case 4
        5: ...       // case 5
        6: ...       // case 6
        default: ... // default case
    end
end
```

An always block is trigger whenever there is a change in the sensitivity list. This list is denoted by the asterisks character in the above example. This means that whenever any input is changed, the following code will trigger. Similarly, we can change the asterisks to certain inputs to limit when this code is triggered.

The case statement is similar to that of C programming. It is important to have a default case to ensure that all cases are covered.

Using SW_{6-0} as the data inputs SW_{9-7} as the select signals. Display on $LEDR_0$ the output of a 7 to 1 multiplexer using the case statement shown above.

1. Create a new Quartus II project for your circuit.
2. Include your Verilog file for the circuit in your project. Use switch SW_{9-7} on the DE1-SoC board as the $select$ input, switches SW_{6-0} as the data inputs. Connect the output to $LEDR_0$.

3. Simulate your circuit with ModelSim for different values of $select$ and $data$. You must show these to the TA as part of your prelab.

4. Draw a schematic outlining the hierarchies you used and explain them to the TA as another part of your prelab.

5. Compile the project.

6. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit by toggling the switches and observing the LEDs.

Part II

Figure 2a shows a circuit for a *full adder*, which has the inputs a, b, and c_i, and produces the outputs s and c_o. Parts b and c of the figure show a circuit symbol and truth table for the full adder, which produces the two-bit binary sum $c_o s = a + b + c_i$. Figure 2d shows how four instances of this full adder module can be used to design a circuit that adds two four-bit numbers. This type of circuit is usually called a *ripple-carry* adder, because of the way that the carry signals are passed from one full adder to the next. Write Verilog code that implements this circuit, as described below.

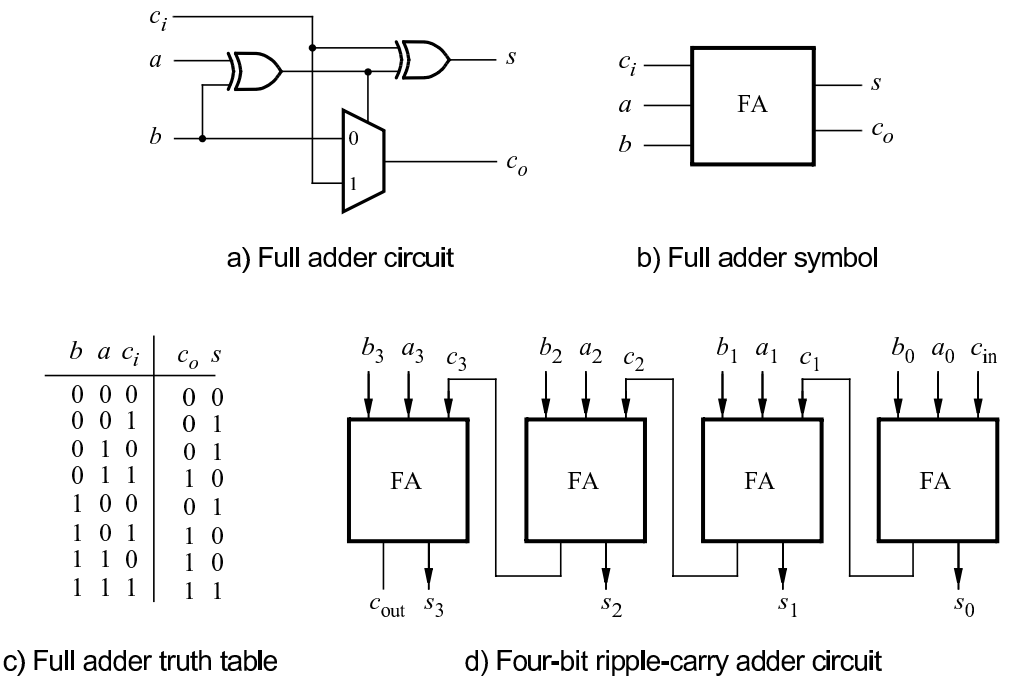

Figure 2. A ripple-carry adder circuit.

Perform the following steps.

1. Create a new Quartus II project for the adder circuit. Write a Verilog module for the full adder subcircuit and write a top-level Verilog module that instantiates four instances of this full adder.

2. Use switches SW_{7-4} and SW_{3-0} to represent the inputs A and B, respectively. Use SW_8 for the carry-in c_{in} of the adder. Connect the outputs of the adder, c_{out} and S, to the green lights $LEDR_9$ and $LEDR_{3:0}$ respectively.

3. Simulate your adder with ModelSim for intelligently chosen values of A and B and c_{in}. You must show these to the TA as part of your prelab.

4. Draw a schematic outlining the hierarchies you used and explain them to the TA as another part of your prelab.

5. Compile the project.

6. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit by toggling the switches and observing the LEDs.

Part III

Using Parts I and II from this lab and the HEX decoder from Lab 2 Part III, you will implement a simple Arithmetic Logic Unit (ALU). This unit can perform multiple operations such as addition, sign extension, etc. The output result of each operation is sent to the multiplexer. If selected by the multiplexer, the operation result will display at the output.

Shown in the case statement blow are the following operations for each case. The multiplexer has an 8 bit input and 8 bit output.

```
always @(*)          // declare always block
begin
   case (select)     // start case statement
   begin
      0: Addition using Part II of this Lab
      1: Addition using '+' operator
      2: Sign extend value B (SW[3:0]) to 8 bits
      3: Find if at least 1 of the 8 bits is 1 using a single OR operation
      4: Find it all of the 8 bits are 1 using a single AND operation
      5: Display the values on the switches
      default: ...   // default case
   end
end
```

Note that in this part of the lab, you will need to learn concatenation for the additions, sign extension, and reduction operations for ORing and ANDing multiple bits without typing ever single bit out.

Perform the following steps:

1. Create a new Quartus II project for your circuit.

2. Create a Verilog module for the simple ALU. Connect the A and B inputs to switches SW_{7-4} and SW_{3-0} respectively, and connect KEY_{2-0} for select signals. Display the outputs on $LEDR_{7-0}$; have *HEX0* and *HEX2* display output of A and B respectively and set *HEX1* and *HEX3* to 0. *HEX4* and *HEX5* should display the sum and carry out respectively.

3. Simulate your circuit with ModelSim for a variety of input settings, ensuring the output waveforms are correct. You must show this to the TA as part of your prelab.

4. Draw a schematic outlining the hierarchies you used and explain them to the TA as another part of your prelab.

5. Compile the project.

6. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit.