A Field-Programmable Mixed-Analog-Digital Array

Paul Chow†, Paul Chow‡, and P. Glenn Gulak

Department of Electrical and Computer Engineering
University of Toronto
Toronto, Ontario, Canada M5S 1A4

Abstract

A novel field-programmable mixed-analog-digital array (FPMA) is proposed, which contains a field-programmable analog array, a field-programmable digital array, and a mixed-signal interface. This device is intended to be used for the rapid implementation of mixed-signal circuits. The resource and architectural requirements for this array are determined by analyzing a set of sample circuits. The mixed-signal interface is constructed from converter blocks that contain configurable A/D and D/A converters, which gives some flexibility in the specification of the interface. A 1.2 µm CMOS prototype IC has been designed to demonstrate the feasibility of FPMA technology.

1 Introduction

The trend in VLSI towards single-chip systems leads to the integration of analog and digital functions on a single chip. The reduction in the number of chips leads to reductions in board space, interconnections, and most importantly, cost. Field-programmable devices are likely to follow the same trend due to the rapidly expanding market for mixed-analog-digital devices, which is growing at a faster rate than either analog or digital devices [1]. Currently, there are many commercial Field-Programmable Gate Arrays (FPGAs) available to implement digital circuits [2]. More recently, there has been research into the area of Field-Programmable Analog Arrays (FPAAs) [3][4]. However, there has been no attempt to combine these two technologies to produce a single Field-Programmable Mixed-analog-digital Array (FPMA).

Although large systems today consist mostly of digital logic, they must still interface with a largely analog world.

† Student.
‡ Professor.

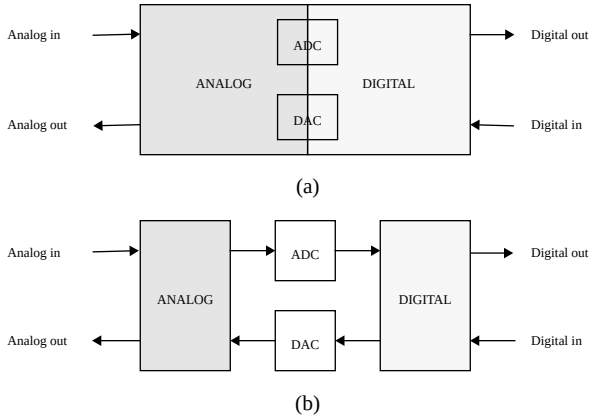


Fig. 1. Conceptual views of mixed-signal architectures: (a) array architecture with field-programmable resources capable of constructing data converter as required; (b) array architecture with dedicated data converters.

To build a single-chip system, these interfaces must be included on chip. Mixed-signal systems can be found in a wide variety of applications such as instrumentation, control, telecommunications, etc. Two conceptual views of an FPMA architecture are shown in Fig. 1. The first view, shown in Fig. 1(a), contains an analog array and a digital array with some interconnect. Any signal conversion that is required can be built from the resources available in the two arrays. An alternative view, shown in Fig. 1(b), provides dedicated data converters to perform signal conversions. The former view offers greater flexibility at the expense of a reduction in speed and an increase in area. To investigate the resource and architectural requirements of an FPMA, a prototype chip called MADAR[1], which includes a field-programmable analog array, a field-programmable lookup-table-based digital array, and configurable converter blocks (CCBs) has been designed and implemented according to the model of Fig. 1(b).

2 Resource and Architectural Requirements

To determine the architecture of an FPMA, it is important to first understand the requirements. Without any prior

1. **M**ixed-**A**nalog-**D**igital **A**rray that's **R**econfigurable. The word MADAR in Persian means circuit.

Circuit	Opamps	Lookup Tables	ADC	DAC	A-D interconnects	D-A interconnects
Sigma-delta ADC	3	14	-	-	1	1
Dual-slope ADC	2	10	-	-	1	3
PWM DAC	1	13	-	-	-	1
Noise Generator	1	5	-	-	-	1
PLL	3	1	-	-	-	1
AGC	4	12	1	1	-	-
Data Acquisition	4	0	2	2	-	-
Signal Processor	2	12	1	1	-	-

Table 1. Summary of mixed-signal resources required.

FPMA designs to use as a basis, a number of mixed-signal circuits was collected and evaluated as a way to gain insight into the resources that are needed in a mixed-signal system [5]. Included in this set of circuits are three types of data converters: a sigma-delta A/D converter, a dual-slope A/D converter, and a pulse-width-modulated D/A converter. These three example circuits serve to illustrate that data converters can be built from the available field-programmable resources in the analog and digital arrays. Other circuits include a noise generator, a phase-locked loop (PLL), an automatic gain controller (AGC), a simple data acquisition system, and a signal processor. A summary of the resources required to implement each of these circuits is extracted and tabulated in Table 1. The key information extracted includes the number of opamps, 4-input lookup tables, data converters, and interconnections required to implement each circuit. By designing a chip that could implement all of the demonstration circuits, it was expected that the most important resource and architectural requirements of a general and widely applicable FPMA will be elucidated.

The field-programmable digital array used in MADAR is implemented by replicating tiles from an earlier digital FPGA (LEGO) designed at the University of Toronto [6]. The general architecture of LEGO is shown in Fig. 2. Each tile in LEGO consists of four 4-input lookup tables, four D flip-flops, and connection resources for sixteen tracks in both the horizontal and vertical directions. From the data in Table 1, the maximum number of lookup tables required is fifteen, thus four LEGO tiles are needed to satisfy the digital logic requirements of the demonstration circuits.

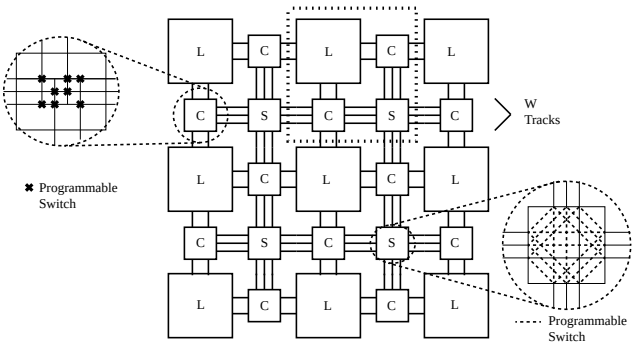


Fig. 2. General architecture of LEGO.

The field-programmable analog array is taken from an area-efficient implementation based on MOS transconductors [7]. Its architecture is shown in Fig. 3. The configurable analog blocks (CABs) that contain opamps and feedback capacitors are located along the right. Located along the bottom are programmable resistors, diodes, and capacitors. A programmable analog crossbar interconnect structure is used to connect these circuit elements. The analog array used in MADAR contains four CABs, which is again sufficient to implement all of the demonstration circuits listed in Table 1. It also contains six signal-controlled resistors, three programmable capacitors, and eight variable resistors.

A mixed-signal interface is required to connect the analog and digital arrays. This interface must provide both direct connections between the two arrays and also low-level signal conversion. Fig. 4 shows a block diagram of how the mixed-

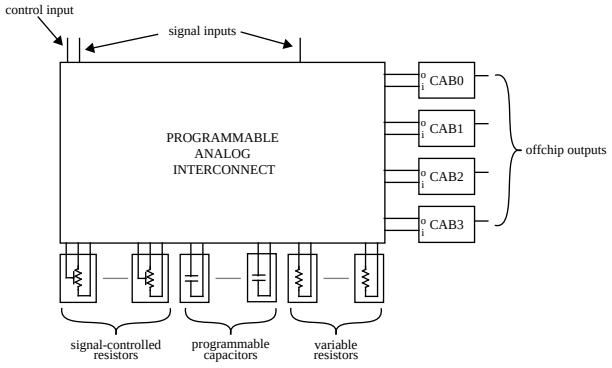


Fig. 3. FPAA architecture based on MOS transconductors.

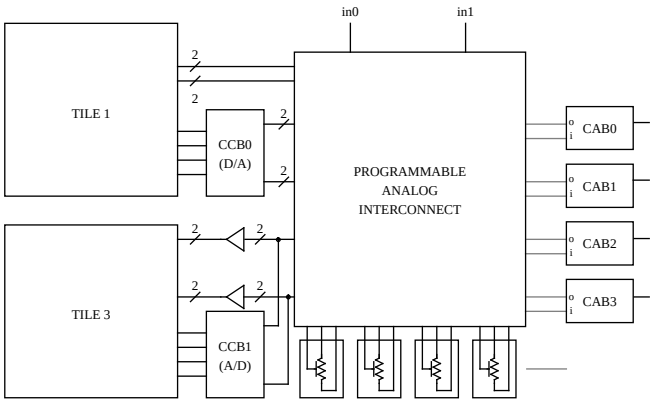


Fig. 4. Block diagram of mixed-signal interface.

signal interface fits within the analog and digital arrays. Included in the figure are two digital tiles, two CCBs, four signal-controlled resistors, four CABs, and the programmable analog interconnect. Since Table 1 shows that the interconnection requirements between the analog and digital arrays is low compared to the connectivity required within the arrays, the routing function is left to be only handled by the analog and digital arrays. By utilizing the routing resources in these arrays, a second level of hierarchical routing, which would have been in the interface, is avoided resulting in speed improvement and area savings. In Fig. 4, the top half of the array handles signals propagating in the digital-to-analog direction, while the bottom half handles signals propagating in the reverse direction.

In the digital-to-analog direction, binary outputs from the digital array can be connected directly to the control terminals of the signal-controlled resistors. A configurable D/A converter is used to convert digital data to an analog signal that can be fed directly as an input to the analog array.

In the analog-to-digital direction, the analog signal can come from the output of a comparator (a CAB with the opamp compensation disabled) so that it is already in digital form. This output signal is buffered to restore it to rail-to-rail voltage levels. A configurable A/D converter is used to provide linear conversion of low-level signals.

3 Configurable Converter Blocks

Data converters play a crucial role in a mixed-signal environment. They serve as the interface between the two different environments by converting data from digital to analog or vice versa. We have shown through the mixed-signal circuit examples that it is possible to build data converters using available field-programmable resources in the analog and digital arrays. This method offers great flexibility in terms of resolution and converter architecture; however, it suffers from both low speed and large area. To address this problem, we can build fast, area-efficient converters with a fixed resolution. However, because these converters are designed for use in a field-programmable environment, they should have some degree of flexibility. Therefore, we will introduce the concept of configurable converter blocks (CCBs), which may contain an A/D converter, a D/A converter, or specialized functional blocks that can be combined to form data converters. Configurability, in this context refers to the number and the resolution of the converters. The maximum resolution achievable from a CCB is given by *N*, and the maximum number of converters that can be realized is denoted by *n*. The general concept of CCBs is shown in Fig. 5. Fig. 5(a) is configured as a single *N*-bit converter, thus representing one extreme. Alternatively, the other extreme is illustrated by Fig. 5(c), which is configured as *n* 1-bit converters.

For the prototype chip (MADAR), we have chosen to implement two CCBs, each with the parameters *N*=4 and *n*=2. Therefore, each CCB can be configured as either a single 4-bit converter or two 2-bit converters. One CCB performs A/D conversion while the other handles D/A conversion. Both CCBs are designed to achieve a conversion rate of 1 MSample/s. Easily expandable area-efficient converter architectures are chosen so that higher resolution CCBs can be implemented in future prototypes. Furthermore, fully-differential signalling is used in the design of the CCBs to reduce the effect of noise and crosstalk. The next two sections will describe the configurable 4-bit data converters that are used as the CCBs.

3.1 Configurable 4-bit D/A Converter

The configurable 4-bit D/A converter, shown in Fig. 6, is based on a linear current division technique using MOS transistors [8]. The transistors form a MOS equivalent of an R-2R network, which performs a binary division of the current by successively partitioning the current between the series and shunt branches. A single configuration bit (4bit) determines the mode of operation; a binary ‘1’ indicates four-bit operation and a binary ‘0’ indicates two-bit operation. In two-bit mode, the two D/A converters function independently by opening the MOS switches that connect the two; in effect, each D/A has its own current source, current division network, and opamp. A single 4-bit D/A converter can be realized by combining the two current division networks. The upper network determines the current contribution from the MSBs, while the lower network determines the current contribution from the two LSBs. Also, the current from the lower network is diverted to the

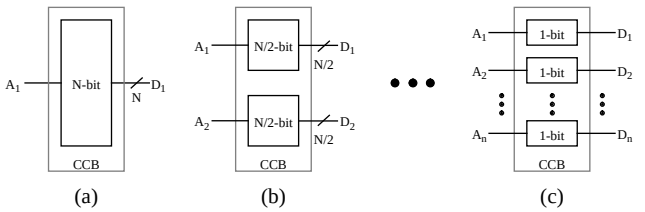


Fig. 5. Concept of configurable converter blocks.

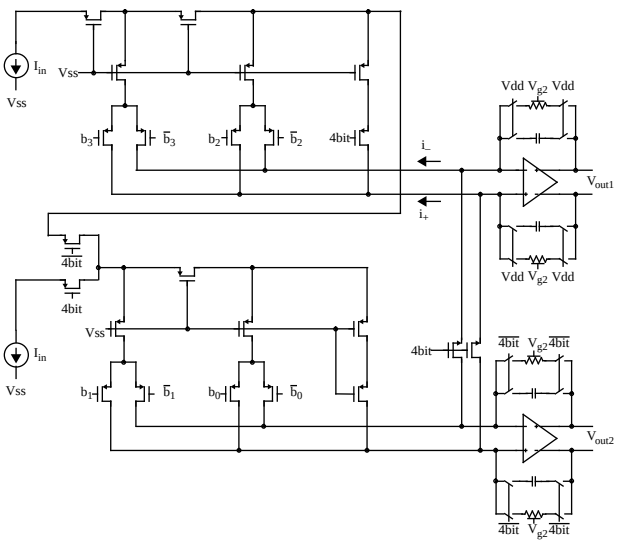


Fig. 6. Configurable 4-bit D/A converter.

upper opamp where it is summed with the current from the upper network.

3.2 Configurable 4-bit A/D Converter

A configurable 4-bit A/D converter with integrated sample-and-hold (S/H) inputs is implemented using a two-step architecture [9]. It takes advantage of the fact that a two-step converter consists of two independent A/D converters as shown in Fig. 7. For four-bit resolution, the coarse and fine sections can be combined by closing the upper configuration switch (4bit) to realize a 4-bit A/D converter. For 2-bit resolution, each A/D can function independently by closing the lower switch ($\overline{4bit}$) to give two 2-bit A/D converters. The coarse and fine A/D converters are constructed using flash architectures to achieve high speed conversions.

4 Prototype Chip

A prototype chip (MADAR) has been designed in a 1.2 μm double-metal double-poly CMOS technology, and its floorplan and plot are shown in Fig. 8(a) and Fig. 8(b), respectively. The chip measures 7292 μm x 4279 μm and is core-limited to 86 I/O pins. A primary goal in the design of the interface is to make it compact; that is, its area should by significantly less than the area consumed by the analog and digital arrays. In MADAR, the interface containing the two

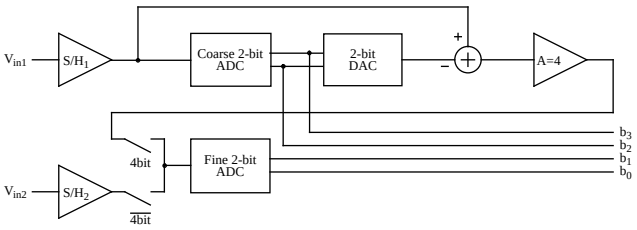
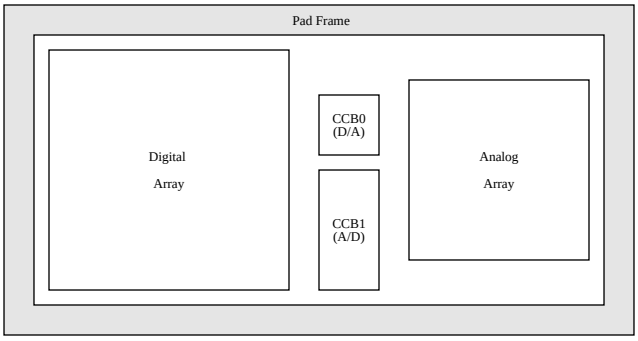


Fig. 7. Configurable 4-bit A/D converter.

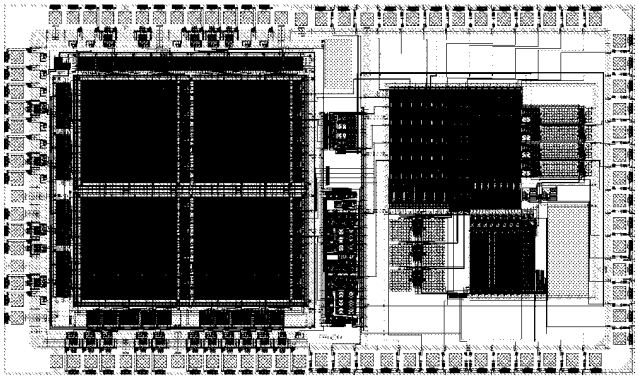
CCBs occupies only 6.7% of the active area. A total of 2471 programming bits are required to map the desired mixed-signal circuit into MADAR with the following distribution: 2116 bits for the digital array, 353 for the analog array, and two for the interface.

Fully-differential circuit design techniques are used throughout the analog circuitry to reduce the effect of noise coupling and crosstalk. Guard rings are used to shield the analog circuitry from noise coupled through the substrate. Furthermore, separate power pins supply the analog and digital circuitry to reduce the effect of noise coupling through the power lines.

The performance of the prototype must be specified individually for each section of the chip. Currently, the performance of the analog array is limited by the opamps in the CABs, which have a measured unity gain frequency of 3 MHz. By improving the opamp performance, the analog array is capable of higher bandwidths. The performance of the LEGO tile used in the digital array is comparable to commercial FPGAs of the same generation [6]. The CCBs were designed to operate at 1 MHz with 4-bit resolution in the prototype chip. These parameters were chosen to maintain compatibility with the analog and digital arrays. Faster, high resolution CCBs are easily attainable with present technology [8][9].

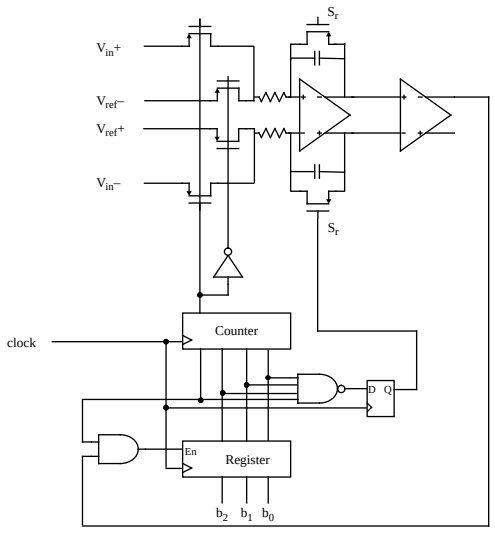


(a)



(b)

Fig. 8. (a) Chip floorplan; (b) chip plot.



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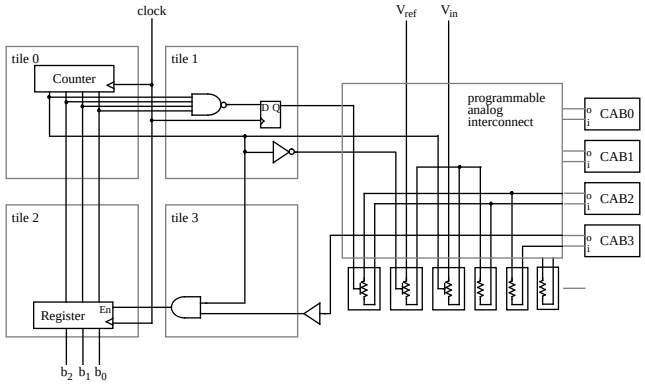

(b)

Fig. 9. Embedding of dual-slope A/D converter into MADAR (a) dual-slope A/D converter schematic (b) embedding into MADAR.

Using the dual-slope 3-bit A/D converter as an example, we will illustrate the embedding of a mixed-signal circuit into MADAR. Fig. 9(a) shows the schematic for the dual-slope 3-bit A/D converter, and Fig. 9(b) shows how the circuit is embedded into MADAR [10]. The circuit takes an analog input signal V_{in} and converts it to an equivalent digital output given by b_2, b_1, and b_0. The circuit operation begins by closing switch S_r to reset the integrator. Then V_{in} charges the integrating capacitor for a fixed time interval determined by the counter, and the output voltage of the integrator proceeds to ramp up with a slope proportional to V_{in}. Next, the capacitor is discharged by a reference source V_{ref} of opposite polarity, and ramps down at a constant rate proportional V_{ref}. When the integrator output reaches zero, the counter contains the digital equivalent of the analog signal, and is transferred to the register.

The 4-bit counter is mapped into tile 0, the register is mapped into tile 2, and the rest of the digital logic is mapped into tiles 1 and 3. Signals that propagate in the digital-to-analog direction must go through tile 1 while signals that propagate in the reverse direction must pass through tile 3. The connectivity between the analog components is accomplished by the programmable analog interconnect. CAB2 is used for the integrator and CAB3 implements the comparator. The input signals V_{in} and V_{ref}, and the output signals b_2, b_1, b_0 are all connected to external pins. The maximum conversion rate of this 3-bit A/D converter is limited by the reset time (1 μs) of the integrator in the analog array. This constraint allows a maximum clock frequency of 1 MHz. The A/D conversion rate is then computed by dividing the clock frequency by the maximum value of the 4-bit counter resulting in a conversion rate of 62.5 kSamples/s. Fig. 10 shows the simulation result for the 3-bit A/D using a mixed-mode simulator called Saber [11]. The digital circuitry is modelled behaviorally, while the analog portion is modelled at the circuit level. The figure shows the resulting digital output response (count up from 000 to 111) to an analog input staircase waveform.

5 Conclusions

A novel FPMA architecture is proposed, which consists of field-programmable analog and digital arrays, and configurable converter blocks (CCBs). Fast area-efficient CCBs are designed to perform signal conversion between the analog and digital arrays. A prototype IC implemented in a 1.2 μm CMOS technology has been designed and will be submitted for fabrication shortly. By implementing the set of mixed signal circuits found in [5], the concept of an FPMA will be successfully demonstrated. This has been only a first attempt to combine the area of field-programmability with that of mixed-signal circuits. Future work to improve the performance of the arrays and CCBs, and to develop a suite of CAD tools for mixed-signal design is required to make FPMAs a commercially viable technology.

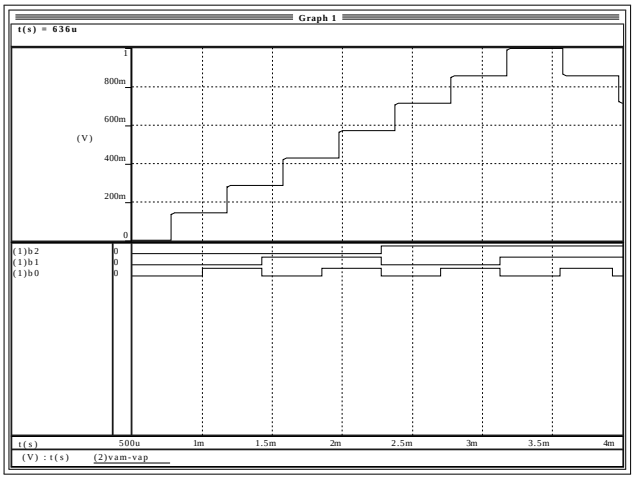

Fig. 10. Saber simulation of dual-slope A/D converter.

Acknowledgments

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