A Compact Parasitic-Insensitive Dual-Frequency $\Delta\Sigma$ Modulated CMOS Capacitive Sensor

Ritu Raj Singh, Karim Abdelhalim and Roman Genov
Department of Electrical and Computer Engineering
University of Toronto
Toronto, Ontario
Email: {rituraj, karim, roman}@eecg.utoronto.ca

***Abstract*— We present a simple, high-sensitivity, array-based capacitive sensor for biological applications. The circuit can accurately sense ungrounded coupling capacitances, while strongly attenuating the effect of unwanted parasitics. It can also perform capacitance-voltage profiling of nonlinear biological capacitances at very low voltages. We implement a dual input frequency $\Delta\Sigma$ modulator to perform improved noise filtering and an increased dynamic range. We verify the circuit implemented in a 0.35μm CMOS technology by simulating for different values of parasitic capacitances, process corners and varying test voltages across capacitors.**

I. Introduction

Lab-on-chip devices are increasingly being used in life science applications. Their small form factor coupled with a fine spatial resolution is attractive for low cost and highly sensitive study of microorganisms. Among the various sensory techniques used in lab-on-chip devices for life science applications, capacitive based sensing is particularly attractive. By measuring the electrical charge developed when a weak electric field is applied in the vicinity of the analyte, the technique is not only minimally invasive but also cost effective. With minimal post-processing requirements, implementation of highly sensitive capacitive sensing on low-cost CMOS technologies is feasible [1].

Some of the life sciences applications of capacitive sensing are membrane capacitance measurement in a patch clamp setup, monitoring cell cultures and bioparticle detection [2]–[4]. Many of these applications require measuring capacitance between two accessible nodes neither of which are an AC ground, known as the coupling capacitor. Development of a high sampling rate and a high density capacitive sensory microsystem for such applications would require compact, low power pixel-based capacitance measurement and digitization.

Charge based capacitance measurement (CBCM) is a widely used capacitive measurement technique [1]. Attractive due to its compact implementation, it cannot selectively measure coupling capacitances [5]. It measures the total capacitance at a node including any unwanted parasitic capacitance. Fig. 1 shows the CBCM circuit. The average charging current measured by the ammeter includes the contribution of the coupling capacitance C_X and the parasitic capacitance C_{P1}. On-chip efforts to measure this current are prone to errors due to limitations in the linearity of the simple current mirrors involved.

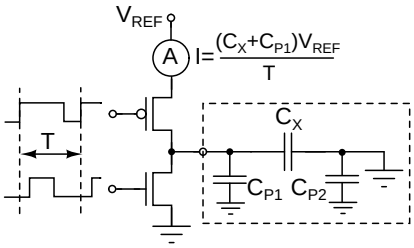

Fig. 1. Charge based capacitance measurement (CBCM) circuit.

Several CBCM modifications are used to cancel the unwanted parasitics which include using differential structures [1] or taking the difference of recordings with and without the analyte [6]. They require exact matching and electrical boundary conditions for better accuracy [1] or are infeasible for applications like cell monitoring [5], [6]. The presence of a large parasitic capacitance or voltage varying leakage currents limit the dynamic range of the system. Calibration is usually used to cancel such effects. This is however cumbersome and may be inefficient when the parameters are time varying such as in a patch-clamp setup [2].

Moreover, biological capacitances are often a nonlinear function of the applied terminal voltage [7]. The CBCM technique cannot perform such capacitance to voltage profiling since the PMOS transistor of the inverter in Fig. [1] would fail to turn-on when V_{REF} drops below its threshold voltage. A fast analog-to-digital conversion is required for applications where the capacitance changes with time as in a flowing bioparticle detection [3] or where a high resistance of the analyte restricts the charging frequency [8].

Coupling capacitance measurement circuits that overcome parasitic sensitivity and voltage-varying leakage currents make the input-output transfer function a weak function of these parameters. Such circuits invariably employ an operational amplifier-based switched capacitor amplifier or an integrator [9]–[11]. The effect of the parasitic capacitance at the output is attenuated proportional to the gain of the amplifier. Thus, to achieve an accuracy of attofarads where the parasitic capacitance could be in the order of a few picofarads, a very high operational amplifier gain of the order of 90dB and above is required. The gain requirement increases com-

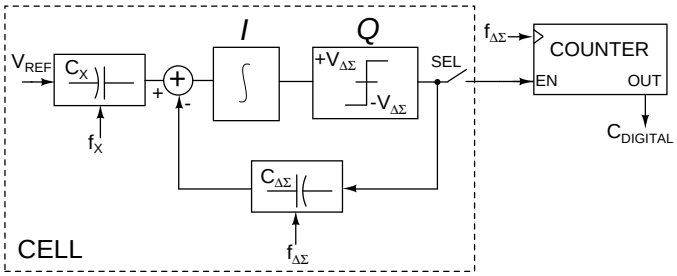

Fig. 2. Top-level architecture of the implemented capacitive sensor.

plexity and adversely affects the compactness of the capacitance measurement circuit. A conventional correlated double sampling (CDS) technique was used in [10] to reduce the requirement of a high amplifier gain. The technique is however sensitive to the parasitic capacitance at the amplifier input. Owing to the low frequency requirements of capacitance measurement, the integrator-amplifier can be placed inside a simple, compact first-order delta-sigma modulator to provide a high accuracy, low-noise digitized output [9]–[12].

This work builds up on the previous efforts, by employing a very-accurate overlapping clock-based charge transfer method for switched-capacitor integrators [13]. The technique has higher tolerance to amplifier input parasitic capacitance by providing much higher amplifier gain than that achieved by the conventional CDS technique [10]. The relaxed amplifier complexity enables the use of a simple single-ended cascode amplifier while retaining a high dynamic range. The amplifier is placed inside a simple, compact first order delta-sigma modulator. Programmable, very high input dynamic range is achieved by utilizing separate operating frequencies and voltage references for the input and the feedback branch of the delta-sigma modulator.

II. Architecture

Fig. 2 shows the block diagram of the implemented switched-capacitor coupling capacitance measurement circuit. Each sensing circuit in the capacitive sensing array consists of an accurate integrator I that accumulates charge proportional to the unknown capacitance C_X. The integrator output is then digitized using a 1-bit quantizer Q, placed in a delta-sigma loop. The integrator I accumulates charge from C_X at a switching frequency f_X. The feedback branch of the delta-sigma loop dumps charge onto the integrator I at a frequency $f_{\Delta\Sigma}$ which could be higher than f_X. This facilitates a faster conversion for applications where f_X is limited due to the resistive properties of the analyte [8]. V_{REF} can be varied to allow capacitance-voltage profiling of C_X. Reducing V_{REF} compared to $V_{\Delta\Sigma}$ increases the dynamic range of the capacitive sensing circuit. In an array implementation, capacitance measurement can be performed in a column parallel fashion, to time-share the counter. The equivalent digitized value of C_X is directly read from the row-parallel counter. The individual blocks of the capacitive-sensing circuit are discussed next.

III. VLSI Circuit Implementation

A. Integrator

Fig. 3 shows the cell-level implementation of the capacitance measurement circuit employing an improved CDS integrator [13]. The input branch contains the coupling capacitance C_X to be measured, C_{P1} and C_{P2}, the lumped parasitic capacitances and R_{path}, the lumped resistance of the charging path. The CDS integrator provides accurate charge transfers from the input capacitor C_X, insensitive to flicker noise, opamp offsets and the parasitic capacitance at the input of the amplifier. It also reduces the effect of charge injection and clock feedthrough errors, crucial for a high sensitivity capacitive sensor. The integrator uses an overlapping clock scheme for operation, which ensures that the input capacitor is never left floating [14].

The basic principle behind the operation of the integrator is switching the node K from V_{REF} to V_{DC} while keeping node L at a steady voltage. This results in an accurate charge dump onto the feedback capacitor C_{F1}, provided the output of the integrator V_{INT+} varies slowly with each clock cycle. The role of the capacitor C_{F2} is to ensure fairly unchanging voltage at node L, before dumping charge onto C_{F1}, in each clock cycle. The size of C_{F1} and C_{F2} is therefore chosen large compared to the input capacitors C_X and $C_{\Delta\Sigma}$. Clock phases ϕ_1 and ϕ_2 can be used interchangeably to generate an inverting or a non-inverting integrator configuration for the $C_{\Delta\Sigma}$ branch.

Assuming zero initial charge on the feedback capacitor C_{F1}, the voltage at the output of the integrator after M clock cycles is shown in eq. (1). As evident, even though the charge integration on the feedback capacitor is accurate, the output of the amplifier contains terms due to the instantaneous flicker noise and the voltage offset of the amplifier. These errors are eliminated by correlated voltage differencing performed by the next-stage quantizer block.

$$V_{INT+} = \frac{M(V_{REF} - V_{DC})C_X}{C_F} + V_{flicker} + V_{offset} \quad (1)$$

A qualitative analysis of the input referred noise of the integrator is provided as follows,

$$\overline{v_{in}^2} = \overline{v_{kTC}^2} + \overline{v_{amplifier}^2} + \overline{v_{supply}^2}, \quad (2)$$

$$\overline{v_{kTC}^2} + \overline{v_{amplifier}^2} = 2\left(\frac{kTx}{C_X(1+x)} + \frac{2kT}{3C_X(1+x)}\right), \quad (3)$$

$$\overline{v_{supply}^2} = \frac{g_m(S_{VREF} + S_{VDC} + S_{VGND})}{4(1+x)C_X}. \quad (4)$$

where, x=$R_{path}g_m$, R_{path} represents the total resistance in the input branch and g_m is the transconductance of the amplifier. S_{VGND}, S_{VREF} and S_{VDC} are the noise-voltage power spectral densities of the supplies assuming a white spectrum. Using a simple single-ended amplifier with gain A shown in Fig. 4, reduces the amplifier noise. It however makes the circuit susceptible to ground supply noise. It should also be mentioned that the random circuit noise is reduced

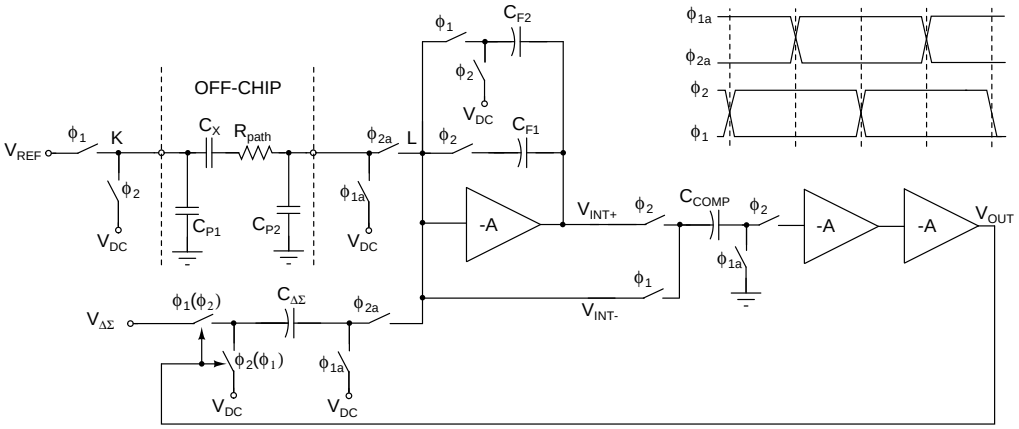

Fig. 3. Capacitance measurement circuit.

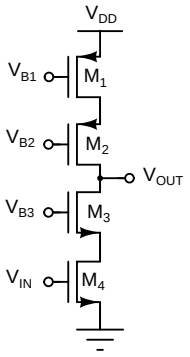

Fig. 4. Single-ended cascode amplifier circuit A.

significantly over multiple samples by the digital low-pass filtering action of the counter.

The capacitor mismatch of C_{F1} is the only significant source of capacitor mismatch in the integrator. Such mismatch errors are moderate, due to a sufficiently large value chosen for C_{F1} [15]. The mismatch in the transistor threshold voltages also introduces errors. V_{DC} equals the threshold voltage of the amplifier shown in Fig. 4, without any mismatch. Due to variation in transistor parameters over the chip, any difference between the amplifier threshold voltage and V_{DC} will cause a small voltage step at the output, whenever the feedback loop containing C_{F2} closes. This introduces errors, due to the movement of the input node L. Corner simulations have been performed to provide an estimate of such errors as discussed below.

B. $\Delta\Sigma$ Modulator

The integrator discussed above is placed inside a delta-sigma loop in each cell. This yields implementation simplicity and the circuit and quantization noise filtering performed using the simple digital counter.

The integrator output feeds the comparator. The capacitor C_{COMP} in the comparator performs a correlated voltage differencing operation canceling the errors mentioned in eq. (1). A single bit quantizer is inherently linear, which makes the delta-sigma modulator insensitive to any mismatch errors due to the offset voltage of amplifier A [16].

The dynamic range of the delta-sigma loop is enhanced at the cost of resolution by using a lower V_{REF} as compared to $V_{\Delta\Sigma}$. The input path resistance R_{path} determines f_X the frequency at which C_X can be charged. The delta-sigma operating frequency $f_{\Delta\Sigma}$ can however be much higher, yielding higher dynamic range. A higher operating frequency also assists in better noise filtering by achieving a smaller bandwidth of the counter-based digital low pass filter.

Let $C_{X(DIGITAL)}$ and $C_{\Delta\Sigma(DIGITAL)}$ be the equivalent digitized capacitance values for capacitors C_X and $C_{\Delta\Sigma}$ from the counter respectively. For a large N, they are related as

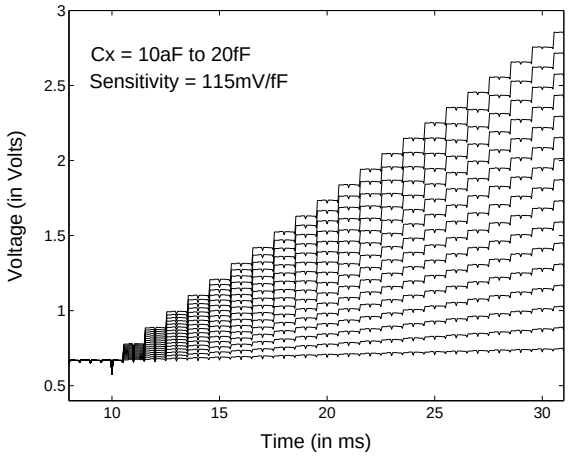

Fig. 5. Transient simulation of the CDS integrator for varying C_X.

TABLE I
ROOT MEAN SQUARE ERROR Vs. PARASITIC CAPACITANCE

C_{P2} (pF)	**RMS error (aF) [C_X=10aF to 20fF, V_{REF}-V_{DC}=2.63V]**	**RMS error (aF) [C_X=19fF to 20fF, V_{REF}-V_{DC}=2.63V]**	**RMS error (aF) [C_X=1fF to 2pF, V_{REF}-V_{DC}=25mV]**
0	3.8	3.8	523
0.1	4.5	4.1	-
0.3	5.8	4.0	-
0.4	5.8	-	535
0.5	6.0	4.3	-
3	6.3	3.7	604
7	9.6	5.0	739

TABLE II
ROOT MEAN SQUARE ERROR Vs. PROCESS CORNERS

Process corner threshold voltage V_T	**RMS error (aF) [C_X=10aF to 20fF, C_{P2}=0.1pF, V_{REF}=3.3 V]**
ΔV_{TN}=+0.1V, ΔV_{TP}=-0.1V	6.3
ΔV_{TN}=-0.1V, ΔV_{TP}=+0.1V	6.3
ΔV_{TN}=-0.1V, ΔV_{TP}=-0.1V	18.0
ΔV_{TN}=+0.1V, ΔV_{TP}=+0.1V	20.5

$$C_{\Delta\Sigma(DIGITAL)} + C_{X(DIGITAL)} \frac{V_{REF} f_X}{V_{\Delta\Sigma} f_{\Delta\Sigma}} = N_{HIGH} \quad (5)$$

$$C_{\Delta\Sigma(DIGITAL)} - C_{X(DIGITAL)} \frac{V_{REF} f_X}{V_{\Delta\Sigma} f_{\Delta\Sigma}} = N - N_{HIGH} \quad (6)$$

Solving (5) and (6), the equivalent digitized capacitance value for the capacitor C_X is given by

$$C_{X(DIGITAL)} = \frac{V_{\Delta\Sigma} f_{\Delta\Sigma}}{V_{REF} f_X} \left(N_{HIGH} - \frac{N}{2} \right) \quad (7)$$

V_{OUT} is the enable signal for the counter as shown in Fig. 2. From eq. (7), if N is an integral power of two, then $C_{X(DIGITAL)}$ can be directly read from the binary counter.

IV. Simulation Results

An example capacitive sensor design has been simulated in a standard 0.35μm CMOS technology. $C_{\Delta\Sigma}$, C_{F1} and C_{F2} have been chosen to be 25fF, 0.5pF and 1pF respectively. The design has an input range C_X from 10aF to 20fF, when V_{REF} = $V_{\Delta\Sigma}$= 3.3V. All switches are transmission gates with both PMOS and NMOS minimum sized for minimal charge injection. f_X was 1 kHz. The simulated open loop gain of the amplifier, A, is 72dB, with transistor channel lengths of 1 μm.

Fig. 5 shows the transient response at the output of the CDS integrator showing charge integration, after an initial reset on C_{F1}. Table I shows the dependence of the measured root mean squared capacitance error versus the parasitic capacitance C_{P2} of the CDS integrator for different input capacitance ranges. For each value of C_{P2}, forty different values for C_X were uniformly chosen between 10aF and 20fF. A linear fit was then performed and the mean square error evaluated. As can be seen from the table, the error gradually increases with increasing C_{P2} but is weakly sensitive.

Table II shows results of the corner simulation for the CDS integrator in Fig. 3. The amplifier shown in Fig. 4 is the only mismatch critical block. The corner results therefore provide a good estimate of the mismatch performance of the integrator. Fig. 6 shows a plot of the digital bits extracted by the delta-sigma modulator versus C_X confirming the system linearity. The simulation was run for 1200 cycles for uniformly spread values of C_X with f_X = $f_{\Delta\Sigma}$ = 1 kHz. C_P was 0.1pF and V_{REF} = $V_{\Delta\Sigma}$ = 3.3V.

V. Conclusions

A simple capacitive sensor attractive for array-based biological sensing applications with accuracy of a few attofarads has been presented. It uses parasitic-insensitive correlated double sampling technique for accurate charge transfers and utilizes a dual input frequency delta-sigma modulator for an improved noise performance and higher dynamic range. Varying the voltage reference allows capacitance-voltage profiling while separating the voltage references for the input branches enhances the dynamic range of the circuit. The circuit performance is fairly tolerant to mismatch errors.

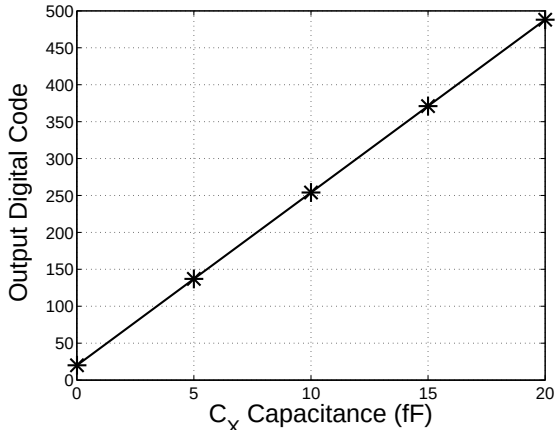

Fig. 6. Digital readout from the delta-sigma loop vs. input capacitance C_X.

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