Low-distortion Super-GOhm Subthreshold-MOS Resistors for CMOS Neural Amplifiers

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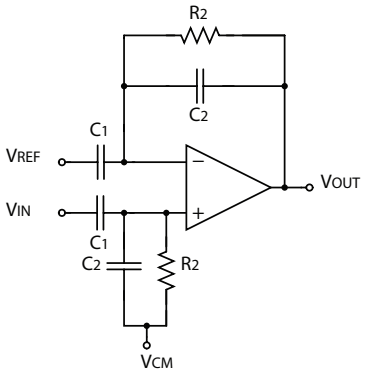
***Abstract*— A low-distortion super-GOhm subthreshold MOS resistor is designed, fabricated and experimentally validated. The circuit is utilized as a feedback element in the body of a two-stage neural recording amplifier. Linearity is experimentally validated for 0.5 Hz to 5 kHz input frequency and over 0.3 to 0.9 V output voltage dynamic range. The implemented pseudo resistor is also tunable, making the high-pass filter pole adjustable. The circuit is fabricated in 0.13-μm CMOS process and consumes 96 nW from a 1.2 V supply to realize an over 500 GΩ resistance.**

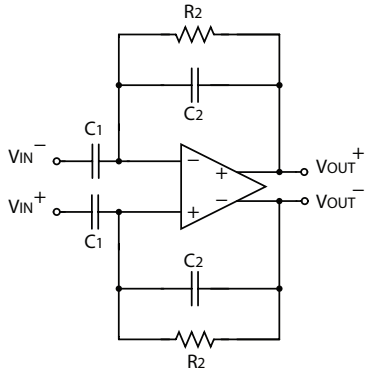
I. Introduction

Monitoring neuro-electrical activity in the brain such as neural oscillations is a vitally important method in diagnostics and evaluation of various neurological disorders such as epilepsy. Typically for neural recordings, the signals are in the range of 10μV to 5 mV with frequencies from as low as 0.5 Hz to a few kHz [1]. Also, the total electrode noise including thermal noise of electrodes and background noise within the extra-cellular region is approximately 20μV for a 1MΩ electrode with a 5kHz bandwidth [2]. The chemical interaction of electrodes and tissue generates a large DC voltage offset which can saturate a neural amplifier, and thus requires a low-frequency high-pass filter (<1Hz) to be eliminated. Thus, the requirements for an integrated neural recording front-end include a compact AC-coupled amplifier with a gain of approximately 60dB, a bandwidth from below 1Hz to up to 5 kHz and an integrated noise of below 10μV. With neural signals as high as 5mV, this requires an ADC dynamic range of 8-10 bits.

Single-ended and differential amplifiers that are commonly used as a neural amplifier are shown in Figure 1. The gain is set by the ratio of the input capacitor to the feedback capacitor. The low-frequency high-pass filter pole is set by the feedback resistance and capacitance product. This results in large integrated passives. An example of neural recording front-end is demonstrated in [3] which integrates 100 channels. A conventional neural amplifier similar to what is shown in Figure 1(a) is used. To implement the feedback resistor that is in the GOhm range,



(a)



(b)

Fig. 1: Single-ended (a) and differential (b) amplifier as an AC-coupled neural amplifier.

subthreshold-biased diode-connected transistors are utilized instead of bulky passive resistors. Due to a simple architecture, this pseudo resistor adds small noise and parasitics to the amplifier. However, its resistance changes significantly over a large voltage swing. Additionally, this or other suggested pseudo resistors, such as those in [4] and [5], should also possess frequency-independent resistance to keep the high-pass pole frequency of the amplifier constant, and consequently, minimize output distortion.

In [6], a complementary circuit with both PMOS and NMOS transistors is proposed where the gates of both transistors are controlled separately. The proposed design performs very well in terms of linearity over a large dynamic range, but suffers

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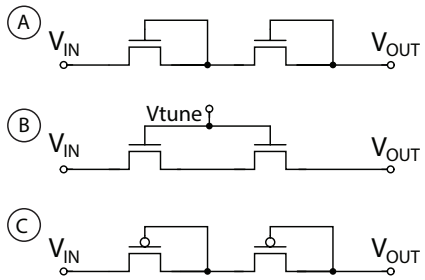

Fig. 2: Three variable-V_{GS} pseudo resistor implementations. High linearity is maintained only for small voltage swings.

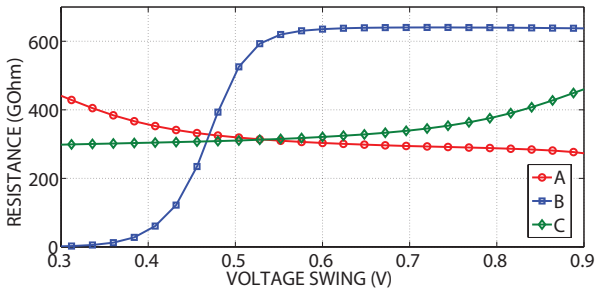

Fig. 3: Simulated resistance of the circuits shown in Figure 2.

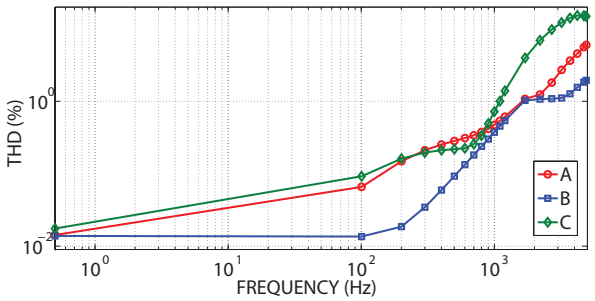

Fig. 4: Simulated output THD versus input signal frequency for the circuits shown in Figure 2.

from being vulnerable to any process, common mode or offset voltage variations, especially because the device operates in the subthreshold mode. To avoid such sensitivity problems, current-controlled pseudo resistors with simple [4], or complex [5] architectures were proposed. Simple methods which typically use a single MOS transistor, suffer from resistance being asymmetric with respect to the output common mode voltage. The complex methods such as the one proposed in [5], which is based on a cross-coupled architecture, demonstrate symmetric resistance with good linearity, but only for 0.2 V.

We present a design of a pseudo resistor which is based on the idea of making V_{eff} of a MOS device independent of the voltage across it to keep its resistance constant over a large dynamic range. Different pseudo resistor implementations are simulated and the results are compared to measurement results from two pseudo resistors that are fabricated in the body of the first and second stages of a neural amplifier in 0.13μm CMOS technology. The rest of the paper is organized as follows. Section II discusses different proposed configurations for the feedback element designed for small voltage swings. Section III presents the proposed feedback element for large voltage swings and contains simulation results that compare it with other methods. Section IV describes the experimental results from a fabricated neural amplifier.

II. Variable-V_{GS} Implentations

Method A in Figure 2 shows the approach used in [3] to implement a pseudo resistor. The diode-connected MOSFET maintains a stable DC operating bias point for the OTA but cannot be tuned and has non-linearity at high output swings. Two other methods are also presented in Figure 2 (methods B and C). These pseudo resistors along with a capacitor connected in parallel yield a high-pass pole in the sub-Hertz range. Thick-oxide NMOS/PMOS pseudo resistors are used in all these methods.

Figure 3 shows the simulated resistance for the three methods at 10 Hz. For these simulations, one node of the device is at 0.6V, while the other node is swept from 0.3V to 0.9V representing the output range of an amplifier. As shown, all the methods show reasonably constant resistance over small output voltage dynamic range of less than 200 mV. The circuits shown in Figure 2 are also compared in terms of THD (total harmonic distortion) as a function of the input frequency as depicted in Figure 4. As shown, THD is less than 1% for frequencies less than 1 kHz and it becomes very low at 0.5 Hz due to the thick oxide MOS devices utilized. This results in linear performance of the amplifier for sub-Hz frequencies for low voltage swings.

An important feature for a pseudo resistor is the ability to be tuned to the bandwidth, allowing not only for attenuation of the low frequency drift or DC offsets but also for a shift in the high-pass pole frequency to correct for process variations. The pseudo resistor can be made tunable by setting gate of the MOS transistor to a programmable DC voltage [7] and operating the device in subthreshold as shown in method B of Figure 2. This MOSFET can be tuned for different

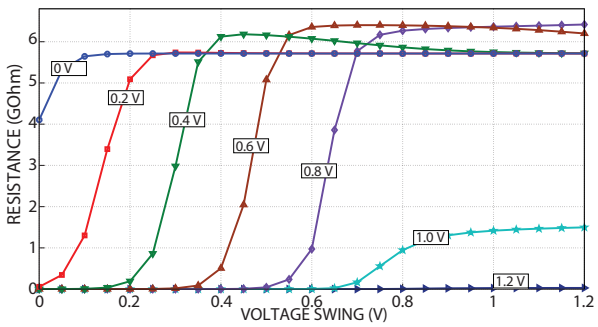

Fig. 5: Simulated resistance of tunable pseudo resistor (case B) for different tuning voltages.

frequency bands, but suffers from non-linearity at high output swings. Also the DC biasing point can drift if the resistance is set too high. Figure 5 shows the effect of changing V_{tune} in method B. Small V_{GS} values result in good linearity over a wide dynamic range, but setting V_{GS} of the feedback device too low leads to leakage issues. Junction leakage results in a bias drift that changes the input common-mode voltage and consequently results in saturating the OTA.

Another point that should be considered is the added parasitic capacitance and noise. Added noise is especially important if the amplifier with the pseudo resistor feedback is the first stage of a multi-stage front-end. Due to simple configuration of all the methods, they are all suitable in terms of added noise and parasitic capacitance.

Knowing the mentioned leakage problems with method B, and based on the simulation results shown in Figure 3 and Figure 4, method A was used in the implementation of the low-swing first stage of the fabricated neural amplifier as described in Section IV.

III. Fixed-V_{GS} Implentations

As the output dynamic range increases to half of Vdd or higher, all of methods discussed in the previous section fail to maintain a reasonably constant resistance. Next, this issue is addressed by implementing the pseudo resistor in a way where a subthreshold MOS device has constant V_{GS} for large voltage swings.

Three pseudo resistor implementations using fixed V_{GS} are shown in Figure 6. Resistance simulation results for these configurations are shown in Figure 7. For these simulations, one node of the device is at 0.6V, while the other node is swept from 0.3V to 0.9V representing the output range of an amplifier. For method D, both devices have a V_{GS} of 0.15V. The simulation results shows reasonably constant resistance over the large voltage swing ($< 16\%$ variation). Unlike method D, in method E, the resistance variation is less symmetric around the mid-range voltage, which leads to a more nonlinear performance of the circuit. Among these three configurations, method F shows the worst performance in terms of linearity over a large voltage swing.

To compare linearity of all the configurations in terms of input frequency, THD of each method is calculated for the input frequency range of 0.5 Hz to 5 kHz and is shown in Figure 8. As shown in this figure, THD of all methods is less than 0.5 $\%$ for frequencies from as low as 0.5 Hz to up to 1 kHz.

Based on mentioned points and simulation results shown in Figure 7 and Figure 8, method D shows the best performance in terms of linearity with a high and reasonably constant resistance over the entire neural amplifier output voltage range (Vdd/2).

IV. Experimental Results

A two-stage neural amplifier shown in Figure 9 was fabricated in 0.13-μm CMOS process. As the total gain

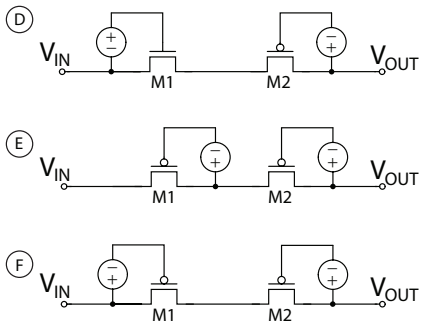

Fig. 6: Three fixed-V_{GS} pseudo resistor implementations. High linearity is maintained for large voltage swings.

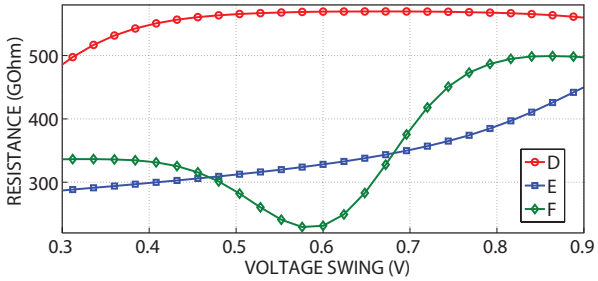

Fig. 7: Simulated resistance of the circuits shown in Figure 6.

is distributed between the two stages, the first stage has an output swing of below 100 mV. As a result, the resistive feedback element designed for this stage experiences a low voltage swing and can be chosen from variable-V_{GS} methods (A to C). For the second stage feedback element, one of the fixed-V_{GS} methods (D to F) must be used, as the output voltage swing is 0.6 V. As discussed, based on the simulation results, method A was chosen for the first stage and method D for the second stage.

Figure 10 shows how method D is implemented. The W/L ratio for M_1 and M_2 is 0.5/15 μm, for M_3 is 2×2.5/0.5 μm and for M_4 is 3×1/0.5 μm. The idea is to dynamically maintain the gate voltages of two MOS transistors using two source followers. This ensures a constant V_{GS} on the sub-threshold feedback devices, even for large voltage swings. The resistance can be reduced by increasing the bias current in the source followers and thus increasing the $|V_{GS}|$ of the MOS devices. The area is minimized by utilizing low-

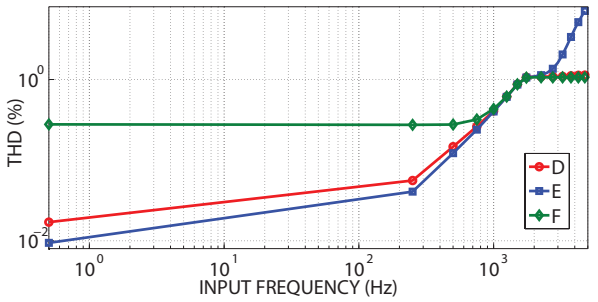

Fig. 8: Simulated output THD versus input signal frequency for the circuits shown in Figure 6.

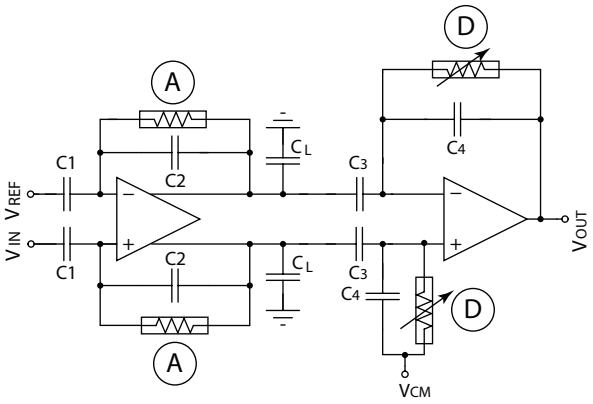

Fig. 9: Fabricated two-stage AC-coupled neural amplifier.

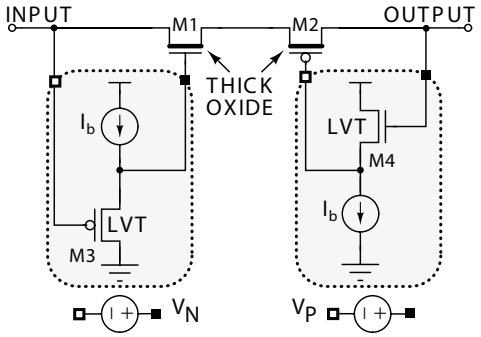

Fig. 10: Schematic of the proposed resistive feedback element with fixed-V_{GS} pseudo resistors

threshold devices (LVT) to allow $|V_{GS}|$ tunability between approximately 0.1V and 0.3V without requiring a wide device. Additionally, compared to the conventional approach [7], this feedback resistance achieves more accurate biasing by guaranteeing a controlled resistance (i.e., with a $|V_{GS}|$ >0V) on the device in the feedback, without leakage problems.

The measurement results are shown in Figure 11. As shown in this figure, the high-pass pole of the feedback element can be adjusted by varying I_b of the source follower. An example of transient experimental results in Figure 11 shows a significant observable improvement in the linearity of the amplifier. A 10-15dB improvement in distortion at sub-Hz frequencies was achieved experimentally when using the implemented approach in Figure 10 over the conventional sub-threshold transistor (method A) when used in the second stage.

V. Conclusion

A low-distortion high-resistance sub-threshold MOS resistor used in the feedback of a neural amplifier is presented. The proposed circuit is experimentally validated and shows a high resistance with less than 16 % variation over 0.6 V dynamic range. The resistive feedback element uses a fixed V_{GS} design technique and demonstrates 10-15 dB improved linearity over the full dynamic range of the amplifier output (0.6 V).

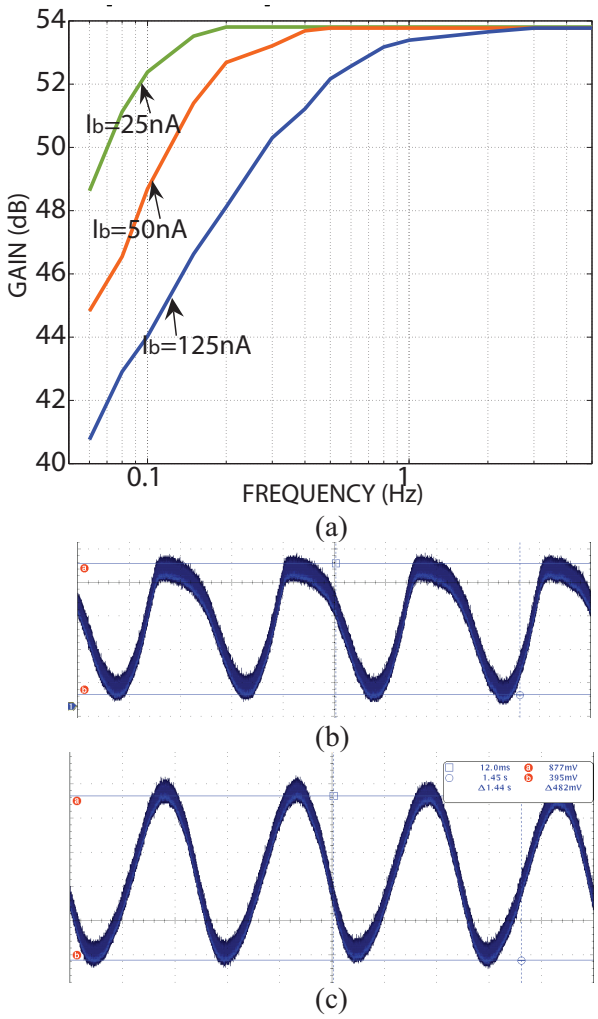

Fig. 11: (a) Experimentally measured high-pass filter frequency response for three different values of I_b. Experimentally measured output waveforms for a 1mV$_{pk-pk}$ 1Hz sinusoid input comparing (b) conventional (method A) and (c) proposed (method D) feedback elements performance, both when used in the second stage.

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