56-Channel Direct-Coupled Chopper-Stabilized EEG Monitoring ASIC with Digitally-Assisted Offset Correction at the Folding Nodes

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Abstract—We present a 56-channel neural recording interface with a chopper-stabilized DC-coupled front-end and a programmable mixed-signal DC cancelation feedback. Each recording channel has a fully-differential amplifier with 51-54dB of gain, an input-referred noise of $5\mu V_{rms}$ integrated from 10Hz to 5kHz and a CMRR of 65dB. Input DC-coupling allows for a simple chopping scheme without the area overhead of large capacitors and extra non-idealities compensation circuitry. Chopping is used to reduce the integrated input-referred noise from $7.5\mu V_{rms}$ to $4.2\mu V_{rms}$ over the bandwidth of 1Hz to 1KHz. Each channel contains a digital integrator and a 16-bit delta-sigma DAC in the feedback in order to cancel input DC offsets of up to ± 50mV and suppress the low frequency drift. Compensating the input DC offset at the folding node of the OTA provides an input-referred noise that is independent of the DC offset value. The recorded data by the array is digitized by 8 column-parallel SAR ADCs with 8-bit resolution and ENOB of 6.6 bits. Each channel in the neural recording array occupies 0.018mm^2. The 8.7mm^2 die, fabricated in a 0.13μm CMOS process, dissipates 1.07mW from a 1.2V supply. The integrated circuit has been validated in vivo in online intracranial EEG recording in freely moving rats.

I. INTRODUCTION

Recording electrographic neural activity from many locations in the brain provides information from a large population of neurons and helps improve our understanding of functions of the brain and of various neurological disorders such as intractable epilepsy [1]. Increasing the number of neural recording sites requires integrating many neural amplifiers on a single chip, which imposes various challenges including packing density, noise and power consumption.

Due to electrochemical reactions at the electrode-tissue interface, the neural tissue has different DC voltage levels at different electrodes. This voltage difference, known as input DC offset, causes a differential DC input signal that is typically 1-10mV and can be up to a maximum of 50mV. This DC component can saturate a high-gain DC-coupled differential amplifier.

The conventional method to implement a neural recording front-end is the widely-used closed-loop capacitive-feedback amplifier [2], [3], [4]. The general circuit architecture in this method is shown in Figure 1, in which the DC offset is blocked by large input capacitors. The first drawback of this method is the large area of the DC-blocking capacitors, preventing integration of many channels. These large capacitors also decrease the input impedance of the neural amplifier. Secondly, recording low-frequency signals while rejecting the tissue DC voltage requires a very small-frequency well-defined high-pass
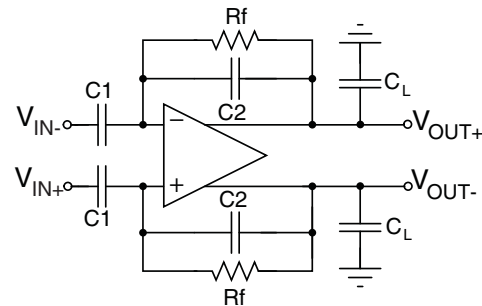

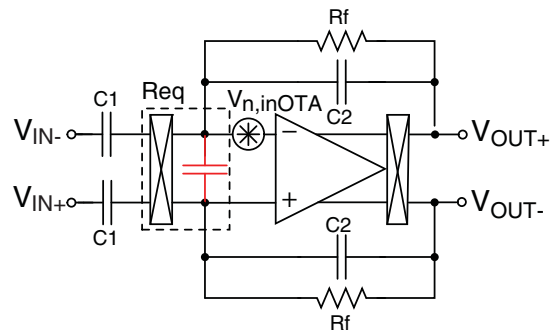Fig. 1. Conventional closed-loop capacitive-feedback neural amplifier.

Fig. 2. Chopping in neural amplifiers: chopper neural amplifier noise model.

pole. In the conventional method this high-pass pole is implemented with pseudo-resistors that suffer from non-linearity in the presence of a large output voltage swing [5], as well as excessive random variations over process and temperature.

The band of interest for neural recording includes frequencies less than 100Hz. Flicker noise from the amplifier is dominant in this frequency band and chopper-stabilization technique is typically used to reduce the flicker noise. Using the chopper-stabilization technique in the circuit in Figure 1 [2], [3], [4] increases the noise at low frequencies by a considerable amount. The equivalent circuit including the OTA input-referred noise source is shown in Figure 2. The chopper switches together with the OTA input transistors parasitic capacitors create a parasitic resistor at the input whose value is inversely proportional to the chopping frequency. This resistance and the DC-blocking capacitors will shape the OTA thermal noise with $1/f$ characteristic when referred to the input. This leads to additional circuit overhead such as a further increased input capacitor size to counter the
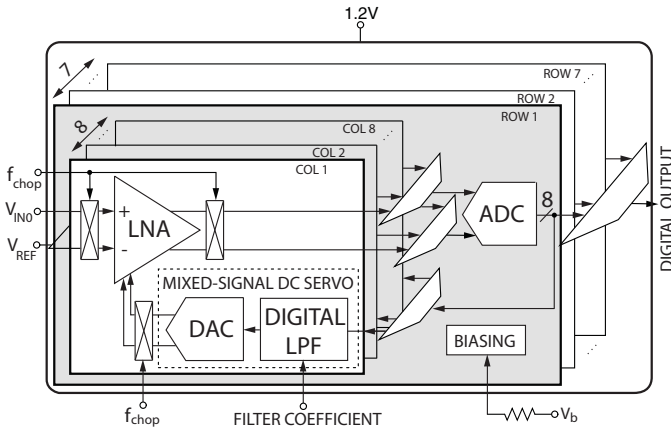
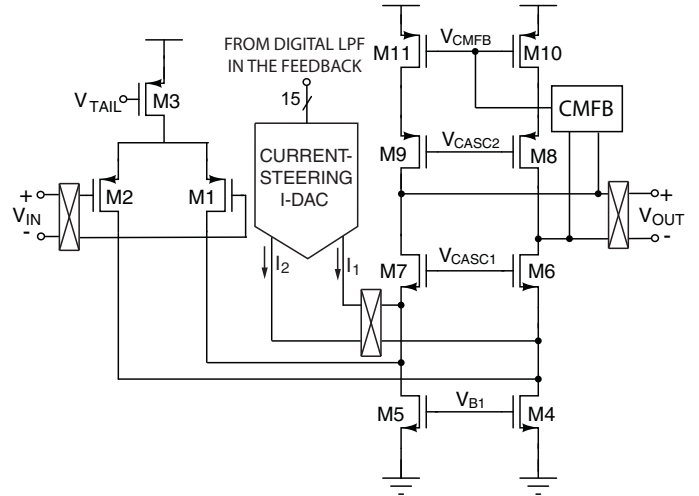Fig. 3. Block diagram of the 56-channel digitally-assisted neural interface.

Fig. 4. Circuit diagram of the front-end folded-cascode OTA. The current-steering I-DAC provides current to the folding node of the folded-cascode OTA.

noise multiplication effect [6], [7], as well as input impedance boosting and ripple compensation loops [7].

An alternative approach in designing neural signal amplifiers that block the tissue DC offset is using a low-pass filter in a feedback configuration. There are a few designs that use this technique but they have a large area and power which are excessive for integrating many recording channels [8] and they suffer from high-pass pole inaccuracy [9].

A fully-digital feedback can be used in the feedback to avoid these issues. A digital feedback loop does not require any large capacitors or pseudo resistors, which enables control of the high-pass pole frequency with more flexibility and accuracy. Also implementing the integrator in the digital domain would require smaller area than that in the design in [9]. The neural amplifier in [10] has such digital feedback for DC and low-frequency suppression with a small number of channels on-chip (4). However, in the design presented in [10] the input-referred noise and CMRR vary with the input offset when the number of fingers in the input transistors are changed. Also, the second digital loop for binary search add extra complexity to the system and impose area overhead. The design [10] does not provide chopping for flicker noise reduction.

This paper presents an integrated neural interface with 56 DC-coupled channels for recording intracranial EEG signals. The tissue DC offset at the input of the amplifier is canceled by a digitally-assisted feedback configuration, which yields channel area reduction by eliminating the large AC-coupling capacitors. The chopper stabilization technique is used to reduce the low-frequency noise of the input transistors without the need for the aforementioned circuit overhead [6], [7]. The high-pass pole frequency is programmed in the digital domain which provides a well-defined HPF cutoff frequency.

II. VLSI ARCHITECTURE AND CIRCUIT IMPLEMENTATION

The block diagram of our DC-coupled digitally assisted integrated circuit is shown in Figure 3. It consists of 56 neural amplifiers with tissue DC offset cancelation digital block, 8 column-parallel SAR ADCs, and one extra channel used for testing. Groups of 8 channels in a column share one ADC. Each channel includes a fully differential low-noise folded-cascode OTA, a digital integrator, a digital delta-sigma modulator, and a 4-bit offset-canceling DAC.

A. Analog Front End

The front-end OTA and the current-steering DAC in the feedback are shown in Figure 4. Neural signal amplification and filtering is performed by a folded-cascode OTA, used as the LNA in the front-end. Fully differential architecture is chosen to reduce common-mode noise and interference and achieve high CMRR. Thick oxide pfet transistors were used for the input pair in order to tolerate the voltage level variations in the tissue. Thermal noise was minimized by biasing the input pair transistors in the subthreshold region to achieve maximum g_m. Large transistor sizes are used for the tail current source(M3) to minimize its flicker noise contribution in the presence of a DC voltage difference at the input. A continuous-time common-mode feedback circuit was used to set the DC level of the output nodes.

Chopper modulation is implemented by cross-coupled switches. Minimum size switches are required in order to minimize residual offset due to charge injection and clock feedthrough. In order to remove flicker noise, the chopping clock frequency should be set higher than the $1/f$ corner frequency.

The mismatches in the OTA circuit cause a systematic offset. This systematic offset is canceled by the mixed-signal feedback, as well as the input DC offset from the tissue. However, when chopper-stabilization is activated, the opamp offset will be up-modulated to the chopper clock frequency and can not be sensed and removed by the digital feedback. This up-modulated offset can be removed by an off-chip low-pass filter or in software.

The OTA bandwidth is set considering a trade-off between the amplifier input-referred noise and the gain error after chopping, since the OTA acts as an anti-aliasing filter for the ADC in this configuration.

The OTA requires $8.2\mu A$ of current, which includes $4.8\mu A$ to the input pair transistors and $3.4\mu A$ into the cascode transistors.

B. Fully Differential SAR ADC

The analog output from each channel is digitized by an 8-bit column-parallel capacitive-charge-redistribution SAR ADC, before being sent to the digital feedback. Split-capacitor array is utilized to minimize the overall ADC area and power dissipation. As the digital output of the ADC is fed back to the opamp through the mixed-signal feedback, extra noise due to aliasing will appear at the output of the opamp and increase the input-referred noise of the analog front-end. The OTA provides a first order filtering. Therefore, considering the first-order roll-off of the opamp, the sampling rate of the ADC is set 10 times higher than the opamp bandwidth to achieve lower than 10μV input-referred noise.

C. Low-Frequency Suppression Mixed-Signal Feedback

The tissue DC offset and low-frequency signal is suppressed by a mixed-signal feedback. The feedback element has a low-pass transfer function and this effectively implements an HPF with a digitally-programmable low cutoff frequency (e.g., 1Hz) and cancels out the DC offset in the input signal (up to $\pm$50mV).

1) Digital Integrator: In order to guarantee stability in the DC cancelation loop, a first order integrator is used as a low-pass filter. A digital low-pass filter provides easier programming to adjust the pole and enables creating a well-defined high pass pole frequency. The digitally-programable high-pass pole does not vary by the large swing at opamp output, or process and temperature variations and linearity is preserved at low frequency. The sampling rate of the integrator is set to 25kHz (5 times the OTA bandwidth).

2) Delta-Sigma Modulator and Current-Steering DAC : A first-order delta-sigma modulator is used after DC offset integration by the digital integrator to reduce the number of bits to 4 [11]. This lowers the area and resolution requirement for the subsequent digital-to-analog conversion. The shaped quantization noise from the delta-sigma modulator is filtered by the feed-forward OTA low-pass characteristic. The first-order roll-off of the OTA introduces a portion of this noise to the ADC, which consequently leads to noise folding due to aliasing. This issue imposes a limitation on the order of the modulator. Therefore, a first-order modulator is used and the number of bits is reduced to 4, instead of 1, to reduce the amount of modulator shaped-noise fed to the ADC.

III. Experimental Results

A. IC Measurement Results

The experimentally measured amplitude frequency response of the neural recording channel is shown in Figure 5. Figure 5 shows the high-pass filter frequency adjusted from approximately 7Hz to 250Hz by modifying the integrator gain coefficient(λ). The high-pass pole can also be modified by changing the integrator sampling frequency.

System level experimental results are summarized in Table I. The output noise has been measured by a network analyzer. The integrated input-referred noise without chopping over the bandwidth of 10Hz to 5kHz is $5\mu V_{rms}$ (at room temperature), which yields a noise efficiency factor of about 7 [12]. The measure input-referred noise is constant
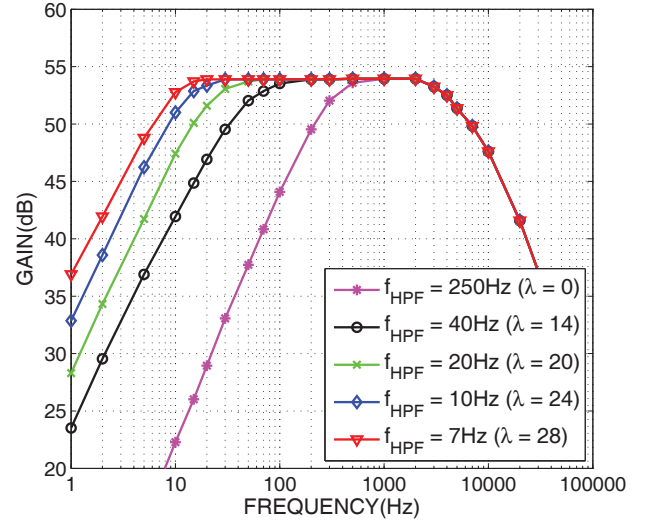

Fig. 5. Experimentally measured amplitude response of the system for different gain coefficients.

for input DC offsets less than $\pm$50mV. Chopping reduces the integrated input-referred noise over the 1Hz to 1kHz bandwidth from $7.5\mu V_{rms}$ to $4.2\mu V_{rms}$. The experimentally measured common-mode rejection ratio (CMRR) for a typical channel at 500Hz is 65dB.

The ADC performance is characterized by a 600Hz sine test input sampled at 50kS/s. The ENOB of two of the ADCs in two columns on the same die is measured to be about 6.6 when sampled at 50kS/s. Each channel consumes $12.5\mu A$ in the front-end (OTA and DAC), from which $8.3\mu A$ is used in the OTA, $3\mu A$ is used in the biasing network, and $1.2\mu A$ is consumed in the current-steering DAC, from a 1.2V supply voltage ($15\mu W$ in total). The digital block in each channel consumes $2.9\mu A$ and the ADC in each column consumes $2.2\mu A$ from a 1.2V supply ($2.64\mu W$).

Each channel in the neural recording array occupies 0.018mm^2, which includes the analog front-end and the digital feedback.

Figure 6 shows the micrograph of the IC implemented in a standard 1P8M $0.13\mu m$ CMOS technology. It occupies an area of 2.9×3mm^2 and has an array of 7x8 neural recording channels plus one test channel. The total system power dissipation is about 1.07mW from a 1.2V supply.

B. In Vivo EEG Recording Results

The integrated circuit was validated in on-line in vivo experiments in a freely moving Wistar rat. Three depth electrodes were implanted into the hippocampus and the frontal lobe of a rat, with two electrodes connected to the inputs of two channels of the neural recording integrated circuit and the third one acting as a reference electrode, connected to 0.6V reference voltage. The amplifier was programmed for a bandwidth of 5Hz to 5kHz. Figure 7 shows normal intracranial EEG (low-amplitude high-frequency activity) recorded from the right frontal lobe (top) and right hippocampus (bottom) in awake rats.
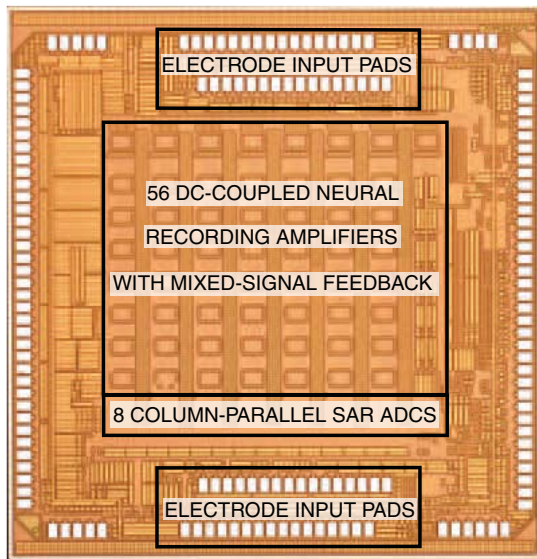
Fig. 6. The die micrograph of the 3mm×2.9mm 0.13μm CMOC neural recording interface.

Fig. 7. Intracranial EEG experimentally recorded from the right frontal lobe (top) and right hippocampus (bottom) in awake Wistar rats.

TABLE I. IC EXPERIMENTALLY MEASURED CHARACTERISTICS

System	
Technology	0.13μm CMOS
Supply Voltage	1.2V
Die Dimensions	2.9mm×3mm
No. of Recording Channels	56
Area per Channel	150μm×120μm
Power Dissipation	1.07mW
Front-end	
Typical Gain	52dB
Gain Mismatch	50.7-54dBdB
Low-Frequency Cut-off (programable)	1-400Hz
Typical High-Frequency Cut-off	5kHz
High-Frequency Cut-off Mismatch	3-6.5kHz
Input-Referred Noise	5μV
Power Dissipation (per 1 ADC)	9.9μW
NEF	7
CMRR	65dB
THD (at 0mV offset)	0.95%
ADC	
Resolution	8-bit
SNDR	41.4dB
ENOB	6.6 bits
Power Dissipation	2.6μW
Input Range	600mVp-p

IV. CONCLUSION

A 0.13μm CMOS DC-coupled digitally-assisted chopper-stabilized neural recording IC is presented. The die integrates 56 compact fully differential DC-coupled neural amplifiers with 8 column-parallel differential SAR ADCs. Input DC offset is canceled by a mixed-signal feedback configuration. The integration area is reduced by 80 percent compared with an equivalent AC-coupled implementation. Additionally, DC input coupling allows for direct input signal chopping without the overhead of large noise multiplication compensating capacitors and extra circuitry. The input DC offset is canceled at the folding node of the OTA to provide noise independence of the input offset. Filtering the low frequency signal in the digital domain provides a well-defined high-pass pole which m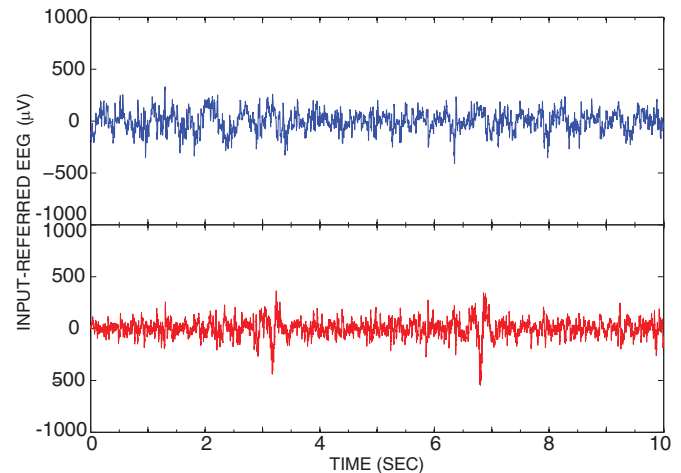akes the design less prone to non-linearity. The total power dissipation of the integrated circuit is 1.07mW from a 1.2V supply. The integrated circuit has been validated in vivo in online intracranial EEG recording in freely moving rats.

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