Wearable Low-Latency Sleep Stage Classifier

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Abstract—A wearable microsystem for low-latency automatic sleep stage classification and REM sleep detection in rodents is presented. The detection algorithm is implemented digitally to achieve low latency and is optimized for low complexity and power consumption. The algorithm uses both EEG and EMG signals as inputs. Experimental results using off-line signals from nine mice show REM detection sensitivity and specificity of 81.69% and 93.83%, respectively, with a latency of 39μ s. The system will be used in a non-disruptive closed loop REM sleep suppression microsystem to study the effects of REM sleep deprivation on memory consolidation.

I. INTRODUCTION

Neurodegenerative diseases affect millions of people worldwide. One of the most common types is Alzheimer's Disease, affecting approximately 5.9 million people only in North America [1]. Epidemiological studies have discovered that excessive REM sleep is a potential risk factor for Alzheimer's disease [2]. Sleep is dominated by cyclic occurrences of SWS (slow-wave sleep) and REM (rapid eye movement) sleep. During SWS, also known as non-REM (NREM), active consolidation of memory takes place by reactivation of newly encoded memories, which are then integrated into the existing network of associated memories. However, the conclusion of REM sleep wakes up the subject and these repeating awakenings, disrupt the memory consolidation process [3]. A recent study demonstrates that antidepressant drugs suppress REM sleep and do not impair consolidation of procedural memory [4]. However, many patients have systemic side-effects and some are drug-resistant. These poor outcomes and adverse effects of the drugs provide motivation for an alternative treatment for REM sleep suppression to supplement conventional options.

Using a wearable/implantable device capable of neural recording, real-time REM sleep stage detection, and stimulation to supress it without disrupting memory consolidation is a promising therapeutic option for the treatment of Alzheimer's disease due to the lower risk of systemic side effects (Fig. 1). To stimulate efficiently for REM sleep suppression, detection latency has to be minimized. This motivates for an FPGAbased digital implementation to avoid long delays caused by data acquisition modules that are required for software-based implementations.

Over the last few years, several mathematical models have been developed for sleep stage classification and implemented on computers for off-line data processing [5-8]. Benefiting from heavy computational schemes, these models succeed to increase detection accuracy and reduce false detections. However, due to the high level of complexity and power consumption, a hardware implementation is not feasible for them. Recently, a few electrocardiogram (ECG) based algorithms implemented in FPGA have been reported [10-12]. The ECG based algorithms either only classify between awake

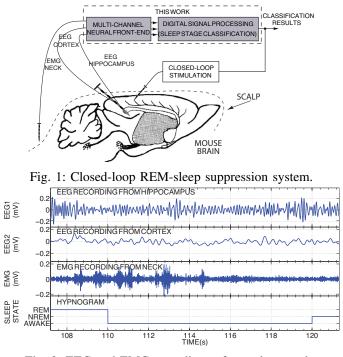


Fig. 2: EEG and EMG recordings of one sleep cycle.

and sleep, or have reported much lower accuracy results of awake, NREM, and REM sleep stage classification compared to electroencephalogram (EEG)/electromygram (EMG) based algorithms [7-9]. Moreover, the best experimentally measured detection latency is 790 ms which is too long for the presented application.

In this work, we have investigated three high performance REM sleep detection algorithms and validated them using our intracerebral EEG (icEEG) and EMG recordings from nine mice. All of these algorithms are based on band-pass filtering of EEG and EMG recordings, followed by performing mathematical functions and thresholding. Fig. 2 shows filtered EEG and EMG signals corresponding to one sleep cycle. θ (5-10 Hz) oscillations from the filtered hippocampus EEG are most prevalent during REM sleep and awake stages, and δ (1-5 Hz) oscillations from the filtered cortex EEG are found during NREM sleep. EMG high frequency (100-200 Hz) oscillations can be used to classify the awake stage. The REM sleep detection sensitivity, specificity and accuracy were evaluated and the best performing algorithm was further implemented in a hardware description language for implementation on an FPGA assembled together with multi-channel recordings and stimulation micro-chip on a small PCB. The algorithm was further optimized to reduce hardware resources and power consumption. The implemented device was validated using off-line icEEG and EMG data from nine mice. The detection

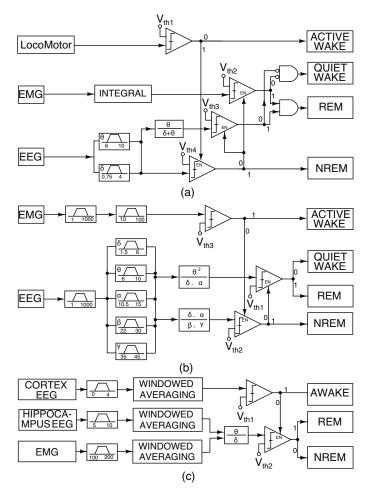


Fig. 3: Block diagrams of three sleep classification algorithms.

performance of the algorithm and the implemented device were compared to the state of the art.

The rest of the paper is organized as follows. Section II introduces the animal data collection method and describes three algorithms that have been tested in software. Digital implementation and power/resource optimization of one of the algorithms is presented. Section III presents the classification results for both software and hardware implementations and compares them with the state of the art. Section IV concludes the paper.

II. METHODS AND MATERIALS

A. Data Collection

1) Animals: Nine male C57 mice (from Charles River Lab, Quebec, Canada) were used in the experiments. The entire experiment was reviewed and approved by the animal care committee of the Douglas Health Institute (Montreal, Canada) according to the Canadian Guidelines for Animal Care.

2) Surgery: Mice were anesthetized with isoflurane and oxygen, and placed in a stereotaxic frame for tetrode (platinum-iridium wire) implantation in the hippocampus. The tetrodes were implanted chronically into CA1 regions using the stereotaxic micromanipulator apparatus. Two EMG electrodes (tungsten wires) were inserted into the neck musculature for postural tone recording. Following the implantation, dental cement was applied to secure the implant to the skull.

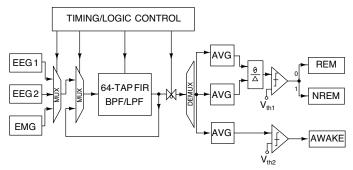


Fig. 4: Block diagram of algorithm's hardware implementation.

3) In vivo intracerebral recording: The icEEG and EMG were recorded with 16 kHz sampling rate using the headstage pre-amplifier for 24 hours a day, 5 days a week. Following the recordings, sleep stages were scored manually by an expert.

B. Sleep Classification Algorithms

Three algorithms were considered and tested for the implementation of the sleep classification system. All of them use EEG and EMG signals for analysis, and have low computational complexity, using only filtering and thresholding for classification.

1) Algorithm I: The first algorithm, as shown in Fig. 3(a), uses a locomotor, EEG, and EMG signals. Three channels are used due to similar θ -band EEG activity during awake and REM stages which makes them indistinguishable using only EEG. The power spectrum of the EEG signal is analyzed using FFT with a Hanning window to extract delta and theta waves. Comparing the magnitude of the delta wave, the ratio of $\theta/(\delta+\theta)$, and the integral of the EMG signal to different threshold values, the system classifies NREM, REM, active wake, and quiet wake stages.

2) Algorithm II: This algorithm is shown in Fig. 3(b). The EMG signal is filtered and compared against a threshold value to classify the active wake stage, characterized by high EMG activity. The EEG signal is also filtered to obtain δ , θ , α , β , and γ band components. Two ratios are calculated and compared with their respective thresholds to classify NREM, REM, and quiet wake stages.

3) Algorithm III: In the third algorithm, as seen in Fig. 3(c), three signals are acquired: one EEG signal from the hippocampus, one EEG signal from the cortex, and one EMG signal from a neck muscle. The EEG from the cortex is filtered to obtain the δ band, and the EEG from the hippocampus is filtered to obtain the θ band. The filtered signals are passed through a Windowed Averaging block. A ratio of the two EEG signals (θ/δ) is then taken and compared with its corresponding threshold value to distinguish between NREM and REM sleep. The EMG signal is also compared against its threshold value for awake stage detection.

C. Hardware Implementation

As mentioned earlier, the algorithm must be implemented in hardware to avoid delays due to data acquisition. This is mainly to avoid loss of data and triggering on-time stimulation for treatment. The trade-off will be limited resources available for hardware implementation compared to the computation power of the computer. As a result band-pass/low-pass filter performance cannot be ideal as in MATLAB. For hardware

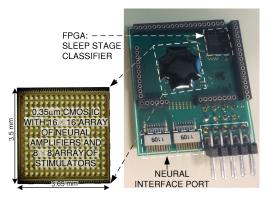


Fig. 5: The 30 mm x 22 mm PCB assembly of FPGA and the closed-loop neurostimulator IC.

implementation, FIR filters were chosen over IIR filters due to the fact that IIR filter coefficient values are very sensitive and a small difference could affect its performance significantly. Minimum of 64 taps are chosen for FIR filter implementation (based on MATLAB simulation results) to achieve the same level of accuracy, sensitivity and specificity.

Synthesis and fitting analysis showed that among all the blocks, the FIR filter used the most number of gates. To reduce resource consumption, a single filter (with variable coefficients) was time-shared between three input channels. This was possible since the clock frequency of the FPGA (40 MHz) was much higher than the sampling rate of the input signals, and no data loss could have occurred. Additionally, to further improve filtering performance and hence detection accuracy, every channel was filtered twice using the same filter. A block diagram is shown in Fig. 4 depicting how the input channels are sharing and reusing the FIR filter. A control block sends appropriate commands to control signal flow and timing of each block. For the averaging filter, every channel has a dedicated filter but the same filter-sharing technique is used to low-pass filter all channels with a single 64-tap FIR filter.

The hardware was assembled in a 30 mm x 22 mm PCB (Fig. 5). The neural signal recording core and stimulation driver was implemented and fabricated in a CMOS 0.35 μ m process and occupied 12.8 mm² of silicon area. Fig. 5 shows photographs of the fabricated chip assembled in the PCB and the zoom inset of the figure shows the fabricated chip [13]. This chip has 256 recording and 64 stimulation channels, three and one of which, respectively, are reserved for the presented application. The PCB has a small low-power FPGA to provide clocks and control signals to the chip and perform data processing for sleep stage classification. Power consumption of each recording and stimulation channel is 13.9 μ W and 2.6 μ W respectively.

III. RESULTS

A. Detection performance of the algorithms.

Output of three MATLAB-based algorithms are shown in Fig. 6. The first and second plots show the two EEG signals from the hippocampus and the cortex respectively. The third plot shows the EMG signal from the neck. The fourth plot is the Hypnogram, which is the result of manual sleepstage scoring and is the reference against the output of the system. The remaining three plots show the outputs of the three algorithms. The accuracy, REM detection sensitivity, and specificity are defined to evaluate each algorithm's performance and compare it to the state of the art as follows: True

TABLE I: Comparison with existing software-based methods

| Ket. | Stages classified | Signals used | Method | Accuracy (%) | Sensitivity (%) | Specificity (%) | Dataset |
|------------|---------------------------------------|-----------------------------------|--|--------------|-----------------|-----------------|-------------|
| [5] | W,REM, S1,S2, SWS | EEG | TFI, MC-LS-SVM | 92.9 | N/R | N/R | 8 adults |
| [6] | W, REM+S1, S2,SWS | EEG | ANN,Wavelet packet coeff. | 93.0 | 84.2 | 94.4 | 7 adults |
| [7] | W,REM, TR,NREM | EMG, EEG | Filtering+ thresholding | 80.2 | N/R | N/R | 6 rats |
| [8] | W,REM, NREM | ECoG, THETA channel, EMG | SVM | >96 | N/R | N/R | 6 rats |
| [9] | Active W, Quiet W, REM, NREM | EEG, EMG | Filtering+ thresholding | 87.9 | N/R | N/R | 14 rats |
| Method I | W, REM, NREM | EEG, EMG | motion sensing+ FFT+ thresholding | 82.34 | 71.02 | 96.40 | 9 mice |
| Method II | W, REM, NREM | EEG, EMG | multi-band FFT+ thresholding | 72.54 | 66.75 | 84.30 | 9 mice |
| Method III | W, REM, NREM | EEG, EMG | multi-band filter+ thresholding | 81.82 | 84.69 | 97.81 | 9 mice |

N/A: Not applicable

N/R: Not reported

positives (TP): the number of discharge events following the detection of the putative discharge precursor. False positives (FP): when a discharge event does not follow the detection of the discharge precursor. True negatives (TN): the absence of discharge activity correctly identified as non-discharge. False negatives (FN): the discharges that occurs without detection of the discharge precursor. Sensitivity: the ratio of TP to TP + FN. Specificity: the ratio of TN to TN + FP.

To further optimize the algorithm, the windowed averaging block was designed for optimal REM sleep detection. The length of the window used is a trade-off between REM detection sensitivity and specificity. A longer window allows a larger portion of the signal to be analyzed, increasing the specificity of the detection, while a shorter window increases the sensitivity of the detection. In Fig. 7, the relationship between window size and accuracy, sensitivity, and specificity is shown. The average value of the three measures was used for overall performance optimization which results in a window size of 8 seconds. The filter order chosen for the three filters was optimized to maximize performance and minimize power and resource consumption. Increasing the filter order improved results; however it increased implementation complexity. A filter order of 4 was chosen as the optimal parameter.

All three algorithms were initially implemented and tested in MATLAB with the same data set. Their results can be compared in Table I. The third algorithm was chosen for hardware implementation because of its low complexity and good performance for REM detection sensitivity and specificity.

B. Detection performance of the hardware

The algorithm was implemented on an Actel ProASIC3 FPGA and tested with data from 9 different mice. Fig. 8 shows a sample output of the FPGA implementation for a 9 minute recording, compared with the reference hypnogram. The system needs 1562 clk cycles for every sample to generate

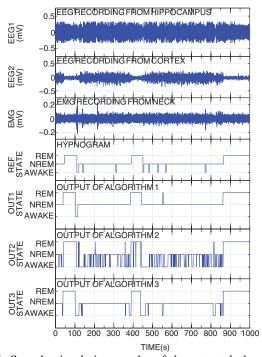


Fig. 6: Sample simulation results of three tested algorithms.

an output which translates into 39 μ s using a 40 MHz FPGA clock. Table II shows the accuracy, sensitivity and specificity of our implementation compared with other hardware-based implementations. As shown, the latency is significantly lower than other works, while accuracy, sensitivity and specificity are quite comparable.

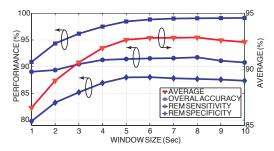


Fig. 7: Effect of averaging window size on sensitivity, specificity and accuracy of REM-sleep detection.

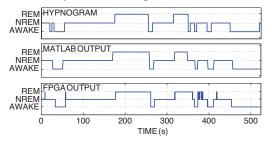


Fig. 8: Sample output results of FPGA implementation.

IV. CONCLUSION

A low-latency, area-efficient microsystem for sleep stage classification and REM sleep detection is presented. EEG and EMG signals are processed and used to classify REM, NREM, and awake stages. The FPGA implementation was optimized to

TABLE II: Comparison with existing hardware-based methods

| Ref. | [10] | [11] | [12] | This work |
|-----------------------|------------------|-----------------------------|---------------------|----------------------------|
| Stages classified | W, Non-wake | W, S1,S2, SWS, REM | W, Sleep | W, REM, NREM |
| Signal(s) used | ECG | ECG | ECG, Resp. | EEG, EMG |
| Method | Random forest | FNGLVQ | FFT, PSD, ANN | Filtering+ thresholding |
| Accuracy (%) | N/R | 68.8 | 77.8-89.0 | 81.66 |
| Sensitivity (%) | 94.2 | N/R | N/R | 81.69 |
| Specificity (%) | N/R | N/R | 91.9 | 93.83 |
| Computation time (ms) | 20k | 790 | 3.75 ¹ | 0.039 |
| Real-time | Yes | No | N/A | Yes |
| Order of filter | 3 | N/A | N/A | 64 |

N/A: Not applicable N/R: Not reported

¹ Estimated value. Algorithm not implemented due to high power consumption.

reduce complexity and power consumption while maximizing REM sleep detection performance. Experimental results show a REM detection sensitivity and specificity of 81.69% and 93.83% respectively. A low latency of 39 μ s has been achieved. This is a critically important design requirement for a closed-loop sleep control system. The system is used for studies to determine the effects of REM sleep suppression on memory consolidation.

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