256-site Active Neural Probe and 64-channel Responsive Cortical Stimulator

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***Abstract*— The 0.35μm CMOS active probe and stimulator enables responsive neural stimulation of the brain cortex. It monitors extracellular neural activity on 256 sites in the brain and generates 64 event-triggered current-mode neural stimuli. Each 0.035mm^2 fully differential neural recording channel includes a 8-bit single slope ADC. Each 0.02mm^2 neural stimulation channel reuses an OTA for both current sampling and current sourcing. The 13.5mW prototype is flip-chip bonded with a 64-shank Utah electrode array and validated in spatial recording of epileptic neural activity in the mouse hippocampus.**

I. Introduction

Neural stimulators are widely utilized to treat such debilitating neural disorders as epilepsy and Parkinson's disease. Conventional implants modulate electrical activity in the brain continuously even when it is not needed. This significantly increases implant size, shortens its lifetime and often leads to suboptimal efficacy of treatment. Responsive neural stimulation offers a promising solution to these problems. A stimulus is applied only when a neurological event of interest is detected. For example, in some intractable epilepsy patients responsive electrical stimulation before the onset of a seizure often prevents the development of the seizure [1]. Responsive neural stimulation requires both neural activity monitoring and neural stimulation. Neurological disorders exhibit neural behaviors that often span large areas of the brain, such as the cerebral cortex, with sub-mm spatial scale. This necessitates wide and fine-grained spatial coverage of the brain both when recording and when modulating neural activity.

Figure 1 illustrates the multi-site responsive cortical neural stimulation system. Several multi-electrode modules are implanted onto the cortex. Each module combines a microelectrode array known as Utah electrode array (UEA) and a neural recording and stimulation integrated circuit flip-chip bonded onto the array. This active probe integration eliminates bulky and noisy wires conventionally used to connect to UEAs. The modules bidirectionally interface with an implanted digital signal processing and data communication unit. Energy is delivered to the implant inductively through the skin. In this paper we present the design of the neural recording and stimulation module.

II. System Description

The VLSI architecture of the system is shown in Figure 2.

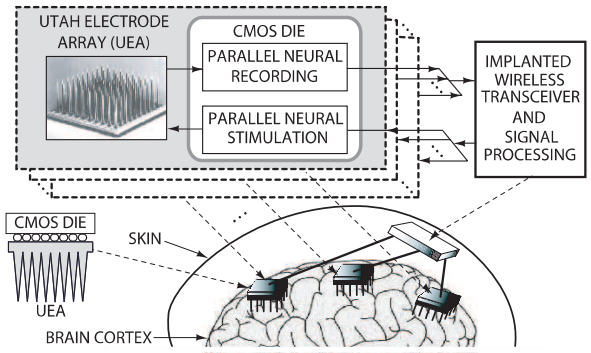

Fig. 1. Implantable responsive neural stimulation system.

A. Neural Recording

An array of 256 recording channels performs bandpass filtering, amplification, sampling and analog-to-digital conversion. Each channel is fully differential to reduce the common mode noise that results from a dense integrated circuit organization. Distributing the gain over two stages lowers capacitor sizes and maintains high linearity. The feedback resistors are implemented as PMOS transistors operating in deep subthreshold region to obtain large resistance [2]. The overall gain is programmable from 54dB to 72dB.

Various OTA topologies have been used for the implementation of neural amplifiers: folded cascode, current mirror and two stage [3]–[6]. As the gain is distributed over two stages a wide output swing topology for the first stage OTA is not needed. The telescopic OTA saves power in the first stage while maintaining low input-referred noise level. The fully differential telescopic OTA of the first stage and its common mode feedback circuit (CMFB) are shown in Figure 3(a). To minimize the thermal noise contribution, transistors $M_{1,2,7,8}$ have to be biased such that $g_{m7,8} << g_{m1,2}$. Reduction in $1/f$ noise is achieved by choosing the input transistors to be of the PMOS type which have a lower $1/f$ noise coefficient than NMOS transistors ($K_P < K_N$), and maximizing the gate area of these transistors. In the design of the second stage OTA a higher noise level can be tolerated due to signal amplification in the first gain stage, however a wide output swing is important to lower distortion due to the feedback PMOS transistor. A folded cascode OTA was chosen for the

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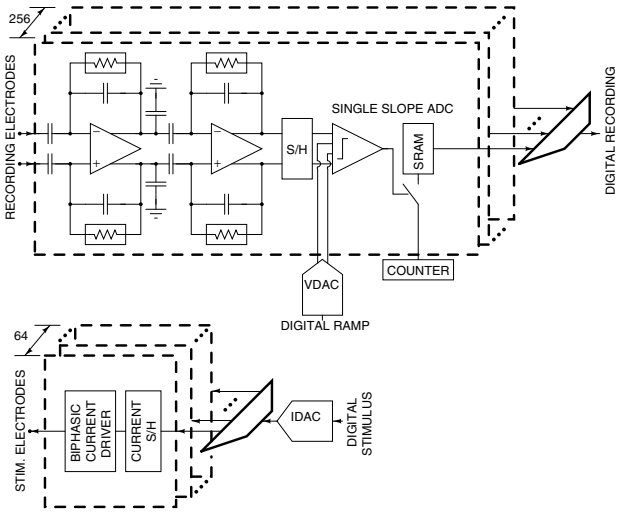

Fig. 2. VLSI architecture and circuit implementation.

second stage with a total bias current of 1.5μA, which is almost half of the first stage bias current. The schematic of the folded cascode OTA and its CMFB circuit is shown in Figure 3(b).

B. In-channel ADC

The architecture of the in-cell fully differential single-slope ADC is shown in Figure 2. Considering the amplitude of the neural signals and the background noise at the recording site, an ADC with 8-bit resolution is sufficient for this application. The quantization of the recorded sample is performed simultaneously on all channels. This allows for rapid parallel evaluation of the entire frame of data. The in-channel ADC consists of a fully differential comparator and an 8-bit SRAM block. Both the ramp generator and the counter are common to all ADCs as quantization is taking place simultaneously on all channels.

C. Neural Stimulation

The memory in each of the 64 neural stimulation channels allows for simultaneous stimulation on multiple channels. A single off-chip current-mode DAC preloads a stimulus value for each channel into its current-mode sample-and-hold circuit. Next, a biphasic current driver array delivers all stimuli to the tissue at the same time. The sample-and-hold circuit and the current driver reuse a single OTA as shown in Figures 4(a,b) [7]. When a current is stored (Figure 4(a)), the circuit is configured as a current copier. The gate voltage of $M1$ corresponding to the input current is stored on C_{mem}. Figure 4(b) shows the circuit configured as a regulated-cascode current driver delivering a current equal to the stored current. Area is saved as only one OTA per channel and one DAC for all channels are used.

D. Integration with Utah Electrode Array

Figure 5(a) shows a prototype fabricated in a standard 0.35μm double-poly CMOS technology. The 3.5mm x

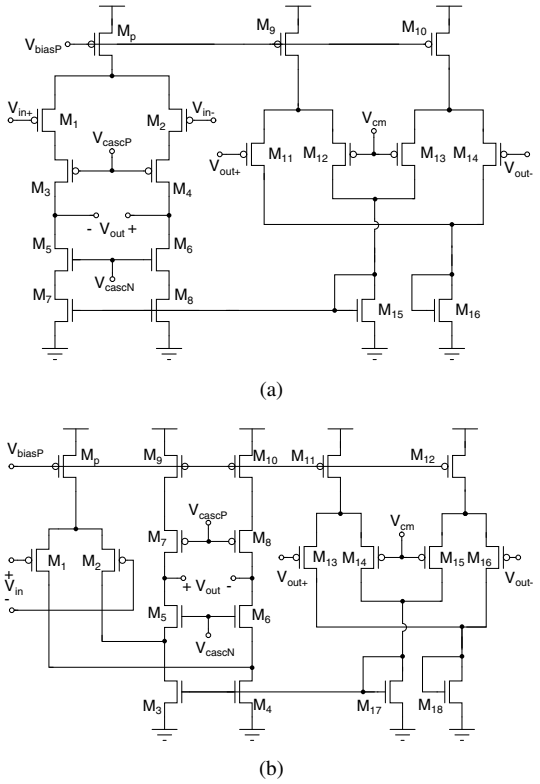

Fig. 3. (a) Telescopic amplifier in the first stage of the recording channel. (b) Folded-cascode amplifier in the second stage of the recording channel.

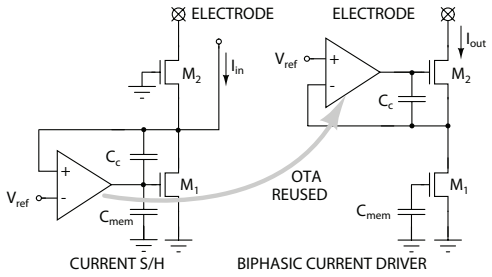

Fig. 4. Circuit implementation of the neural stimulator. (a) Current storing phase, and (b) current driver phase.

3.65mm die consists of an array of 16×16 neural recording channels organized on a 200μm-pitch grid and interleaved with an array of 8×8 neural stimulator channels. Bonding pads for the tissue I/O signals are also arranged on the same grid. Each bonding pad is connected to a recording channel input. One of every four pads is connected to a neural stimulator channel output. This results in a 400μm pitch of stimulation electrodes. This pitch is chosen to match that of the Utah electrode array (UEA) for direct bonding of a microelectrode array onto a CMOS die as shown in Figure 5(b). The stimulation channels time-share 64 UEA shanks with 64 recording channels. The remaining 192 recording channels are available for connection to additional off-chip electrodes such as ECoG microgrids for greater spatial coverage of the brain cortex.

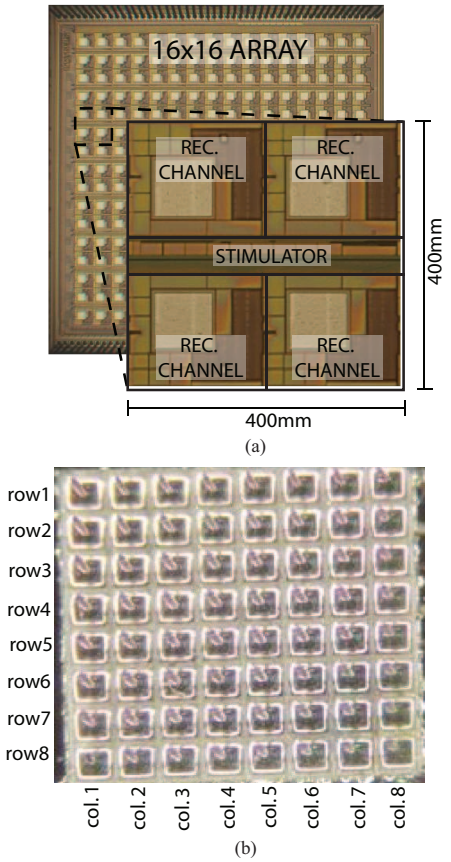

Fig. 5. (a) Micrograph of the 0.35μm CMOS prototype. (b) Top view of a Utah electrode array (UEA) bonded onto the CMOS die. UEA shanks connect to every fourth recording channel and each stimulation channel.

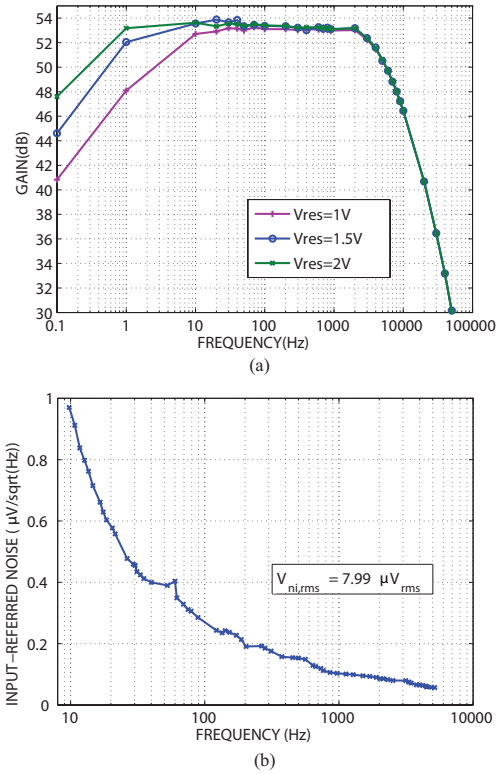

Fig. 6. (a) Experimentally measured amplitude frequency response of the neural amplifier. (b) Experimentally measured noise of the neural amplifier.

III. Experimental Results

The experimentally measured amplitude frequency response of the two filtering and amplification stages is shown in Figure 6(a). The gain was set to the minimum and the high-pass corner frequency was adjusted by changing the bias voltage of the feedback PMOS transistors, V_{res}. The plot of the experimentally measured input-referred noise of the two stages is shown in Figure 6(b). Integrating the noise over the bandwidth of 10Hz-5kHz results in the overall input-referred noise of 7.99μV_{rms}. The NEF of the fully differential recording amplifier is 8.9, while the CMRR is 60dB at 200Hz. The recording channel including the amplifier and ADC dissipates 52μW per channel.

The neural stimulator delivers an output current in the range from 20μA to approximately 250μA as shown in Figure 7(a). The output current for various resistive loads is depicted in Figure 7(b). The neural recording and stimulation channels occupy only 0.035mm^2 and 0.02mm^2 respectively. The full system dissipates 13.5mW from a 3.0V supply. The quiescent power dissipation for the neural stimulation is 2.6μW per channel or 166μW for all 64-channels. The non-quiescent neural stimulation power dissipation is additional and is stimulus-dependent. Table I summarizes the experimental characteristics of the prototype. Table II compares several existing parallel

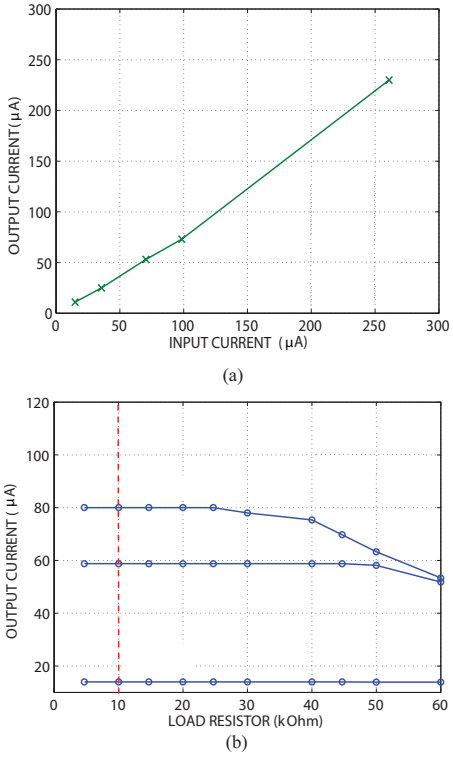

Fig. 7. (a) Experimental neural stimulator transfer characteristic. (b) Experimental neural stimulator output current for a varying load.

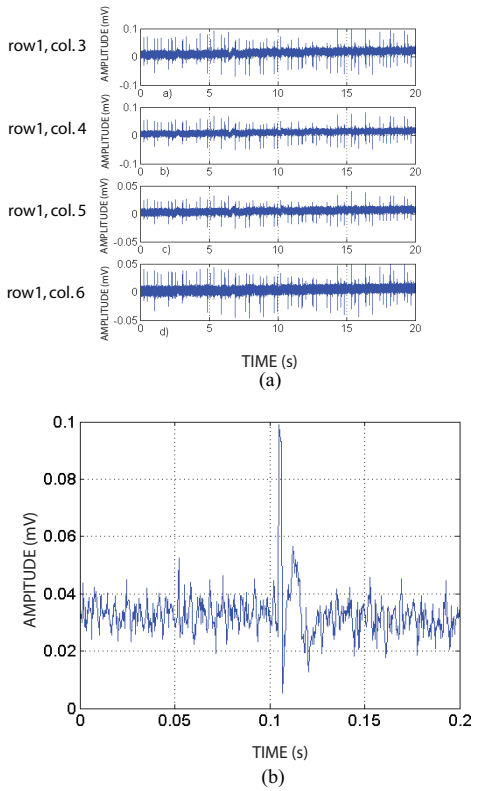

Fig. 8. (a) Neural activity in a mouse hippocampus recorded by the chip through four on-chip UEA electrodes. (b) One neural spike from (a).

integrated neural recording and stimulation interfaces with the presented design. The CMOS prototype bonded with a 64-shank Utah electrode array was validated experimentally in recording epileptic neural activity in a mouse hippocampus in vitro. An intact hippocampus was placed onto the electrode array bonded onto the CMOS die and perfused. A low-glucose perfusing solution was used to invoke epileptic activity. Recorded epileptic neural spikes on four selected channels out of 64 are displayed in Figure 8(a) with a zoomed-in neural spike shown in Figure 8(b).

IV. Conclusion

A 0.35μm CMOS bidirectional integrated neural interface for responsive stimulation is presented. The die integrates 256 fully differential neural recording channels, each with an in-channel ADC, and 64 neural stimulation circuits. A Utah electrode array was bonded directly to the die and validated in a mouse hippocampus neural recording in vitro. The total power dissipation of the chip is 13.5mW.

TABLE I

Experimental Characteristics

System	
Technology	0.35μm CMOS
Supply Voltage	3.0V
Die Dimensions	3.5mm×3.65mm
No. of Recording Channels	256
No. of Stimulation Channels	64
Power Dissipation	13.5mW
Neural Amplifier	
Programmable Gain	53-72dB
Low Frequency Cut-off	0.5-50Hz
High Frequency Cut-off	500Hz-10kHz
Input-Referred Noise	7.99μV
NEF	8.9
CMRR (200Hz)	60dB
THD (1mV_{pp})	0.8%
Recording Channel (including ADC)	
Resolution	8-bit
Power Dissipation	52μW
SNDR	32.18dB
SFDR	38dB
Stimulation Channel	
Quiescent Power	2.6μW
Output Current	20-250μA

TABLE II

Integrated Neural Recording and Stimulation Interface Arrays

Spec.	[5]	[8]	THIS WORK
# Rec. Chan.	128	8	256
Fully Diff.	Yes	No	Yes
Gain	70dB	40dB	54-72dB
ADC	SAR	Log	S. Slope
ADC Res.	8-bit	8-bit	8-bit
Power/Chan.	160μW	9μW	52μW
# Stim. Chan.	128	64	64
Stim. Mode	Voltage	Current	Current
Stim. Curr.	up to 10mA	3-135μA	20-250μA
CMOS Tech.	0.6μm	0.18μm	0.35μm
On-die Electrodes	2-D	N/A	3-D

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