915-MHz Wireless 64-Channel Neural Recording SoC with Programmable Mixed-Signal FIR Filters

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***Abstract*— A system-on-chip (SoC) neural recording interface with 64 channels, 64 16-tap programmable mixed-signal FIR filters and a fully integrated 915MHz OOK/FSK closed-loop wireless transmitter is presented. Each recording channel has a fully differential amplifier with 54dB of gain and utilizes a tunable low-distortion subthreshold MOS-resistor to reject DC offsets with an input-referred noise of 6.5μV and a CMRR of 78dB. Each channel contains a modified 8-bit SAR ADC with an ENOB of 7.8-bits and can provide analog-digital multiplication by modifying the the sampling phase of the ADC. It is used in conjunction with 12-bit digital adders and registers to implement 64 programmable transposed FIR filters that enable precise separation of various bands in the neural spectrum. The 915MHz FSK/OOK transmitter offers data rates up to 1.5Mbps with a maximum output power of 0dBm. The 4x3mm chip fabricated in a 0.13μm CMOS process dissipates 5.03mW from a 1.2V supply.**

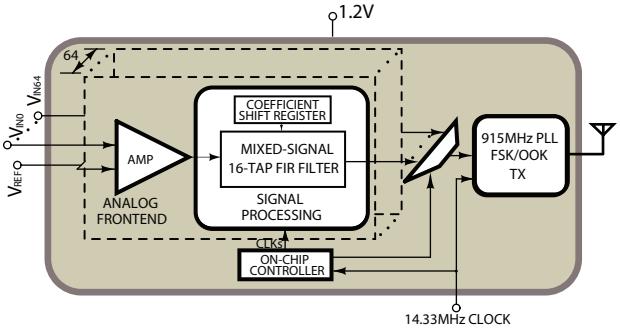

Fig. 1. Simplified system diagram of the wireless neural recording SoC.

I. Introduction

Monitoring neuro-electrical activity in the brain is a vital method in diagnostics and evaluation of various neurological disorders. A number of non-invasive techniques can be used for brain function testing such as EEG, MEG, fMRI and PET scans. These methods are complementary and often have limited efficacy and applicability. Cortical surface electrical recordings known as electrocorticography (ECoG) provide better signal-to-noise ratio than scalp surface EEG, as well as a higher bandwidth, up to 500Hz of signal content, and increased spatial resolution. 64-site ECoG is currently the gold standard procedure for seizure localization in most patients with intractable epilepsy who are candidates for resective surgery. Other invasive methods include neural recording from microelectrodes, such as Utah electrode arrays employed in experimental animal and human studies, which allow for recording signals with even wider bandwidths and for monitoring action potentials of individual neurons. Currently most of these methods involve tethered wires connecting the electrodes to bench-top neural amplifiers.

An implanted RF wireless interface enables the freedom of movement for a patient, reduces artifacts and noise in the recording data and reduces the possibility of an infection. The requirements of a large number of recording channels and wide signal bandwidth translate to a high output data rate (>1Mbps). Tissue heating and available power budget severely limit the transmitter output power. Existing designs overcome this limitation by transmitting only neural spikes on most or all channels [1], [2] and by utilizing simple low-power transmitter architectures [1], [3]. Spike detection results in a loss of vital information such as neural oscillations in the gamma band present in patients with epilepsy, schizophrenia, Alzheimer's disease and many other neurological disorders. Simple transmitter architectures have shortcomings and are typically not fully integrated. Open-loop VCO designs [1], [3] suffer from temperature sensitivity and frequency drift. Basic UWB architectures [4] are susceptible to interference and noise.

We present an integrated 64-channel neural recording interface system-on-chip (SoC) that densely integrates 64 neural recording amplifiers and ADCs, 64 programmable 16-tap FIR filters, an on-chip digital controller and a fully-integrated closed-loop wireless transmitter on a 4mm×3mm 0.13μm CMOS die. It performs versatile signal filtering individually configurable for each channel to extract information of interest such as beta, gamma or other frequency bands, local-field potentials (LFP) and spikes. It also performs interference suppression, spike detection, precise bandwidth control and a variety of other filtering tasks. A mixed-signal FIR filter implementation eliminates the need for 512 conventional 8-bit digital multipliers by efficiently implementing the multiplication within an ADC conversion cycle. This results in over an order of magnitude savings in the power-area product.

II. System Architecture and VLSI Implementation

The full system architecture is shown in Figure 1. It consists of 64 neural recording amplifiers with a tunable high-pass pole frequency in the sub-Hz range. Each channel contains a programmable mixed-signal 16-tap FIR filter. Digital data is sent to the 915MHz PLL-based transmitter and modulated using either Manchester encoded FSK or OOK. The transmitter output power, FSK modulation index, VCO center frequency

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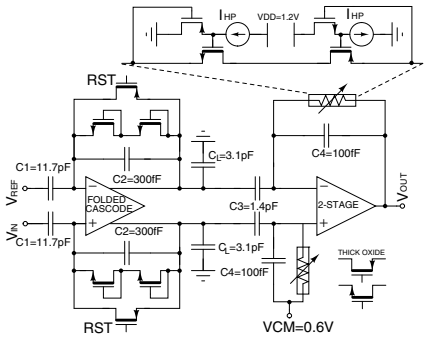

Fig. 2. Schematic of the analog front end.

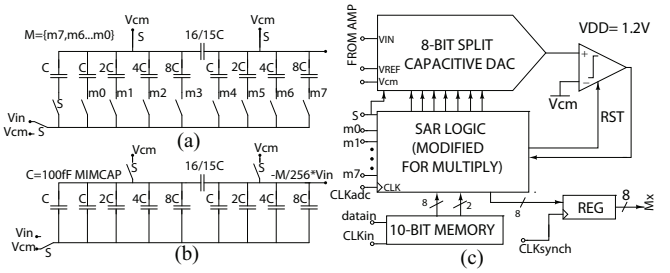

Fig. 3. (a) Sampling phase of multiplying SAR ADC. (b) Hold phase of multiplying SAR ADC. (c) Schematic of in-channel multiplying SAR ADC.

and the PLL bandwidth can all be programmed. A single off-chip 14.32-MHz crystal oscillator generates all on-chip clocks.

A. Analog Front End

The schematic of the analog front end is shown in Figure 2. Amplification and filtering are performed over two stages with 54dB of gain set by the input and feedback capacitor ratios. The first stage uses a fully differential architecture to ensure high CMRR, which is important for dense SoC implementations. The first stage uses a folded-cascode OTA with a total current of 3μA. Large PMOS input devices were selected to minimize flicker noise and are biased in weak inversion to maximize their transconductance. The first stage has a small output swing and uses two thick oxide NMOS pseudo-resistors as feedback elements which along with C_2 yields a high-pass pole in the sub-Hertz region. To maximize output swing, the second stage uses a 2-stage OTA with a total current of 1μA. The pseudoresistor as implemented in the first stage exhibits distortion as it is a non-linear resistance when large output swings are present [1]. It can be made tuneable by setting its gate to a voltage [5] and operating the device in subthreshold. Setting the V_{GS} of the feedback device too low leads to leakage issues and bias drifts often saturating the OTA. To address these issues, the feedback resistor in the second stage was implemented using two source followers to ensure a constant V_{GS} on the subthreshold device for large output swings as shown in Figure 2. A 10-15dB improvement in distortion at sub-Hz frequencies was observed experimentally when using the implemented approach in Figure 2 over the conventional subthreshold transistor when used in the second stage.

B. Multiplying SAR ADC

Each channel can be configured in one of the two modes: raw data analog-to-digital conversion, and FIR filtering. The in-channel ADC is an 8-bit capacitive charge redistribution SAR ADC. The same ADC circuits are reused in both modes. The filtering mode requires the ADC to perform analog-digital multiplication as part of the conversion cycle. The successive approximation register (SAR) ADC architecture can implement such computation with minimal area and power overhead. Analog multiplication within the ADC is introduced by modifying the digital SAR logic to perform multiplication during the sampling phase as shown in Figure 3(a). During the sampling phase, the capacitors in the array are disabled or enabled which is equivalent to performing a multiplication between 0 and 1. The hold phase is similar to a conventional SAR ADC as shown in Figure 3(b). A similar sampling approach was utilized in [6] which requires a modified SAR capacitor array and a modified digital SAR algorithm. The ADC architecture is shown in Figure 3(c) and utilizes a split capacitor array to minimize area and power dissipation. The comparator uses 2-stages with offset correction followed by a digital buffer. The analog-digital multiplication requires only a few extra digital gates in the SAR logic. Each channel includes a 10-bit shift register to store the multiplication and sign coefficients and dissipates 1.8μW at 57kS/s.

C. Mixed-Signal FIR Filter

In the filtering mode a 16-tap transposed FIR filter architecture depicted in Figure 4(a) is employed. Conventionally this architecture requires 64x16 8-bit digital multipliers. This number can be reduced by half due to the symmetry in the filter coefficients $|M_i| = |M_{15-i}|$ for i=0,1,...,15 so only eight filter coefficient absolute values are utilized. We use a bank of eight adjacent channel ADCs to implement this computation in parallel as depicted in Figure 4(b). As shown in Figure 4(c) the outputs of eight LNAs are multiplexed and sampled by eight ADCs in parallel. Each ADC output is fed to two simple digital sign multipliers in the corresponding two slices of the 16-tap add-and-delay line. Eight add-and-delay lines corresponding to the eight input channels are clocked cyclicly. This architecture is tiled eight times for a total effective number of 64 FIR filters. In this mixed-signal FIR implementation the 512 digital multipliers (for 64-channels) as depicted in Figure 4(a) (for 1-channel) are eliminated from the system, while the ADCs are clocked 8 times faster than the in-channel sampling rate. The implemented mixed-signal FIR approach yields 10 times less area and 1.5 times less power dissipation for a savings in the power-area product of 15.

D. Fully Integrated 915MHz FSK/OOK Transmitter

The digital data is transmitted wirelessly using either OOK or FSK modulation and transmits 64 channels of FIR-filtered neural data at 1.5kS/s. The transmitter operates in a closed-loop PLL to prevent the VCO frequency from drifting. The

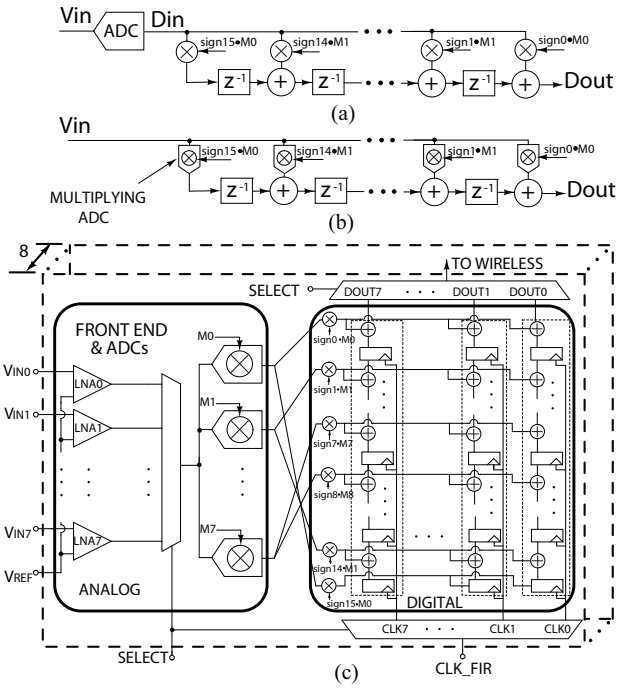

Fig. 4. (a) Conventional 16-tap transposed FIR structure. (b) Mixed-signal 16-tap transposed FIR filter structure. (c) Schematic of implemented mixed-signal 64 16-tap FIR filters.

full wireless transmitter schematic is shown in Figure 5. The voltage-controlled oscillator (VCO) was implemented using a cross-coupled architecture with a 12.6nH on-chip inductor implemented using a thick copper top-level metal. A large varactor implemented using a P+/N junction diode was connected to the control voltage of the VCO to lock the PLL to 916.3MHz. The data is modulated at high bit-rates through Manchester-encoded FSK on the smaller NMOS varactors. They consist of binary-weighted transistors and have 3-bit programming to adjust the FSK modulation index. The bandwidth of the PLL must be significantly lower than the data bit-rate to prevent it from being filtered out by the PLL [7]. The loop filter was implemented on-chip and is tunable to achieve different PLL bandwidths. The output of the VCO is buffered and sent to the power amplifier which utilizes a 12.6nH on-chip inductor and a capacitive matching network to match to a 50-Ohm antenna. The output power has 4-bit digital tuning and is adjustable from -20dBm to 0dBm through P_0 to P_3 in Figure 5. For OOK modulation, the PLL is locked to the carrier frequency and the cascode transistors of the power amplifier are turned ON or OFF.

III. Experimental Results

The experimentally measured amplitude frequency response and input referred noise of a neural recording channel are shown in Figure 6(a) and Figure 6(b), respectively. The high-pass corner frequency can be adjusted from approximately 0.1Hz to 10Hz by adjusting the bias current of the source follower in Figure 2. Integrating the noise over the bandwidth

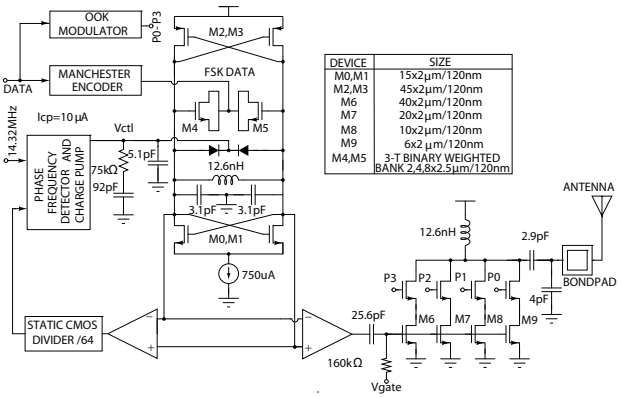

Fig. 5. Schematic of the wireless transmitter.

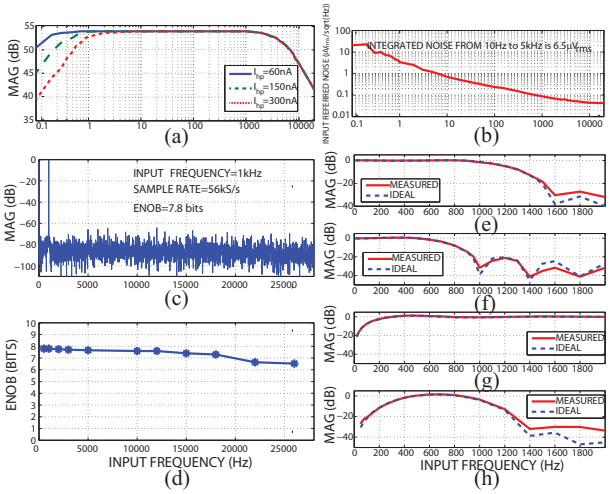

Fig. 6. (a)(b) Measured amplitude response and input-referred noise of the analog front end. (c) FFT of an in-channel ADC output for 1kHz sinusoid input at 54kS/s (d) ENOB vs. input frequency for an in-channel ADC. (e)-(h) Measured filter responses of different FIR filters at 7.1kSps.

of 10Hz to 5kHz results in an input-referred noise of 6.5μV_{rms} and an NEF of 7.2. The CMRR at 1kHz is 78dB.

The experimentally measured ADC performance is shown in Figure 6(c) and (d) with an ENOB of 7.8 and close to 7-bits over the full Nyquist bandwidth when sampled at 54kS/s. Four different 16-tap FIR configurations operating at 7.1kS/s (two different low-pass, one high-pass, and one band-pass filter) are shown in Figure 6(e) to (h) with a very close match between the experimental result and the ideal filter response.

Experimental results for the wireless transmitter are shown in Figure 7. Figure 7(a) shows the spectrum analyzer with 1.2Mbps of Manchester-encoded FSK data and Figure 7(b) shows transmitted and received data at a distance of 1m. Figure 7(c) shows OOK-modulated data on an oscilloscope and Figure 7(d) shows transmitted and received OOK data from a distance of 1m. The full transmitter dissipates 3.7mW and 6.6mW in FSK-mode for an output power of -20dBm and 0dBm, respectively and 5mW for 0dBm OOK modulation.

Figure 8(a) shows the wireless neural recording SoC implemented in a standard 1P8M 0.13μm CMOS technology

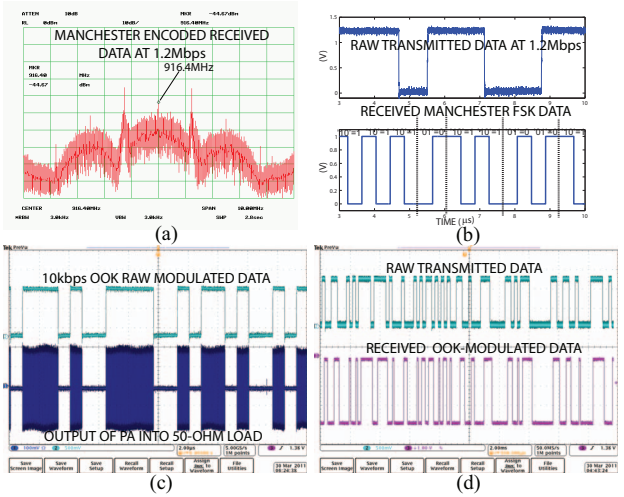

Fig. 7. (a) Spectrum of FSK-modulated data at a 1m distance. (b) Transmitted and received data from 1m distance at 1.2Mbps using FSK-modulation. (c) OOK modulated data into 50-ohm termination and (d) transmitted and received data from a 1m distance at 10kb/s using OOK modulation.

which occupies $4\times3\text{mm}^2$ of area. An array of 8x8 neural recording channels are organized on a 300μm pitch grid to be flip-chip bonded to a 8x8 trace carrier or an electrode array. The power dissipation of the neural recording SoC is 0.8mW for the analog front end, ADCs and biasing, 0.53mW for the digital controller and the adders/registers to implement the FIR filters while operating at 7.1kS/s. The total system power dissipation is 5.03mW from a 1.2V supply when using FSK modulation with a -20dBm output power. A comparison with other wireless neural recording SoCs is given in Table I.

The functionality of the analog front end, ADC and FIR filters was also verified with pre-recorded neural activity of epileptic seizure events. Seizure-like events were induced in an intact hippocampus from Wilstar rats by immersing it in a low-Mg2+ solution. The signals were recorded with a conventional bench-top low-noise amplifier and then programmed onto an arbitrary waveform generator with the original signal as shown in Figure 8(b). The input signal was then contaminated with 60Hz interference with a much larger power than that of the pre-recorded signal as shown in Figure 8(c) and applied to one of the 64 channels on the chip. The FIR filter was programmed with the bandpass filter response shown in Figure 6(h). Figure 8(d) shows the output after the FIR filtering with the neural activity clearly visible and the 60Hz interference removed.

IV. Conclusion

A 0.13μm CMOS wireless neural recording SoC is presented. The die integrates 64 fully differential recording amplifiers with 64 SAR ADCs modified to perform in-channel multiplication. This implements 64 programmable 16-tap mixed-signal FIR filters to perform versatile signal filtering in each channel. A fully integrated PLL-based FSK/OOK transmitter wirelessly sends the digitized neural recorded data at up to 1.5Mb/s. The total power dissipation is 5.1mW from a 1.2V supply.

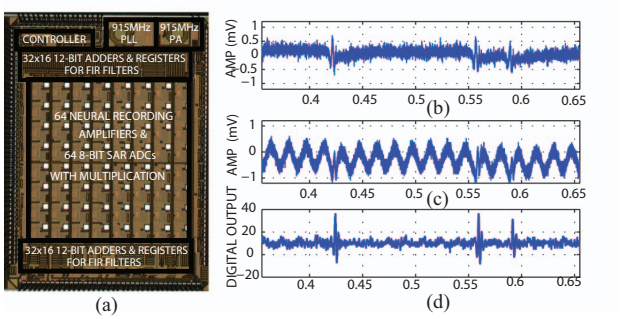

Fig. 8. (a) Micrograph of the $4\times3\text{mm}^2$ 0.13μm CMOS prototype. (b) Original prerecorded neural spike from a rat. (c) The input into the amplifier which includes the signal from (b) and an added 60-Hz interference. (d) Output after the amplifier and ADC/FIR filter programmed to implement a BP filter.

TABLE I

Integrated Wireless Neural Recording SoCs.

Spec.	[1]	[2]	[3]	[4]	THIS WORK
Power Diss.	13.5mW	17.2mW	7.05mW	6.0mW	5.03mW
CMOS Tech.	0.5μm	0.35μm	0.5μm	0.35μm	0.13μm
Area $(\text{mm})^2$	27.3	8.4	16.3	63.4	12
Supply (V)	3.3	3.0	3.0	3.3	1.2
# Rec. Chan.	100	16	32	128	64
Power/ch.	38μW	9μW	75μW	11μW	6.3μW
Gain (dB)	60	60	68-78	57-60	54-60
Noise	$5.1\mu V$	$3.1\mu V$	$9.3\mu V$	$4.9\mu V$	$6.5\mu V$
ADC	1xSAR	1xSAR	PWM	1xSAR	64xSAR
ADC Res.	9b	8b	N/A	6-9b	8b
Sig. Proc.	Spike	Spike	None	Spike	64x16t-FIR
Programmable	No	No	No	Yes	Yes
RF Carrier	433MHz	433MHz	915MHz	3.1GHz	915MHz
Modulation	FSK	FSK	FSK/OOK	UWB	FSK/OOK
Data rate	330kb/s	1.25Mb/s	708kS/s	90Mb/s	1.5Mb/s
PLL	No	Yes	No	No	Yes
Fully Int. TX	No	No	No	Yes	Yes
P_{out}(dBm)	N/A	0	-22	N/A	-20 to 0
P_{DC}(mW)	4.0	16.6	3.3	4.8	3.7 to 6.6

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