64-Channel UWB Wireless Neural Vector Analyzer and Phase Synchrony-Triggered Stimulator SoC

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***Abstract*— A UWB 64-channel responsive neural stimulator is presented. It wirelessly monitors magnitude, phase and phase synchronization of neural signals. Abnormal phase synchrony triggers programmable-waveform biphasic current-mode stimulation in a closed loop. To implement these functionalities, the SoC integrates 64 neural recording amplifiers with tunable switched-capacitor (SC) bandpass filters, 64 multiplying 8-bit SAR ADCs, 64 programmable 16-tap FIR filters, a tri-core CORDIC processor, 64 biphasic current stimulation channels, and a 3.1-10.4GHz UWB wireless transmitter onto a 4mm $\times$ 3mm 0.13μm CMOS die. The SoC dissipates 1.4mW/1.5mW when recording/stimulating and has been validated in early detection and abortion of epileptic seizures in freely moving rodents on-line and in early seizure detection in humans off-line.**

I. Introduction

Abnormal coordinated interactions in various regions of the brain are widely recognized as key indicators of pathological brain states in numerous neurological disorders such as those listed in Fig. 1. Quantifying phase synchronization among neural oscillations is effective for diagnostics, monitoring or treatment of such disorders. For example, in epilepsy large fluctuations of phase synchrony in narrow frequency bands within the neural signal spectrum are among the earliest precursors of an upcoming seizure [1]. Detecting the seizure before it develops is critical in a closed-loop implantable neural stimulator. Chances of aborting a seizure are much higher if responsive electrical stimulation takes place before one fully develops [1]. Previously reported integrated neural interfaces [2]–[6] and commercial neural stimulators currently lack this capability.

We present a wireless 0.13μm CMOS SoC with 64 neural recording channels that performs neural vector analysis and responsive neural stimulation based on phase synchrony. It is the first reported on-chip neural vector analyzer to process not only the magnitude, but also the phase of neural signals. It is also the first SoC to demonstrate real-time on-chip computation of the phase synchrony among neural signals and to demonstrate on-chip closed-loop stimulation based on bivarite signal processing. This approach has shown promise to outperform other methods used in commercially available neural stimulators for epilepsy treatment [1].

II. VLSI Architecture

The functional diagram is depicted in Fig. 1. The loop consists of the neural vector analyzer in the feed-forward path and the phase synchrony-triggered neural stimulator in the

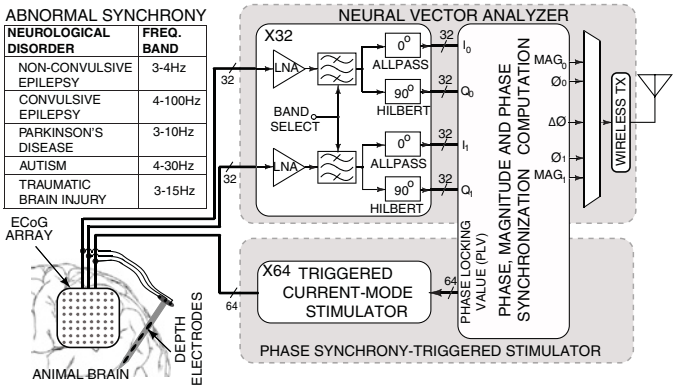

Fig. 1. Frequency bands of neurological disorders abnormal phase synchrony and a simplified functional diagram of the SoC.

feedback. Pairs of neural signals are amplified and filtered in a narrow pass-band in which abnormal synchrony is monitored. In-phase (I) and quadrature-phase (Q) components are computed by allpass and Hilbert filters, respectively. I and Q are used to compute magnitude, phase, and phase difference of the signals which are then wirelessly monitored. Phase locking value (PLV), a common metric of phase synchrony, is computed in the feedback. The current-mode stimulator is triggered when the PLV indicates abnormal phase synchrony levels. In epilepsy, seizure precursors are abnormally large fluctuations in PLV which can be detected by thresholding.

A detailed block diagram of the SoC is presented in Fig. 2. There are 64 ADCs organized in a scalable manner, one per neural input, for raw neural data monitoring (not shown). In the phase synchrony computation mode, the ADCs are re-configured as multiplying ADCs (MADCs) to perform multiplications, the most computationally intensive operations in allpass and Hilbert FIR filters. A bank of eight MADCs combined with a 16-tap folded add-and-delay line yields a 16-tap transposed symmetric mixed-signal FIR filter. MADCs are time-multiplexed among eight neural inputs and eight add-and-delay lines to comprise eight FIR filters [7]. The use of in-channel MADCs eliminates 64 8-bit digital multipliers clocked at 8$\times$ sampling rate. As opposed to [7], in this design, two sets of filters, eight allpass and eight Hilbert FIR filters, are implemented to compute I and Q components, respectively, in two sets of eight recording channels. These circuits are repeated four times to accommodate 64 inputs. The phase, magnitude and phase synchronization processor utilizes three digital CORDIC cores [8]. The computed PLV value is

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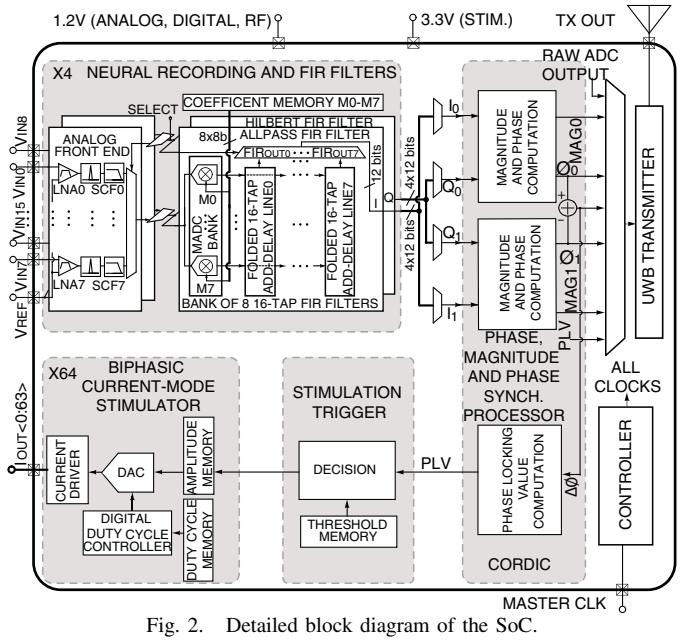

Fig. 2. Detailed block diagram of the SoC.

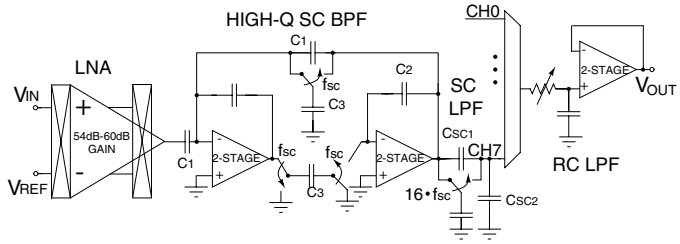

Fig. 3. Neural recording channel.

compared with programmed stimulation criteria. When triggered, the 64-channel neural stimulator generates individually programmable biphasic currents. A UWB wireless transmitter sends raw ADC data, neural vector parameters and PLV off-chip. All control signals are generated by an on-chip controller.

III. Circuit Implementation

Fig. 3 depicts the circuit implementation of the analog front-end. Two stages of AC-coupled capacitive feedback amplifiers provide 54-60dB programmable gain. The first stage is chopper stabilized. The high linearity of the second stage is achieved by biasing subthreshold MOS transistors with a constant voltage generated by source followers [7]. The 2nd-order bi-quad switched capacitor (SC) BPF with the quality factor of 3.2 selects a narrow neural band of interest. The SC LPF removes aliasing components introduced by the BPF. A subsequent compact tuneable buffered RC LPF removes aliasing caused by the SC LPF.

Fig. 4(a) shows the circuit implementation of a set of 8-channel recording and stimulation signal paths. To extract the real and imaginary components the RC LPF drives two sets of eight parallel successive approximation register (SAR) MADCs. Each MADC requires an MDAC that uses a binary-weighted split-capacitor DAC. It multiplies two digital values at the cost of a small overhead of three two-input logic gates

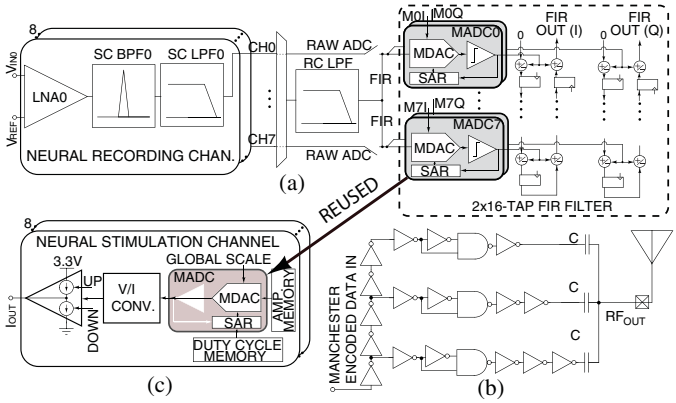

Fig. 4. Integrated circuit implementation of (a) eight neural recording channels for I/Q separation, (b) the UWB transmitter and (c) the neural stimulator.

per bit. One set of eight MADCs implements an FIR filter programmed for an all pass-filter (I-extraction). The other set of eight MADCs, implements an FIR filter programmed for the Hilbert transform (Q-extraction). In this mode, 32 recording channels utilize 64 FIR filters (32 allpass and 32 Hilbert FIR filters) as shown for 8 channels in Fig. 4(a). Both the I and Q signals are sent to the on-chip digital processor. The 10-bit processor utilizes three CORDIC cores to simultaneously compute the magnitude, phase, phase difference and the phase-locking value per sample. Expensive multiplication operations are eliminated as only shift operations are performed by the CORDIC processor. An all-digital delay line-based UWB transmitter shown in Fig. 4(b) generates a double-differentiated Gaussian pulse. The delay cells in all the paths are implemented as current-starved inverters to allow for tuning of the UWB pulse width for two different FCC bands (0-1GHz or 3.1-10.4GHz).

In the stimulation mode, the MDACs and SAR logic are reused in the neural stimulation channel for programmable waveform generation as shown in Fig. 4(c). A V-I converter and a 3.3V biphasic current driver deliver the triggered stimulus. An in-channel 12-bit memory stores an 8-bit current amplitude and a 4-bit duty cycle values. The reuse of MDACs and SAR logic eliminates 64 8-bit DACs and 64 digital duty cycle controllers.

IV. Experimental Results

The micrograph of the 4mm $\times$ 3mm SoC implemented in a standard 1P8M 0.13μm CMOS technology is shown in Fig. 5(a). There is a total of 1kB of on-chip memory and approximately 1 million transistors. The layout of the channel including the neural recording amplifier, SC bandpass filter, biphasic current driver, SAR multiplying ADC/DAC and a 22-bit memory is depicted in Fig. 5(b). Each 300μm $\times$ 300μm channel has a bondpad to be flip-chip bonded directly to a microelectrode array.

The experimentally measured results for the analog front end are depicted in Fig. 6(a)-(c). The experimentally measured frequency response of the amplifiers and the SC filters for several frequency bands is shown in Fig. 6(d). An FFT of the ADC output yields ENOB of 7.6-bits at 28 kS/s as presented

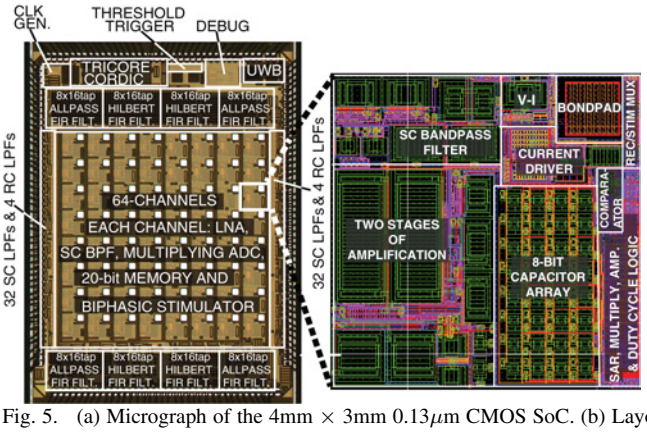

Fig. 5. (a) Micrograph of the 4mm × 3mm 0.13μm CMOS SoC. (b) Layout of the 300μm × 300μm recording and stimulation channel.

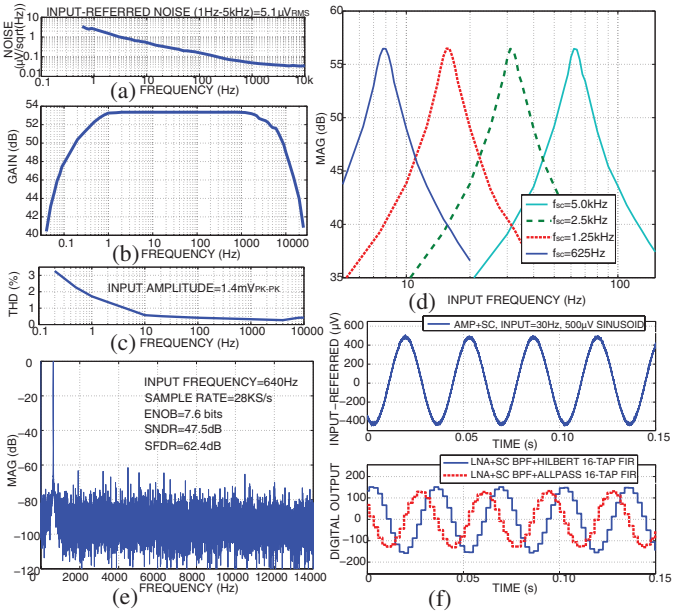

Fig. 6. Experimentally measured (a) input-referred noise, (b) frequency response and (c) total-harmonic distortion (THD) of the neural recording amplifier. (d) Experimentally measured frequency response of the neural recording amplifier and the SC BPF. (e) Experimentally measured FFT of an in-channel ADC. (f) Experimentally measured I/Q separation including the full signal path of input.

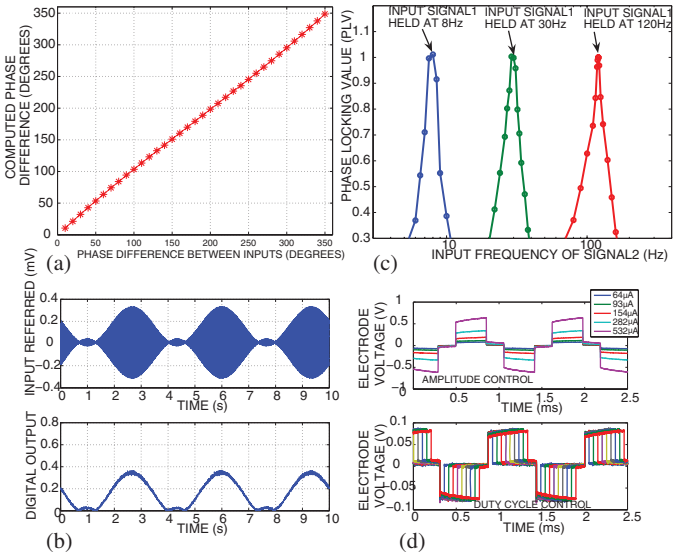

Fig. 7. (a) Experimentally measured results including the entire signal path: (a) phase difference computation (b) magnitude computation (envelope extraction) (c) PLV computed between two channels and (d) neural stimulating current into a saline solution.

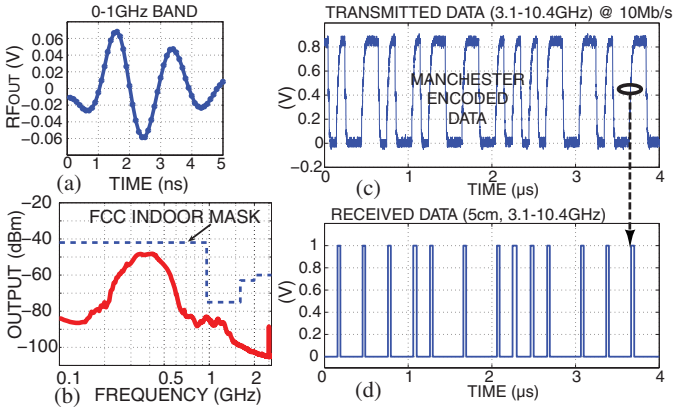

Fig. 8. Experimentally measured results for the wireless transmitter: (a) UWB pulse in the 0-1GHz band and (b) output spectrum of the 0-1GHz UWB pulse. (c) Transmitted Manchester-encoded data at 10Mb/s and (d) wirelessly received data from a 5cm distance modulated in the 3.1-10.4GHz band.

in Fig. 6 (e). Fig. 6(f) demonstrates experimentally computed I and Q components of the shown input fed through the full signal path.

The full signal path from the input of the neural recording channel to the output of the digital processor was also experimentally characterized. Fig. 7(a) depicts the phase difference between two 100μV sinusoidal signals computed on-chip with less than 1.5 percent deviation from the ideal case. Fig. 7(b) shows the magnitude of a 30Hz 300μV_{pk} sinusoid modulated with a higher-frequency sinusoid computed on-chip. Fig. 7(c) shows the PLV between two signals with the frequency of one signal held at three fixed values and the frequency of the other swept. Fig. 7(d) depicts experimentally measured neural stimulator output current into a saline solution for various amplitude and duty cycle settings. The experimentally measured UWB pulse in the 0-1GHz band is shown in Fig. 8(a). The measured output spectrum and the corresponding FCC mask for the UWB transmitter operating in the 0 to 1GHz frequency band is depicted in Fig. 8(b). Fig. 8(c) shows transmitted 10MB/s Manchester encoded-data and Fig. 8(d) displays the wirelessly received UWB modulated data utilizing the 3.1-10.4GHz frequency band over a 5cm distance.

The SoC was validated in on-line in vivo experiments in a population of 4 freely moving rats and in off-line human ECoG data. In animal studies, two types of rat models of epilepsy were employed, non-convulsive epilepsy induced by gamma butyrolactone (GBL) and convulsive epilepsy induced by kainic acid, both recorded and stimulated with 8 depth electrodes. For rats, the SC BPF was set to either a 4Hz or 8Hz center frequency to capture the abnormal phase synchrony in these frequency bands. An example of the experimental results for non-convulsive seizures (4Hz) is shown in Fig. 9(a). GBL injected at time t=0s induces a seizure at time t=222s. At time t=50s, 172s before the seizure starts, the PLV at 4Hz computed by the chip increases, resulting in an early seizure detection.

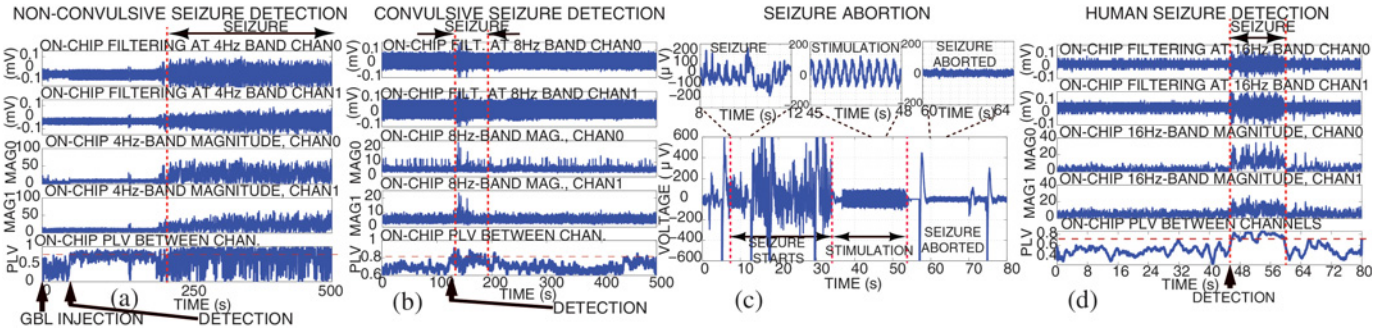

Fig. 9. Results of in-vivo testing in freely moving rats demonstrating (a) early detection of a seizure triggered by a GBL injection, (b) early detection of a seizure triggered by kainic acid injection, and (c) abortion of a seizure using the on-chip neural stimulator. (d) An example of a result of off-line human seizure detection for a University of Toronto epilepsy patient.

TABLE I

STATE-OF-THE-ART NEURAL RECORDING AND/OR STIMULATION SOCS

Spec.	[5]	[2]	[4]	[3]	[7]	THIS WORK
Pwr. Diss.(mW)	0.375	0.077	0.27	6.5	5.03	1.4/1.5
Tech.(μm)	0.35	0.18	0.18	0.13	0.13	0.13
Area(mm)^2	10.9	6.25	2.7	25	12	12
Supply(V)	1.5	1.0	1.8	1.2	1.2	1.2/3.3
# Record Chan.	4	1	8	96	64	64
Pwr/chan.(μW)	32.8	4	9	68	6.3	10
Gain(dB)	52-66	72	-	56	54-60	54-60
Noise(μV_{rms})	3.1	1.3	-	2.2	6.5	5.1
f_{L3dB}(Hz)	0.1	0.5	-	280	10	1
f_{H3dB}(Hz)	12k	100	-	10k	5k	5k
CMRR(dB)	58	60	-	-	75	78
ADC SNDR	54.7	65	44	60.3	48.5	47.5
SC Filter	-	BPF	BPF	BPF	-	BPF
Signal Proc.	Yes	Yes	Yes	No	Yes	Yes
FIR Filters	-	7x48T	1x22T	-	64x16T	64x16T
IIR Filters	1x1T	-	-	-	-	-
DSP	-	Feature Extract	-	-	-	Tri-CORDIC
Univariate Operations	4x Spike	1x Mag	-	-	64x Spike	64xMag 64xϕ
Bivariate Operations	-	-	-	-	-	32x$\Delta\phi$ 32xPLV
Closed-loop Stimulation	Yes	No	Yes	No	No	Yes
# Stim. Chan.	4	-	64	-	-	64
DAC Res.(bits)	6	-	7	-	-	8
Compliance(V)	3.2	-	1.8	-	-	2
Current(mA)	0-0.1	-	0-0.14	-	-	0.01-1.2
Duty Cycle Res.	No	-	6-bit	-	-	4-bit
Wireless TX	Yes	No	No	No	Yes	Yes
Modulation	FSK	-	-	-	FSK	UWB
Date-rate(Mb/s)	-	-	-	-	1.5	10
TX Pwr.(mW)	0.2	-	-	-	3.7	0.1

In Fig. 9(b), a convulsive seizure (8Hz) in a rat is induced by a kainic acid injection at time t=-5min and detected before the seizure starts. In Fig. 9(c), a 5Hz 100μA biphasic current burst that starts early in the seizure successfully aborts it. Overall, on-chip responsive electrical stimulation aborted 80 percent of all rat seizures. For spontaneous seizures in humans the SC BPF center frequency was set to 16Hz to capture abnormal synchrony at that frequency. Fig. 9(d) depicts an example of on-chip off-line early seizure detection in ECoG data recorded from an epilepsy patient at the Hospital for Sick Children in Toronto.

A comparitive analysis is given in Table I. This design demonstrates advanced functionality among recently published state-of-the-art neural recording and stimulation SoCs. It combines 64 recording channels with SC bandpass filters, 64 stimulation channels, 64 programmable 16-tap FIR filters, a tri-core CORDIC processor and an UWB transmitter. It computes phase and phase synchronization which triggers closed-loop current-mode neural stimulation.

V. CONCLUSION

A 0.13μm CMOS wireless closed-loop neural recording and stimulation SoC is presented. The SoC has 64 neural recording and stimulation channels. The on-chip neural vector analyzer computes phase synchrony among inputs to trigger a closed-loop biphasic current-mode neural stimulation. The total power dissipation is 1.4mW from a 1.2V supply in the recording mode and 1.5mW from a 3.3V supply in the stimulation mode. The system was characterized in vivo and demonstrates early seizure detection and abortion in freely moving rodents and off-line seizure detection in humans.

REFERENCES

[1] F. Mormann, R. G. Andrzejak, C. E. Elger, and K. Lehnertz, "Seizure prediction: the long and winding road," *Journal of Neurology, Brain*, vol. 130, no. 2, pp. 314–333, September 2007.

[2] N. Verma, Ali Shoeb, J. Bohorquez, Joel Dawson, John Guttag, and Anantha P. Chandrakasan, "A micro-power EEG acquisition SoC with integrated feature extraction processor for a chronic seizure detection system," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 804–816, April 2010.

[3] Hua Gao, Ross M. Walker, Paul Nuyujukian, Kofi A. A. Makinwa, Krishna V. Shenoy, Boris Murmann, and Teresa H. Meng, "HermesE: A 96-channel full data rate direct neural interface in 0.13μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 4, pp. 1043–1055, April 2012.

[4] J. Lee, H. Rhew, D. R. Kipke, and M. P. Flynn, "A 64 channel programmable closed-loop neurostimulator with 8 channel neural amplifier and logarithmic ADC," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1935–1945, September 2010.

[5] M. Azin, D. J. Guggenmos, S. Barbay, R. J. Nudo, and P. Mohseni, "A battery-powered activity-dependent intracortical microstimulation IC for brain-machine-brain interface," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 4, pp. 731–745, April 2011.

[6] M S Chae, W Liu, Z Yang, T Chen, J Kim, M Sivaprakasam, and M Yuce, "A 128-channel 6mW wireless neural recording IC with on-the-fly spike sorting and UWB transmitter," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 146–603, February 2008.

[7] K. Abdelhalim and R. Genov, "915-MHz wireless 64-channel neural recording SoC with programmable mixed-signal FIR filters," *IEEE European Solid-State Circuits Conference*, pp. 223–226, September 2011.

[8] K. Abdelhalim, V. Smolyakov, and R. Genov, "Phase-synchronization early epileptic seizure detector VLSI architecture," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 5, no. 5, pp. 430–438, October 2011.