An Impedance-Tracking Battery-less Arbitrary-Waveform Neurostimulator with Load-Adaptive 20V Voltage Compliance

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I. Abstract

A 4-channel wireless and battery-less neurostimulator with impedance-tracking power-adaptive voltage compliance is presented. The device houses a 10 mm^2 0.35μm HV-CMOS SoC (system on a chip) that performs current-mode arbitrary-waveform stimulation with voltage compliance of up to 20 V. An on-chip mixed-signal controller together with a 3-bit charge-pump maintain supply voltage at its minimum required value, resulting in up to 68.5% saving in power. An 8-bit current DAC is implemented in each channel, which together with adjustable supply voltage yield a current range from 23 μA to 95 mA (100Ω load). The device receives both power and configuration commands wirelessly using a near-field inductive link. The neurostimulator SoC is wire-bonded on a 2×2 cm^2 PCB. Additional rigid and flexible PCBs of the same size provide wireless command and power interface. The 3-board 2×2×0.7 cm^3 stacked system weighs 6 grams.

II. Introduction

Current-mode neurostimulators with high voltage compliance have been demonstrated useful in many applications such as intra-cranial stimulation [1], trans-cranial functional neuromuscular stimulation (FNS) [2], and optogenetic brain stimulation [3]. The high voltage compliance which is made possible by using high-voltage CMOS technologies [4]–[7], is required for either high stimulation current amplitudes (e.g. neuromuscular stimulation (>10mA)), or stimulating to a high-impedance electrode (e.g. epi-retinal stimulation).

Despite the advantages over voltage-controlled and charge-controlled stimulators (listed in [3]), current-controlled stimulators typically suffer from poor power efficiency. This is mainly because the supply voltage of these stimulators is set to accommodate sufficient headroom voltage for the worst-case scenario, which is stimulating with the highest-amplitude current into the largest-possible tissue impedance. To deliver a rectangular current-mode stimulation pulse with an amplitude of I_{stim}, the minimum required supply voltage is [4]:

$$VDD_{min} = I_{stim} \cdot R_{elec} + \frac{I_{stim} T_{stim}}{C_{elec}} + V_{headroom} \quad (1)$$

where R_{elec} and C_{elec} are the load resistive and capacitive components, respectively, and $V_{headroom}$ is the minimum required headroom voltage for the current driver. This equation shows that the voltage compliance of a stimulator is set by (a) the stimulation current amplitude, and (b) the instantaneous electrode-tissue interface impedance. Consequently, a large portion of the stimulator power (up to 80%) is wasted when stimulating with lower-than-maximum current amplitudes or into smaller-than-maximum tissue impedances. For the case of stimulators with high voltage compliance (∼20V), this power loss becomes a significant value.

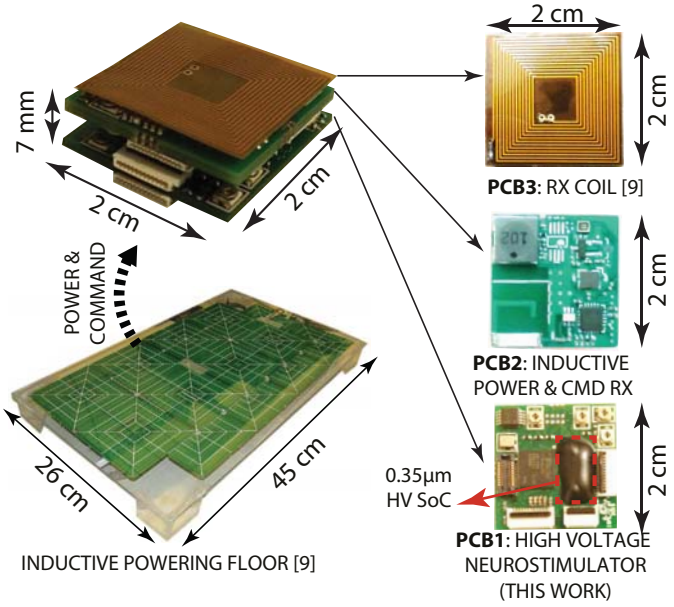

Fig. 1. Inductively-powered 2×2×0.7 cm^3 wireless neurostimulator device with the HV (high voltage) 0.35μm CMOS SoC wire-bonded onto PCB1. The inductive powering system is first presented in [9].

To address this issue, some power-adaptive stimulator designs are reported in the literature [5]–[7]. For most cases, the supply voltage is only adaptive to the changes in the stimulation current amplitude, while the electrode impedance variation is usually ignored [5], [6]. In [7] the authors have proposed an adaptive design that takes both current amplitude and electrode impedance into account, however, the proposed design is a voltage-mode stimulator, which has its disadvantages discussed in [3].

We present a 3-board 2×2×0.7 cm^3 device that hosts a 10 mm^2 high-voltage 0.35μm CMOS neurostimulator SoC. The SoC has 4 independently-programmable and independently-power-optimized current-mode stimulation channels. It benefits from a power-optimized design with a voltage compliance of up to 20V, that is automatically adaptable to variations of both stimulation current amplitude, and instantaneous electrode impedance. The device receives stimulation commands wirelessly and is powered inductively, which makes electrodes the only wires connected to the it during an animal experiment.

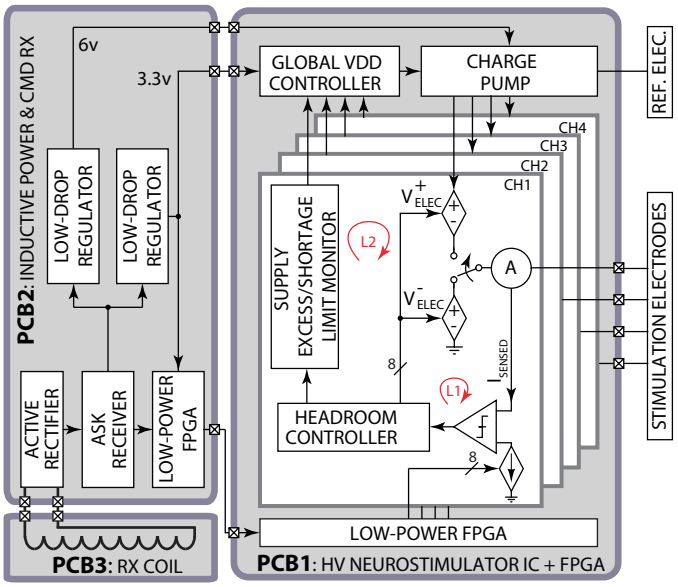

Fig. 2. System block diagram of the 3-PCB neurostimulator device with an on-chip nested dual-loop impedance-tracking voltage compliance control system.

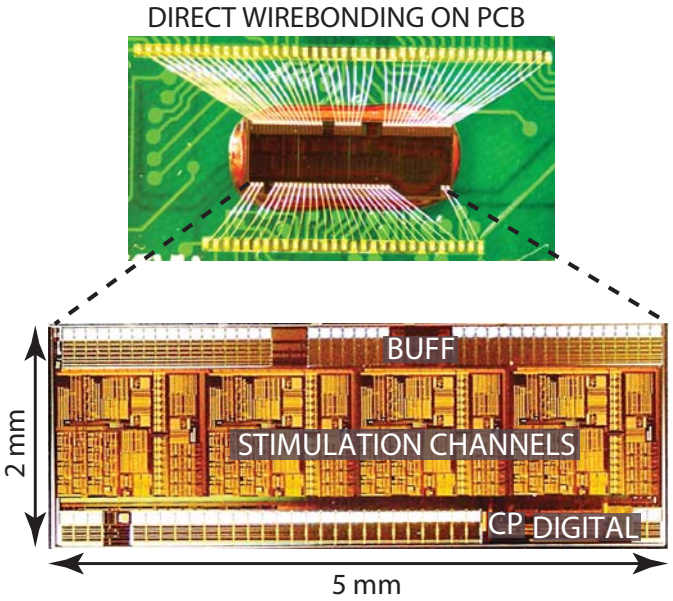

Fig. 3. $2\times2\times0.7$ cm^3 neurostimulator and its 0.35μm IC.

III. System Architecture

Fig. 1 shows the inductively-powered wireless neurostimulator device (top, left), with an inductive floor designed to provide power and commands to the device (bottom, left) [9]. As shown, the device is a stack of three PCBs (printed circuit board) that are shown in Fig. 1(right): a high-voltage neurostimulation board (PCB1), a wireless data communication and power management board (PCB2) [10], and an inductive power-receiving coil (PCB3). Also as illustrated, a 4-channel high-voltage 10 mm^2 0.35μm CMOS SoC (system on chip) is directly wire-bonded to the PCB1 to perform power-adaptive current-mode neurostimulation.

Fig. 2 depicts the system architecture of the presented neuro-stimulator device. Inductively-transmitted power signals are received by the coil (PCB3) and are fed to an active rectifier on the PCB2. The rectifier output is then sent to voltage regulators as well as an ASK receiver, to demodulate amplitude-shift-keyed power signals that carry stimulation commands such as pulse frequency, width, amplitude and duty-cycle. Using a vertical connector, these commands are sent to the IC that is wirebonded onto PCB1 (Fig. 3). The DC voltage outputs of the LDOs (low dropout regulators) on PCB2 are also shared with PCB1 through the same connector and are used by the on-chip charge pump to generate the adjustable supply voltage in the range of 6-20V.

The inductive link provides up to 30 mW continuously with the maximum distance of 15 cm away from the transmitter. A 470 mF super capacitor is utilized that gets charged during the idle phase and provides stable supply voltage during stimulation phase for a maximum of 2 minutes continuous pulse-train with the maximum signal amplitude. The inductive powering system operates at 1.5 MHz, and achieves an overall wireless power transfer efficiency of up to 40% at a maximum distance of 15 cm [9].

To maximize the neurostimulator power efficiency, two nested mixed-signal control loops are implemented on the chip to monitor and maintain both the voltage headroom in each channel (loop L1), and the global chip VDD (loop L2) at their minimum required values, defined by Eq. 1. The control loops monitor both electrode impedance (variable during the experiments) and stimulation current amplitude, and adjust the stimulator's voltage compliance accordingly, resulting in minimum power consumption throughout the experiment.

IV. VLSI Implementation

Fig. 4 depicts the block diagram of the 4-channel neurostimulation IC with the simplified circuit schematic of its major blocks. As shown, four load-adaptive power-efficient stimulation channels, a global digital controller unit, and a charge-pump for adjustable supply voltage generation are included on the chip. A low-power area-optimized current DAC in each channel generates a reference current with 8 bit resolution. This current and the electrode stimulation currents are converted to voltage using Rail-to-rail OpAmps. The voltages are then compared (using a rail-to-rail comparator) and the result is fed to an up/down counter which its output is used by an 8-bit voltage DAC to set the new voltage at the electrode.

Using this closed-loop configuration, The current that is injected to the tissue is always kept at the level set by the reference current, while any electrode impedance variations are compensated by automatically adjusting the voltage at the electrode. This technique allows us to perform current-mode stimulation, and at the same time, keep the voltage headroom to the minimum, resulting in no power loss due to excess of supply voltage.

In addition to the in-channel controller (loop L1), a limit control unit monitors the 4 most significant bits of the 8-bit up/down counter, and sends a 2-bit command to the global VDD controller indicating whether there is a shortage or excess of supply voltage for that channel. A "01" means shortage of supply in one of the channels (increase VDD), a "10" means excess of supply in all channels (decrease VDD),

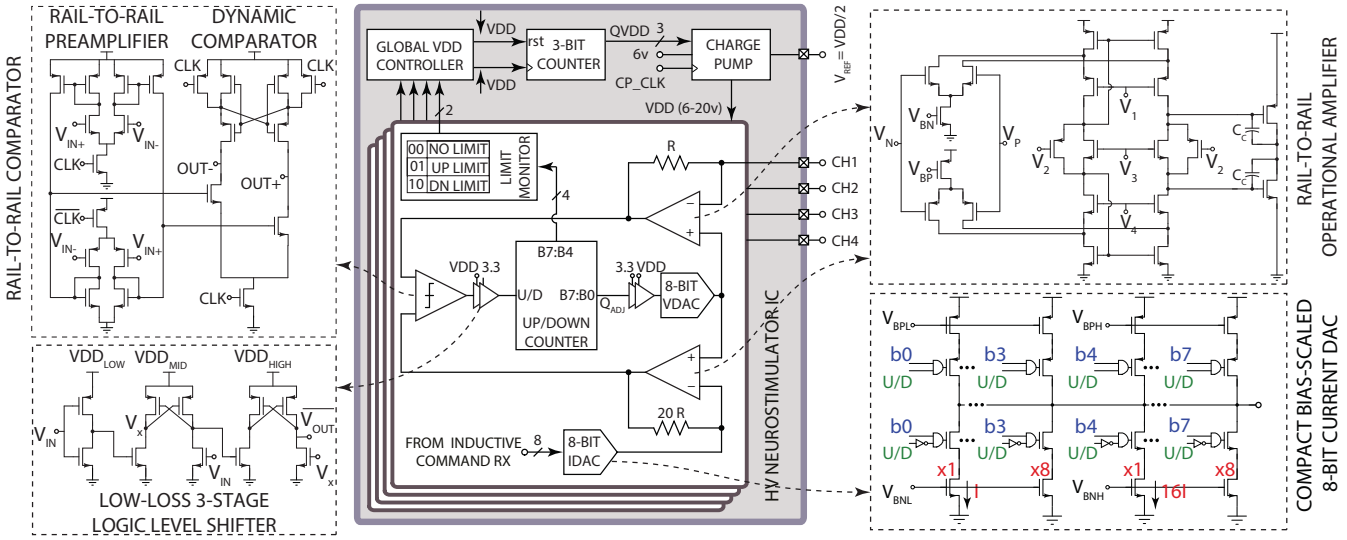

Fig. 4. Block diagram of the neurostimulator IC with simplified circuit schematics of the major blocks.

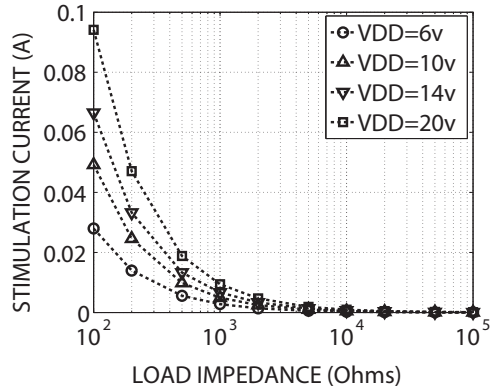

Fig. 5. Experimentally measured Stimulation current amplitude versus load impedance for 4 VDD examples.

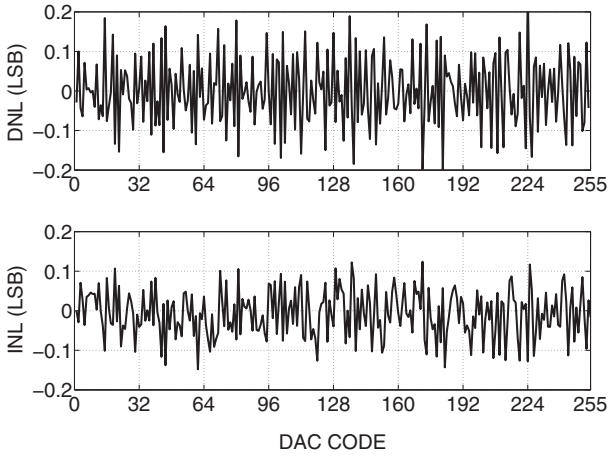

Fig. 6. Experimentally measured differential and integrated nonlinearity of the 8-bit current DAC used for reference stimulation current generation.

and a "00" means normal operation (maintain VDD). The global controller (loop L2) adjusts the VDD using the on-chip charge-pump with 3 bits of resolution. In addition to bipolar stimulation, to enable bi-phasic mono-polar stimulation using a single supply, a switched-capacitor voltage divider is also added to the device which makes sure that the reference electrode voltage, V_{REF} is always kept at VDD/2.

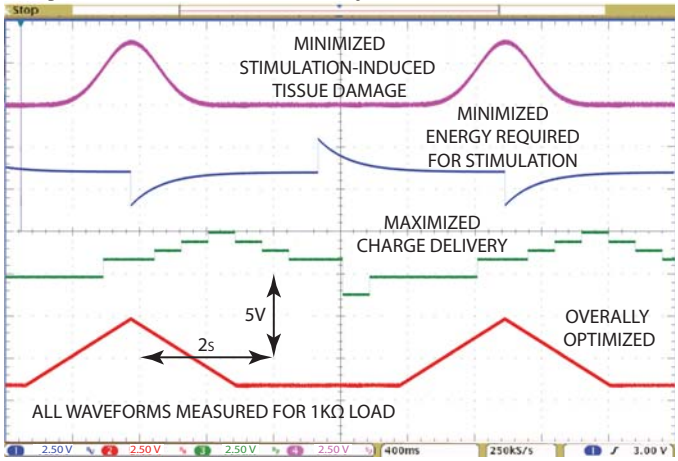

Fig. 7. Experimentally measured waveforms generated by the 4 stimulation channels, each optimized for a different purpose.

V. Experimental Results

Fig. 5 shows the measured stimulation current amplitude versus the load impedance for four different VDD values. Each channel on the chip provides a current resolution of 23μA, which is also the smallest stimulation current amplitude. Additionally. the output stage of the rail-to-rail opamp is sized to drive loads as small is 100Ω with a maximum current of 95 mA. This yields an effective dynamic range of 12 bits. Fig. 6 shows the differential and integral nonlinearities of the in-channel current DAC, both being below 0.2$\times$LSB.

The stimulation waveform is investigated extensively in the literature and optimized shapes are suggested for different purposes such as decreasing stimulation-induced tissue damage, increasing charge injection and decreasing the energy requirements of stimulation [11]. Fig. 7 shows four different experimentally-measured stimulation waveforms, each generated by one of the arbitrary-waveform stimulation channels on the chip, and each optimized for a specific purpose that is shown in Fig. 7.

Fig. 8 shows the measured global VDD and the electrode voltage of one of the channels as the Z_{ELEC} is increased.

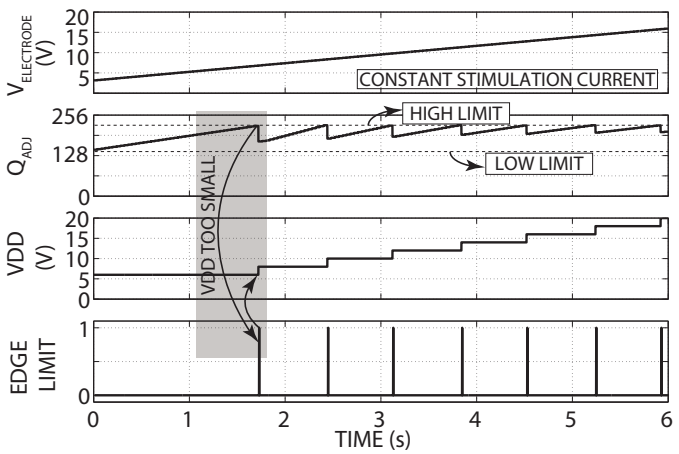

Fig. 8. Experimentally measured electrode voltage, digital controller outputs and supply voltage when load impedance is varied.

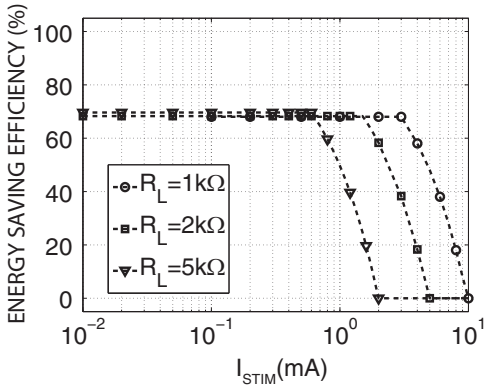

Fig. 9. Experimentally measured energy saving for different stimulation current amplitudes and three examples of load impedance.

As the electrode voltage increases with Z_{ELEC}, its digital equivalent (Q_{ADJ}) is monitored by the limit controller. Once the electrode voltage reaches close to the channel supply value, the limit controller signal becomes one, which triggers the charge-pump to increase the VDD to compensate for the initial increase in the Z_{ELEC}.

Fig. 9 shows the energy saving efficiency of the stimulator with reference to the case that the VDD is fixed at the highest value (20V). As shown, for lower impedance$\times$currents that require smaller voltage compliance, using the adaptive supply scheme results in saving more energy. The maximum measured power saving efficiency is 68.5% which happens when the VDD is set to its minimum value, 6 V.

VI. Conclusion

A inductively-powered wireless and battery-less neurostimulator is presented. The device hosts a 4-channel 10 mm^2 0.35μm HV-CMOS SoC, where each channel generates independently-programmable arbitrary waveforms (8-bit resolution) for stimulation with a voltage compliance of up to 20V. A dual-loop impedance- and current-monitoring digital controller continuously monitors and adjusts the channel voltage headroom and global supply voltage, resulting in up to 68.5% saving in power consumption. The neurostimulator system is powered inductively and receives configuration commands wirelessly using the same link. The system is miniaturized and is implemented using a stack of two rigid and one flexible PCBs, with the size of 2$\times$2$\times$0.7 cm^3 and weight of 6 grams.

TABLE I

TABLE I: State-of-the-art HV neurostimulator ICs.

Specification	JSSC'1 [4]	JSSC'10 [8]	TBioCAS'12 [7]	THIS WORK
TECHNOLOGY (μm)	0.35 HV	0.18 HV	0.35	0.35 HV
AREA (mm^2)	0.47	26.52	0.58	10
SUPPLY (V)	20	32	3.3	20
# OF CHANNELS	8	1024	1	4
# OF INDEPENDENT CH.	2	256	1	4
ADAPTIVE POWER	YES	NO	YES	YES
MAX POWER SAVING	64.7	-	62%	68.5%
STIMULUS CONTROL	Current	Current	Current	Current/Voltage
WIRELESS POWER	YES	YES	NO	YES
WIRELESS DATA COMM.	NO	YES	NO	YES
CHANNEL:				
AREA (mm^2)	0.235	0.081	0.58	1.2
CURRENT DR(mA)	0.003-1	0.003-0.5	<0.45	0.023-95
WAVEFORM	Arbitrary	Arbitrary	Biphasic	Arbitrary

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