DELTA-SIGMA ALGORITHMIC ANALOG-TO-DIGITAL CONVERSION

Grant Mulliken[1,2], *Farhan Adil*[1,3], *Gert Cauwenberghs*[1], *and Roman Genov*[1]

[1]Adaptive Microsystems Laboratory, ECE Dept., Johns Hopkins University, Baltimore, MD 21218
[2]BME Dept., Johns Hopkins University School of Medicine, Baltimore, MD 21205
[3]School of Electrical Engineering, Georgia Tech, Atlanta, GA 30332
E-mail: {*grant,farhan,gert,roman*}*@bach.ece.jhu.edu*

ABSTRACT

Delta-sigma modulation for analog-to-digital conversion resolves a number of bits logarithmic in the number of modulation cycles, and linear in modulation order. As an alternative to higher-order noise shaping, we present an algorithmic scheme that iteratively resamples the modulation residue, by feeding the integrator output back to the input. This yields a bit resolution linear in the number of cycles, similar to an algorithmic analog-to-digital converter. The scheme simplifies the design of the digital decimator to a single shifting counter, and avoids interstage gain errors in conventional algorithmic analog-to-digital converters. Experimental results from an integrated CMOS array of 128 converters show the utility of the design for large-scale parallel quantization in digital imaging and hybrid analog-digital computing.

1. INTRODUCTION

Delta-sigma ($\Delta\Sigma$) modulation has emerged as the architecture of choice for high-resolution analog-to-digital (A/D) conversion using low-precision analog components [1]. The increased resolution comes at the expense of reduced conversion bandwidth or increased clock speed due to oversampling, and increased digital complexity to decimate the modulator output stream. For very low bandwidth applications, lowest digital complexity is achieved with a first-order $\Delta\Sigma$ incremental converter [2], where a counter implements a rectangular decimation filter. Higher-order $\Delta\Sigma$ incremental converters [3] are capable of attaining higher conversion bandwidth, using additional analog and digital circuitry. Alternatively, higher bandwidth can be obtained from a first-order incremental converter by further refining the modulation residue on the integrator at the end of conversion using a Nyquist A/D converter [4, 5, 6]. The principle is similar to dual-quantization oversampled converters [7, 8], except the second quantizer operates at the conversion rate and requires no decimation.

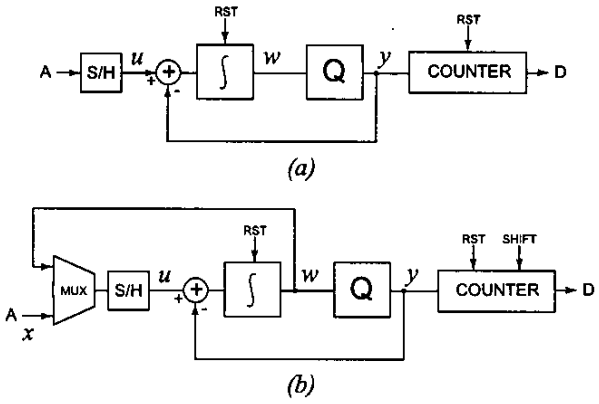

Fig. 1. (a) *First-order $\Delta\Sigma$ incremental A/D converter.* (b) *$\Delta\Sigma$ algorithmic A/D converter, with residue resampling across the accumulator, and shifting counter for the decimator.*

The presented architecture uses the same first-order modulator, with virtually no overhead in analog and digital hardware, to incrementally convert the modulation residue of preceding incremental conversion. By using the same signal path in ratio-insensitive manner, precise matching between multiple quantization results is obtained. Matching is a concern in the precision of multiple-quantization oversampled data converters [9], usually requiring compensation in the digital domain [10]. The presented scheme is similar to algorithmic A/D conversion, but avoids interstage gain errors when precisely ratioed analog components are not available. Very high integration density can be achieved by virtue of the simple modulator and decimator architecture.

2. $\Delta\Sigma$ INCREMENTAL A/D CONVERSION

For clarity of exposition we start the formulation with that of the first-order incremental A/D converter [2], depicted in

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Figure 1(a). A first-order $\Delta\Sigma$ modulator converts an analog sequence $u[i]$ into a bitstream $y[i]$, using a 'resetable' (RST) analog accumulator

$$w[0] = 0 \quad (1)$$

$$w[i+1] = w[i] + \alpha\,(u[i] - y[i])\,, \quad i = 0, \ldots N-1 \quad (2)$$

$$w[N+1] = w[N] - \alpha\, y[N] \quad (3)$$

and a single-bit quantizer

$$y[0] = -1 \quad (4)$$

$$y[i] = \mathrm{sign}(w[i])\,, \quad i = 1, \ldots N\,. \quad (5)$$

A binary counter accumulates the bits[1] $y[i]$ to produce a decimated output. The rectangular decimation window, and initial reset of the accumulator, avoid tones in the quantization noise spectrum at DC input that are characteristic of a conventional first-order $\Delta\Sigma$ modulator with lowpass decimation filter [2]. The quantization error (conversion residue) is directly given by the final accumulator value $w[N+1]$, as verified by summing (2) and (3) over i:

$$\sum_{i=0}^{N} y[i] = \sum_{i=0}^{N-1} u[i] - \frac{1}{\alpha} w[N+1]\,. \quad (6)$$

For an input $u[i]$ within the conversion range $[-1, 1]$ (in dimensionless units), $w[N+1]$ in (3) is bounded by the range $[-\alpha, \alpha]$, and a worst-case resolution of $\log_2(N)$ bits is warranted[2].

Higher resolution at lower oversampling N can be obtained using higher-order incremental conversion [3]. A lower-complexity alternative is presented next.

3. $\Delta\Sigma$ ALGORITHMIC A/D CONVERSION

The conversion residue $\frac{1}{\alpha}w[N+1]$ in (6) is converted further into digital form to obtain higher resolution. As in other multiple-quantization oversampled converters [3]-[8], gain mismatch between quantization signal paths is a limiting factor in the precision available [9]. Ratio-insensitive matching is achieved by resampling the residue through the same signal path as used for accumulation (2), and employing the same modulator to convert the residue.

Assume a constant input (or its average) x presented to the incremental converter for N initial cycles, $u[i] = x$, $i = 0, \ldots N-1$,

$$\sum_{i=0}^{N} y[i] = N\,x - \frac{1}{\alpha} w[N+1]\,. \quad (7)$$

[1] $y = -1$ corresponds to logic 0 for notational convenience.

[2] Note that the last modulation cycle (3) contributes one full bit of resolution, since $w[i]$ for $i \leq N$ in (2) is bounded by 2α in amplitude. The extra zero-input modulation cycle (3) can be avoided by quantizing $w[i] + \alpha u[i]$ instead of $w[i]$ in (5).

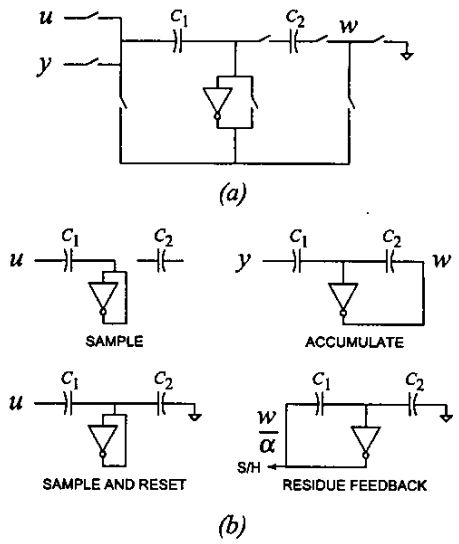

Fig. 2. *Invertable, resetable analog accumulator.* (a) *Circuit diagram.* (b) *Operational modes.*

At the end of conversion, the residue $w[N+1]$ is fed back to the input for subsequent incremental conversion over N' additional cycles, $u'[i] = \beta w[N+1]$, $i = 0, \ldots N'-1$, where β represents the residue resampling gain. Thus

$$\sum_{i=0}^{N'} y'[i] = N'\beta\, w[N+1] - \frac{1}{\alpha} w'[N'+1] \quad (8)$$

which under the matching condition $\alpha\beta \equiv 1$ combines with (7) to cancel the first residue $w[N+1]$:

$$N' \sum_{i=0}^{N} y[i] + \sum_{i=0}^{N'} y'[i] = NN'\,x - \frac{1}{\alpha} w'[N'+1]. \quad (9)$$

The left-hand side of (9) is readily available in digital form, and the right-hand terms conform to (6) with effective NN'-level resolution. Therefore, the residue conversion (8) enhances the resolution of (7) by an extra $\log_2(N')$ bits. The algorithmic recursion can be continued to produce $\log_2(N)$ bits for every conversion of the preceding residue over N incremental cycles. The recursion corresponds to a radix-N algorithmic A/D converter, but without the need for N-ratioed analog components.

The matching condition $\alpha\beta \equiv 1$ for ratio-insensitive operation is met using an invertable circuit topology for the analog accumulator, described next.

4. IMPLEMENTATION

The hardware complexity of the $\Delta\Sigma$ algorithmic A/D converter, depicted in Figure 1(b), is essentially identical to

that of the $\Delta\Sigma$ incremental converter in Figure 1(a). The accumulator is extended to sample the residue in ratio-insensitive manner, and the counter is extended to shift bits in between residue conversions for proper scaling in the decimation.

4.1. Invertable, Resetable Analog Accumulator

Critical to attaining ratio-insensitive sampling of the residue is the design of the accumulator. A simple circuit achieving multiple objectives is depicted in Figure 2 (a), with different modes of operation illustrated in Figure 2 (b). The circuit is shown with minimum number of components using an inverting amplifier, but can be directly extended to differential designs for higher resolution. Correlated double sampling (CDS) in the accumulation of the difference $u[i]-y[i]$ according to (2) offers the advantage of $1/f$ noise and offset cancellation. The switched-capacitor accumulator has ratio-dependent gain $\alpha = C_1/C_2$ that is prone to mismatch; however this mismatch is immaterial in the operation of the first-order modulator with single-bit quantizer. For ratio-insensitive sampling of the residue, the signal and feedback path of the accumulator is inverted by interchanging the C_1 and C_2 components in the circuit topology, shown in Figure 2 (b). As a result, the matching condition $\alpha\beta \equiv 1$ between (7) and (8) is satisfied independent of C_1 and C_2, to a precision limited by the finite gain of the amplifier, and noise and charge injection in the sampling.

4.2. Decimating Shifting Counter

For every algorithmic iteration, the preceding decimated output needs to be scaled by a factor N, the number of incremental cycles in the residue conversion, prior to continued counting. It is particularly convenient to assume N to be radix-2, so that the scaling is simply performed by a binary shift in the decimation count, as suggested in Figure 1(b). A shift register is readily incorporated in a binary counter, with little overhead in the circuit complexity of the implemented decimator.

5. EXPERIMENTAL RESULTS FROM INTEGRATED A/D ARRAY

To demonstrate the advantages of the approach to large-scale, densely integrated quantization in an embedded application, we implemented a bank of 128 $\Delta\Sigma$ algorithmic converters as part of a mixed-signal computational array. The 256 × 128 array performs externally digital matrix-vector multiplication using internally analog elements for very large energetic efficiency (10^{12} multiply-accumulates per Watt of power) [11]. The array core performs analog accumulation of binary-binary partial products, requiring row-parallel A/D conversion for each of the 128 output vector

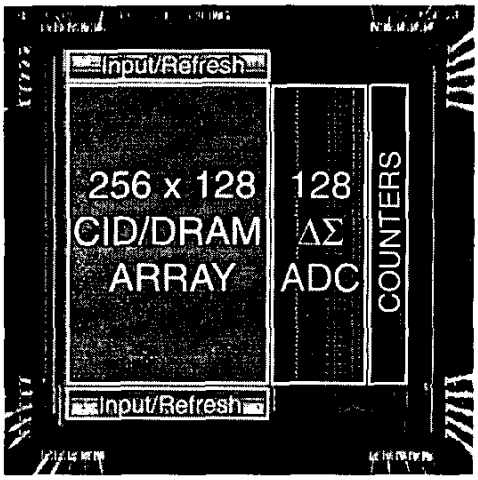

Fig. 3. *Micrograph of mixed-signal array processor [12], containing an array of* 256 × 128 *CID/DRAM multiply-accumulate cells [11], and a row-parallel bank of* 128 *algorithmic* $\Delta\Sigma$ *A/D converters. Die size is* 3 mm × 3 mm *in 0.5 μm CMOS technology.*

components. The micrograph of the integrated system [12] is shown in Figure 3. Each of the 128 A/D channels measure 14 μm by 850 μm.

To maximize integration density, the analog path of the $\Delta\Sigma$ algorithmic architecture of Figure 1(b) uses single-stage cascoded nMOS inverting amplifiers throughout, with nominal gain of -300. Capacitances C_1 and C_2 are nominally 0.25 pF and 0.5 pF, respectively, with $\alpha = 0.5$. Sample-and-hold and comparator blocks are implemented in standard switched-capacitor circuitry, with CDS $1/f$ noise and offset compensation. Dynamic logic implements binary counter and registers.

Example conversion waveforms from the fabricated array are illustrated in Figure 4. Least-squares fits of integral quantization error observed over one channel of the array, configured both for 8-bit incremental and algorithmic $\Delta\Sigma$ conversion, are within the LSB level as shown in Figure 5. However, incremental conversion requires $2^8 + 1 = 257$ cycles, while 2-step algorithmic conversion takes $2 \times (2^4+1) = 34$ cycles. With a 300 ns clock in 2-step 8-bit algorithmic mode, the 128-channel A/D bank delivers 12.8 Msamples/s at 2.6 mW power dissipation, including decimation.

Resolutions larger than 10-bit require higher-gain amplifiers at the cost of decreased integration density and increased power dissipation. In digital imaging and other integrated sensing modalities, maintaining high spatial resolution is usually a more stringent requirement than increasing amplitude resolution.

Note that matching *is* at stake even at low (8-bit) res-

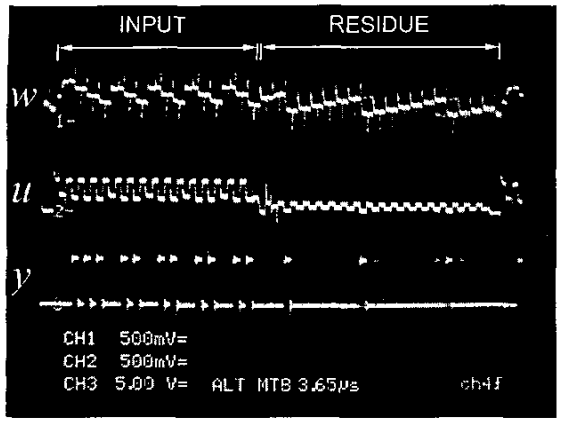

Fig. 4. *Observed waveforms for two-step ΔΣ algorithmic A/D conversion.* Top: *Integrator voltage* $w[i]$. Center: *Sample-and-hold voltage* $u[i]$. Bottom: *Output bits* $y[i]$ *prior to decimation.*

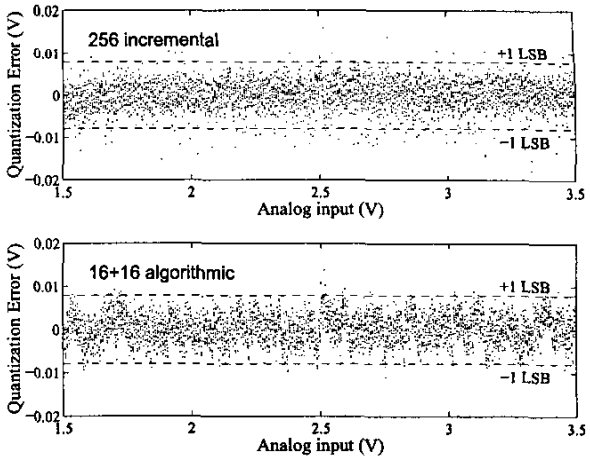

Fig. 5. *Integral quantization residue, recorded from a single channel of the VLSI A/D array in Figure 3, configured for 8-bit conversion.* Top: *ΔΣ incremental conversion (*$N = 256$*).* Bottom: *ΔΣ algorithmic A/D conversion (*$N = 16$*, 2-step).*

olution. Precise matching between capacitors with up to 12-bit uncalibrated precision can be achieved through careful layout in centroid geometry, but not within dimensions pitch-matched to, say, a 45 λ (14 μm) photosensor pixel.

6. CONCLUSION

The proposed technique combines advantages of ΔΣ modulation and algorithmic (cyclic) A/D conversion in a single, simple architecture. Both are included as special limiting cases: a single algorithmic iteration reduces to ΔΣ incremental conversion, and $N = 2$ cycles per iteration yield a ratio-insensitive form of algorithmic A/D conversion.

The reduced hardware complexity and improved component tolerance of the architecture offer a major advantage in integrated applications calling for large-scale parallel quantization at low to medium resolution (8 to 12 bits) but very high integration densities, with a potential for extremely large combined quantization throughputs (Gsample/s range at mW power levels). Bandwidth can be traded for resolution in reconfigurable manner through external control of clock waveforms. Ratio-insensitive matching makes the architecture especially suited for applications of integrated digital acquisition in spatial sensor arrays. An 128-element integrated array prototype demonstrated the principle for applications in mixed-signal analog-digital computing [12].

7. REFERENCES

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