256-Channel Integrated Neural Interface and Spatio-Temporal Signal Processor

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***Abstract*— We present an architecture and VLSI implementation of a distributed neural interface and spatio-temporal signal processor. The integrated neural interface records neural activity simultaneously on 256 voltage-mode channels. Each channel implements differential signal acquisition, amplification and band-pass filtering. An array of in-channel double-memory sample-and-hold cells stores two 16 × 16 electronic images of distributed neural activity consecutively in time. A column-parallel double sampling circuit performs frame differencing in order to identify spatio-temporal neural activity patterns. A 3 mm × 4.5 mm integrated prototype was fabricated in a 0.35 μm CMOS technology. The functionality of the neural interface was experimentally demonstrated in extracellular in vitro recordings from the hippocampus of mice. The utility of the on-sensory-plane signal processor was validated in simulated wavefront detection performed on experimentally measured distributed neural activity recording**

I. Introduction

The human brain is a large-scale interconnected network with common behavioral properties extending across large spatial areas. To gain full understanding of how biological neural networks encode and process information, it is necessary to both record and analyze signals from many neighboring neurons.

Significant insights have been gained into ways of neural information coding through the use of micro-electrodes that can record the activity of single neurons and neural populations in the brain. Recording of neural activity has been traditionally performed using bench-top biomedical instrumentation equipment. These instruments are generally stationary, bulky, limited to one or a few acquisition channels, and prone to excessive noise due to wiring. Integrated neural interfaces, fabricated on a single miniature physical substrate, lack these drawbacks. They offer a small, low power, low noise, and cost effective chronically implantable alternative to commercial bench-top instruments. Integrated neural interfaces perform signal acquisition, amplification, filtering, and, in some instances, quantization and stimulation [1], [2], [3], [4], [5], [6], [7]. They may also provide wireless data interface on the same chip [8].

Various strategies in the analysis of spatio-temporal dynamics of the neuronal activity have been developed. Examples of such analysis include cross-correlation, spectral analysis [9] and population vector analysis [10]. To date, brain activity analysis techniques have been implemented off-chip, on a stationary computer or an additional high-throughput digital processor. Integrated neural interfaces allow for local on-chip intelligent spatio-temporal signal processing, extending their functionality beyond signal acquisition and conditioning. Such signal processing can be performed for data reduction in a wireless communication link, and for automated medical diagnostics and therapy.

To this end, we have designed, prototyped, and experimentally validated a multi-channel single-chip brain-silicon neural recording interface and signal processor. The neural interface contains 256 signal acquisition channels recording neural field potentials from an array of 16x16 electrodes simultaneously, in a distributed fashion. Each channel contains a low noise amplifier with an up to 74dB programmable gain, a tunable anti-aliasing low-pass filter (LPF), and a high-pass filter (HPF) that removes a DC offset present at the electrode-tissue interface. The brain-chip interface records action potentials in the range of tens of microvolts to hundreds of microvolts in the tunable 0.1 Hz - 10 kHz frequency band in order to capture relevant neural activity, as required for analysis and treatment of neurological disorders [9].

Each channel of the integrated neural interface has a sample-and-hold circuit with analog memory, allowing for truly simultaneous signal acquisition across all channels, with subsequent multiplexed array readout and off-chip serial analog-to-digital conversion. The analog memory consists of two capacitive storage cells. This double buffer captures two neural activity electronic "video frames" with no rolling delay effect. A column-parallel double-sampling circuit performs frame differencing in order to analyze spatio-temporal patterns in neuronal population activity. The capability to analyze spatio-temporal neural activity directly on the sensory plane allows for implementations of intelligent electronic implants. Such electronic implants can locally detect characteristic neural

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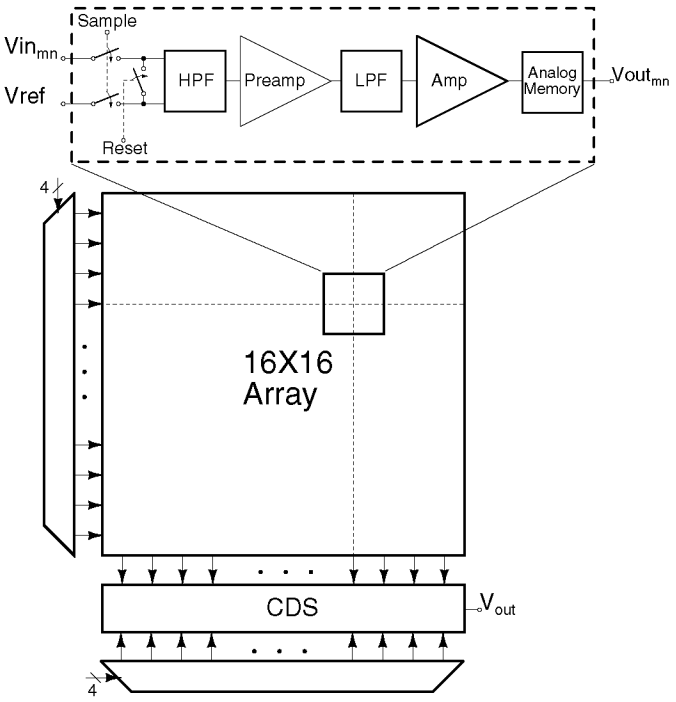

Fig. 1. Block diagram of the integrated neural interface and spatio-temporal signal processor.

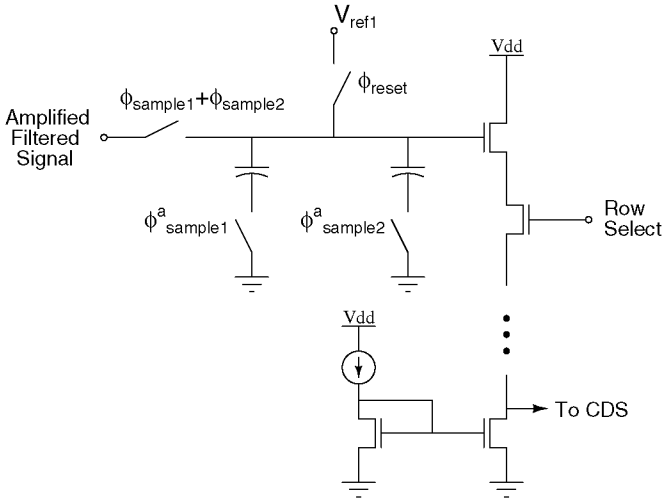

Fig. 2. Sample-and-hold cell with double analog memory for correlated double sampling and neural activity frame differencing.

ensemble behaviors such as action potential wave propagation and focal firing. This functionality also opens up an opportunity to detect and predict states of particular neurological disorders such as epileptic seizures directly in an implant.

The rest of this paper is organized as follows. Section II presents the architecture of the integrated neural interface and spatio-temporal signal processor. Section III details its VLSI implementation. Section IV contains simulated and experimentally measured results validating the functionality and utility of the presented integrated neural interface and spatio-temporal signal processor.

II. Architecture

Most of the frequency content of extracellular action potentials in the brain is concentrated between 0.1Hz and 10kHz. Signal amplitudes range from 50 μV to 500 μV, with 100 μV being a typical average value. For low-noise distributed neural potential field recording and spatio-temporal analysis, a multi-channel integrated neural interface has been designed and prototyped. The neural interface acquires voltages on 256 independent channels simultaneously. The signal acquisition circuits are organized in a 16x16 array as shown in Figure 1.

Each channel in the array shown in Figure 1 contains a high-pass filter (HPF), a low-pass filter (LPF) and two amplification stages. Each channel also contains a sample-and-hold cell with double analog memory. A bank of correlated double sampling (CDS) cells sample the two analog memories, one row at a time, to remove offsets, resulting from device mismatches and to allow for spatio-temporal neural signal processing. Array readout is implemented in a serial fashion as controlled by row and column address decoders. Each channel is connected to on-chip differential recording electrodes through non-passivated top-most metal. Additional circuitry for optional post-fabrication electrode electroplating is also included.

III. VLSI Implementation

A single-stage wide-swing cascoded transconductance amplifier with p-channel MOS input differential pair is employed, both for the preamplifier and the amplifier in each signal acquisition channel. The transconductance amplifier is optimized for low rms noise of 13 μV over a 10kHz bandwidth under the 170 μm pitch cell integration area constraint and 6mW overall power dissipation constraint. The low noise amplifier design procedure employed is detailed in [5].

High pass filtering prevents DC signals, generated at the electrode-tissue interface, from saturating the amplifiers. The HPF is implemented as a frequency selective feedback of the pre-amplifier [5]. Post processing of the neural recording is performed in the discrete domain by means of switched capacitor circuits. The sampling from continuous time to discrete time requires anti-aliasing low pass filtering. The LPF filter is implemented by starving the bias current in the second amplifier.

Accurate distributed multi-site sensing requires maintaining a high degree of correlation in time between all the samples. Time-multiplexed recording architectures do not allow for such correlation. This necessitates a memory buffer in each sensory cell to sample and store the recorded value. Frames of samples across the whole array are captured simultaneously. This eliminates the rolling delay during serial read-out. The local memory cell also allows for time-multiplexing to reduce noise due to substrate coupling. Low-noise signal acquisition is time-multiplexed with high-noise peripheral switch capacitor signal processing and read-out. This ensures no high-amplitude switching activity during the signal acquisition phase and thus

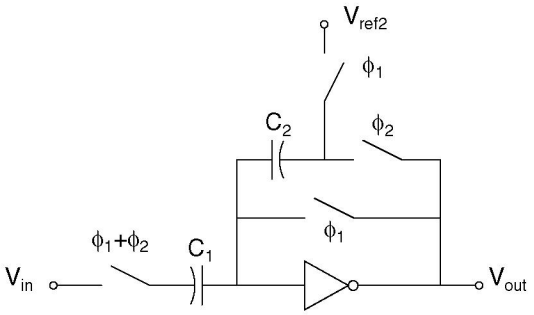

Fig. 3. The schematic of the CDS circuit.

prevents substrate noise from coupling into the low-amplitude signal being acquired.

Spatio-temporal neural signal processing is performed directly on the focal plane by extending the analog memory to include two capacitive storage cells. The memory cells are implemented as sample and hold circuits as shown in Figure 2. One of the main concerns in sample and hold circuits is the dependency of charge injection, originating from switch transistors turning off, on the sampled signal, which introduces non-linear distortion to the signal. To avoid the signal dependency of the charge injection, the bottom plate sampling technique is used. Two advanced versions of the clock signals (denoted by the superscript a) cause the charge injection on the sampling capacitance C_s to be independent of the stored signal. To ensure memoryless charge sharing between the two sampling capacitors and the parasitics, a reset phase sets the initial voltage to a fixed value.

The double buffer captures two neural activity frames with no rolling delay effect on either one. The column-parallel double-sampling circuit, shown in Figure 3, performs frame differencing in order to analyze spatio-temporal patterns in neuronal population activity. The double sampling also removes DC offsets due to channel-to-channel mismatches.

The 256-channel integrated neural interface and signal processor was fabricated on a $3\text{mm} \times 4.5\text{mm}$ die in a $0.35\ \mu m$ double-poly standard CMOS technology. The die micrograph is shown in Figure 4. The golden electrodes were post-fabricated on the surface of the die to contact directly with non-passivated aluminum pads. Each electrode is 100 microns high. The experimentally measured characteristics are summarized in Table I.

IV. Results

The functionality and utility of the presented integrated neural interface and spatio-temporal signal processor has been validated in experimental recordings from the mouse brain as well as in simulated spatio-temporal signal processing tasks performed on distributed brain activity recordings.

Figure 5 depicts an extracellular neural activity recording performed on one of the channels of the integrated neural interface. The recording is that of an epileptic seizure induced in the hippocampus of a mouse in vitro. Characteristic to

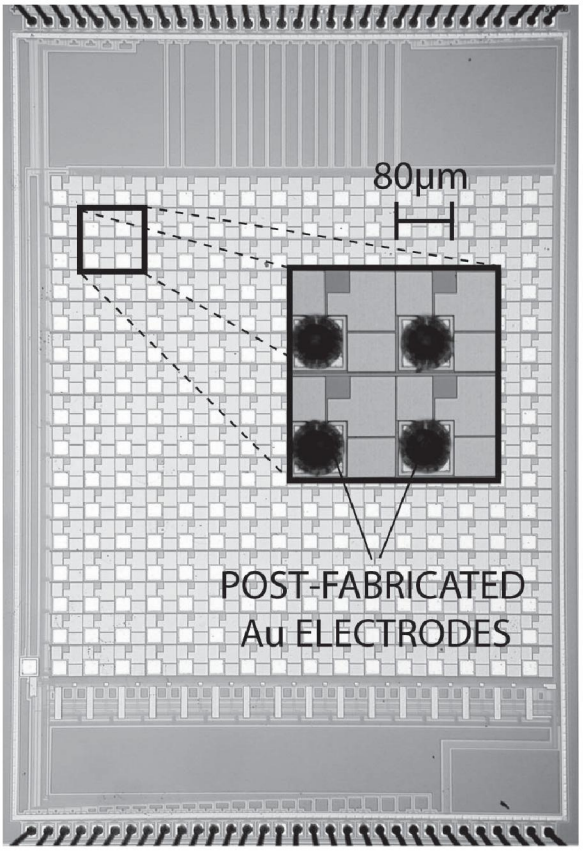

Fig. 4. Micrograph of the 256-channel integrated neural interface. The 3×4.5 mm^2 die was fabricated in a 0.35 μm CMOS technology. Electrode pitch is 170 μm.

TABLE I
EXPERIMENTALLY MEASURED CHARACTERISTICS

Channels	256
Max Sampling Rate	40kHz
Programmable Gain	200, 1000, 2500, 5000
Input-Referred RMS Voltage Noise	13µV over 10kHz
Output Voltage Range	1.5V
DC Offset Compensation	Double Sampling
LPF Cut-off Freq.	1kHz - 10kHz
HPF Cut-off Freq.	< 0.1Hz
Supply Voltage	3.3V
Core Power Dissipation	6mW
Technology	0.35µm, mixed-signal CMOS, double poly
Electrode type	On-chip, Au; 170µm pitch
Die Size	3 mm x 4.5 mm

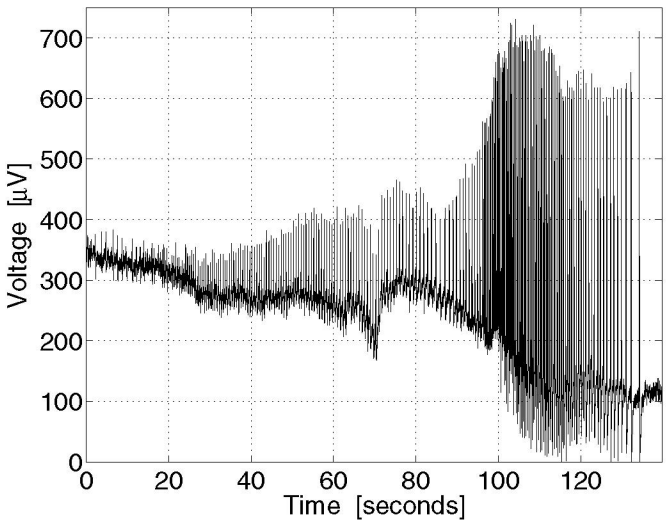

Fig. 5. Experimentally measured neural recording of a seizure in an intact hippocampus of a mouse.

a seizure are increase in the amplitude of the signal and transitions between oscillation states of different complexity.

To demonstrate the utility of the spatio-temporal neural signal processor, we simulate its frame differencing functionality and apply it to a distributed neural recording obtained optically using a voltage sensitive die. Figure 6 demonstrates a sequence of consecutive frame differences showing neural activity wave propagation in time. The frame differencing allows to identify the front of the neural activity wave and observe its propagation pattern over time. Such spatio-temporal processing when performed directly on the sensory plane opens up the opportunity to detect or predict states of particular neurological disorders such as epileptic seizures directly in an implant. Such capability may allow for local medical diagnostics and treatment directly on the neural implant.

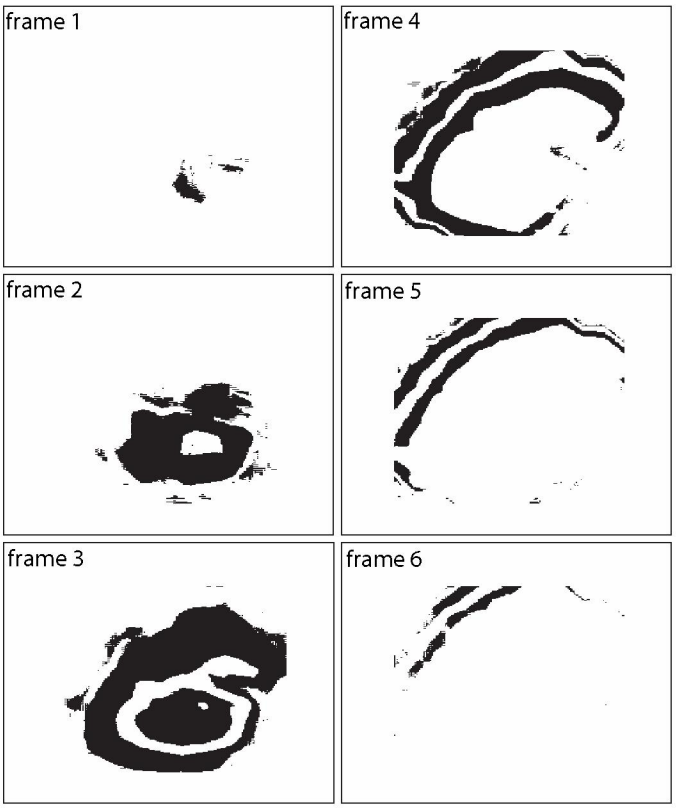

Fig. 6. The front of the neural activity wave obtained by frame differencing and thresholding computed on a distributed neural recording.

V. Conclusions

We have presented an architecture and VLSI implementation of a neural interface for distributed neural activity recording and spatio-temporal analysis. This work extends the field of integrated neural interfaces beyond signal acquisition and conditioning, to local on-chip intelligent signal processing. Such signal processing can be performed directly on an electronic implant, for data reduction in wireless sensory data transmission, and for automated medical diagnostics and therapy. A 3 mm $\times$ 4.5 mm 0.35 μm CMOS integrated prototype was validated in extracellular in vitro recordings and wavefront detection of distributed neural activity.

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