Electro-Chemical Multi-Channel Integrated Neural Interface Technologies

Joseph N. Y. Aziz

Department of Electrical and Computer Engineering University of Toronto Toronto, ON M5S 3G4, Canada Email: joseph@eecg.toronto.edu

Abstract— We present a comparative review of two multichannel integrated neural interface technologies. The first integrated neural interface prototype performs simultaneous currentmode acquisition of 16 independent channels of redox currents ranging five orders of magnitude in dynamic range over four scales down to hundreds of picoamperes. The second neural interface acquires neural field potentials in microvolts to millivolts range on a 16x16-electrode microarray in voltage mode. Each microsystem features programmable gain amplifiers, tunable band filters, configurable sample-and-hold circuits, and is ready for external analog-to-digital conversion. The currentmode and voltage-mode neural interface prototypes have been experimentally validated in chemical and electrical neural activity monitoring respectively. Side-by-side quantitative comparison of the two neural interface technologies is given.

I. INTRODUCTION

Electro-chemical activity of neurons typically exhibits considerable heterogeneity across biological ensembles. Sensory systems capable of recording on very many channels allow to capture, study and utilize this heterogeneity. The spectrum of electro-chemical neural activity often remains significant at higher frequencies (i.e., up to 10kHz). Time-multiplexed signal acquisition does not allow to accurately capture heterogeneity across biological ensembles as recording on different channels takes place at different time instances. This calls for sensory systems performing simultaneous signal acquisition on multiple channels, with one dedicated channel for each recording site.

Conventional bench-top signal acquisition instruments are bulky, expensive, and prone to interference noise due to wiring. They typically are stationary and provide only one or few recording channels. Single-chip neural interfaces offer a small size, low power, low noise and cost effective *chronically implantable* alternative to commercial bench-top instruments.

A number of integrated neural interface prototypes with more than two channels have been developed. The two dominant simultaneous sampling integrated neural interface technologies are those recording electric currents and voltages. The former perform chemical neural activity recording, while the latter monitor electrical neural activity. Currentacquisition neural interface microsystems, or potentiostats, record chemical concentrations of neurotransmitters by measuring reduction-oxidation currents. Recently reported inteRoman Genov

Department of Electrical and Computer Engineering University of Toronto Toronto, ON M5S 3G4, Canada Email: roman@eecg.toronto.edu

grated potentiostats [1], [2] employ oversampling data conversion techniques and achieve very high dynamic range, down to 8 pA currents, at the cost of reduced sampling rate of less than 30 samples per second. Voltage-acquisition microsystems record neural action potentials by measuring extracellular potential field. Existing designs trade between acquisition channel circuit area and intrinsic circuit noise. The 4×4 sensor array design reported in [3] achieves 9 μV RMS noise at the expense of 400 μm cell pitch. The 128 × 128 biosensor array design presented in [4] has 7.8 μm cell pitch at the cost of increased circuit noise.

In this paper we perform a comparative review of microsystems where signal processing is performed in the same signal-type domain as the signal being acquired, namely current-acquisition current-mode neural interfaces and voltageacquisition voltage-mode neural interfaces. Hybrid implementations are outside the scope of this paper. We present two integrated neural interface prototypes for simultaneous signal acquisition of currents and voltages on very many channels, for chemical and electrical sensing respectively. The current-acquisition microsystem, described in Section II, is implemented in current mode and can simultaneously sample 16 redox currents down to 46 pA with the sampling rate of up to 200 ksps. The voltage-acquisition voltage-mode neural interface, presented in Section III, simultaneously samples 256 action potentials on a 170 μm electrode grid with 13 μV RMS noise. The two neural interface technologies are quantitatively compared in Section IV to offer integrated neural interface design trade-off insights.

II. CURRENT-ACQUISITION CURRENT-MODE INTEGRATED NEURAL INTERFACE

For multi-site simultaneous chemical sensing, a currentacquisition current-mode integrated neural interface was designed, prototyped and experimentally characterized.

A. Architecture

The current-acquisition neural interface is a track-andhold potentiostat [5], [6] comprising 16 current-mode inputs, 4 voltage references setting the voltage levels of the virtualground current inputs in groups of 4, and a single full-range differential voltage output, all on a single chip. The block



Fig. 1. Block diagram of the current-acquisition integrated neural interface.

diagram of the single-chip potentiostat is given in Figure 1. Each of the 16 channels is independently configured for a gain of attenuation covering four orders of magnitude allowing to acquire bidirectional currents in the range from 46 pA to 50 μ A, at a reference voltage ranging from 0 to 5V. Programmable cut-off frequencies ranging from 50Hz to 400kHz prevent aliasing of high frequency components and allow to decrease the level of noise generated prior to sampling. The maximum fully sustained sampling rate ranges from DC to 200kHz. The outputs of the chip are pipelined and continuously valid, interfacing asynchronously to an external ADC on the PC host acquisition board for data post-processing.

B. VLSI Implementation

The input current to each data channel in Figure 1 is summed with a reference current I_{ref} , to convert the signal from bipolar to unipolar form. A transconductance amplifier drives a PMOS load transistor to provide a low impedance input stage. The acquired input current is then fed into a scaling circuit which normalizes the signal to the range [0, 1] μ A. The same scaling factor is used to attenuate the reference current I_{ref} at the input stage. The normalized current is fed into an anti-aliasing low-pass filter.

The integrator at the end of the channel is used for currentto-voltage conversion. The timing of integration in one of the reference channels (bottom of Figure 1), supplied a constant current equal to the normalized current range (1 μ A), sets the voltage range of conversion in the 16 channels. A 16-to-1 multiplexer selects the integrated signal of one of the 16 channels at the output. The output of the second reference channel, supplied half the current of the timing reference channel, serves as a 'zero-level' reference to the other channels in a differential output format, for reduced sensitivity to noise and power supply variations. In hold mode, the differential output from the previous integration cycle is buffered and held at the output while the current integration process is taking place.

The track-and-hold potentiostat was integrated on a $2.25 \times 2.25 \text{ mm}^2$ die fabricated in a 1.2 μ m double-poly CMOS



Fig. 2. Chip micrograph of the 16-channel current-acquisition integrated neural interface. Die size is $2.25 \times 2.25 \text{ mm}^2$ in a 1.2 μ m CMOS technology.

process. The chip micrograph is shown in Figure 2. Details on the circuits and characterization of the chip are presented in [5]. Experimentally verified electrical characteristics are summarized in Table I.

III. VOLTAGE-ACQUISITION VOLTAGE-MODE INTEGRATED NEURAL INTERFACE

For low-noise distributed neural potential field recording, a multi-channel voltage-mode integrated neural interface has been designed and prototyped.

A. Architecture

The voltage-acquisition neural interface records action potentials on 256 independent channels simultaneously. The voltage-mode signal acquisition circuits are organized in a 16×16 cell array as shown in Figure 3.

Each channel in the array contains a high-pass filter (HPF), a low-pass filter (LPF) and two amplification stages. Each channel also contains a sample-and-hold cell with double analog memory. A bank of correlated double sampling (CDS) cells sample the two analog memories, one row at a time, to remove offsets, resulting from device mismatches. Array readout is implemented in a serial fashion as controlled by row and column address decoders. Each channel is connected to on-chip differential recording electrodes through non-passivated topmost metal. Additional circuitry for optional post-fabrication electrode electroplating is also included.

B. VLSI Implementation

A single-stage wide-swing cascoded transconductance amplifier with p-channel MOS input differential pair is employed, both for the preamplifier and the amplifier in each signal acquisition channel. The transconductance amplifier is optimized for RMS noise of 13 μV under the 170 μm pitch cell integration area constraint and 6mW overall power dissipation constraint.



Fig. 3. Block diagram of the voltage-acquisition integrated neural interface.

The low noise amplifier design procedure employed is detailed in [7].

High pass filtering prevents DC signals, generated at the electrode-tissue interface, from saturating the amplifiers. The HPF is implemented as a frequency selective feedback of the pre-amplifier [7]. Post processing of the neural recording is performed in the discrete domain by means of switched capacitor circuits. The sampling from continuous time to discrete time requires anti-aliasing low pass filtering. The LPF filter is implemented by starving the bias current in the amplifier. Double sampling is performed by single-ended cascoded common-source amplifiers in a switched capacitor configuration.

Accurate distributed multi-site sensing requires maintaining a high degree of correlation in time between all the samples. Time-multiplexed recording architectures do not allow for such correlation. This necessitates a double memory buffer in each sensory cell to sample and store the recorded value. Frames of samples across the whole array are captured simultaneously. This eliminates the rolling delay during serial read-out. The local memory cell also allows for time-multiplexed memory readout in order to reduce noise due to substrate coupling. Low-noise signal acquisition is time-multiplexed with highnoise peripheral switch capacitor signal processing and readout. This ensures no high-amplitude switching activity during the signal acquisition phase and thus prevents substrate noise from coupling into the low-amplitude signal being acquired.

The 256-channel integrated neural interface and signal processor was fabricated on a $3 \text{mm} \times 4.5 \text{mm}$ die in a $0.35 \ \mu m$ double-poly standard CMOS technology. The die micrograph is shown in Figure 4. The golden electrodes were post-fabricated on the surface of the die to contact directly with non-passivated aluminum pads (not shown). The

Fig. 4. Chip micrograph of the 256-channel voltage-acquisition integrated neural interface. Die size is $4.5 \times 3 \text{ mm}^2$ in a 0.35 μm CMOS technology.

experimentally measured characteristics are summarized in Table II.

IV. NEURAL INTERFACE TECHNOLOGIES COMPARISON

Table I and Table II offer a side-by-side comparison of the characteristics of the current-acquisition and voltageacquisition neural interfaces prototypes. The tables offer insights into current-mode versus voltage-mode technologies for implementing current-acquisition and voltage-acquisition neural interfaces respectively. Design parameters such as channel area density, signal bandwidth, sampling rate, dynamic range, and power dissipation per channel represent various tradeoffs in voltage-mode and current-mode technologies. These should be taken into account when designing a custom neural interface.

Current-mode implementations are suitable for direct chemical sensing, while voltage-mode implementations are suitable for direct electrical sensing. The current-acquisition potentiostat simultaneously transduces neurotransmitter activity at multiple locations in the brain tissue, e.g., in synaptic clefts. The neural interface acquires oxidation-reduction currents generated at the surface of each sensing electrode. The voltageacquisition neural interface monitors a two-dimensional action potential field within a brain tissue area under observation. These technologies allow to study various neurophysiological phenomena such as those in sensory-motor systems, hippocampus, auditory nerve and visual cortex. The availability of the vast amount of data recorded simultaneously from many distributed sites is necessary in studying and analyzing heterogeneity across neural populations. Dual implementations with



TABLE I CURRENT-ACQUISITION CURRENT-MODE NEURAL INTERFACE MEASURED CHARACTERISTICS

Channels	16			
Max Sampling Rate	200kHz			
Input Current Range	-50nA- +50nA	-500nA- +500nA	-5μΑ– +5μΑ	-50μΑ– 50μΑ
Input Resolution	46pA	1nA	8nA	25nA
DC Offset	+/-5mV	+/-5mV	+/-5mV	+/-10mV
Input Impedance	125Ω			
LPF Cut-off Freq.	50Hz - 400kHz			
Output Volt. Range	0-5V			
Power Suppl. Volt.	-2V; +7V			
Power Dissipation	12.5mW			
Technology	1.2µm, BiCMOS (vertical NPN), double poly			
Electrode type	Off-chip			
Die Size	2.25 mm x 2.25 mm			
Sensor Type	Chemical			
Sensory Input	Redox Current			

both current acquisition and voltage acquisition capabilities may be suitable for general-purpose electro-chemical neural activity recording.

V. CONCLUSION

We presented a current-acquisition and a voltage-acquisition neural interfaces for simultaneous distributed multi-site electrical and chemical activity monitoring. The multi-channel architectures for both signal acquisition microsystems were introduced and VLSI implementations discussed.

The current-mode neural interface has 16 independent acquisition channels for simultaneous recording of redox currents with an input dynamic range spanning over five orders of magnitude down to 46 pA. The sampling rate can be programmed in the range from DC to 200kHz. The power consumption is 12.5 mW at the maximum sampling rate.

The voltage-mode neural interface has a 16 \times 16 array of voltage acquisition cells for two-dimensional simultaneous recording of extracellular action potentials. The input voltage ranges from 50 μV to 500 μV , with an **RMS** input referred noise of 13 μV measured over 10kHz bandwidth. The power consumption is 6 mW.

Side-by-side qualitative comparison of the two approaches was made to offer insights into design trade-offs between voltage-mode and current-mode neural interface technologies for electro-chemical neural activity monitoring.

TABLE II

VOLTAGE-ACQUISITION VOLTAGE-MODE NEURAL INTERFACE MEASURED CHARACTERISTICS

Channols	256		
	238		
Max Sampling Rate	40kHz		
Programmable Gain	200, 1000, 2500, 5000		
Input-Referred RMS Voltage Noise	13μV over 10kHz		
DC Offset Compensation	Correlated Double Sampling		
HPF Cut-off Freq.	< 0.1Hz		
LPF Cut-off Freq.	1kHz - 10kHz		
Output Voltage Range	1.5V		
Power Suppl. Volt.	3.3V		
Core Power Dissipation	6mW		
Technology	0.35µm, mixed-signal CMOS, double poly		
Electrode Type	On-chip; 170µm pitch		
Die Size	3 mm x 4.5 mm		
Sensor Type	Electrical		
Sensory Input	Action Potential		

REFERENCES

- M. Stanacevic, K. Murari, G. Cauwenberghs, and N. Thakor, "16channel wide-range VLSI potentiostat array," *IEEE International Work*shop on Biomedical Circuits and Systems, December 1-3, 2004.
- [2] K. Murari, N. Thakor, M. Stanacevic, and G. Cauwenberghs, "Wide-Range, Picoampere-Sensitivity Multichannel VLSI Potentiostat for Neurotransmitter Sensing," *Proc. 26th Ann. Int. Conf. IEEE Engineering in Medicine and Biology Society (EMBS'2004)*, San Francisco, September 1-4, 2004.
- [3] W.R. Patterson, Yoon-Kyu Song, C.W. Bull, I. Ozden, A.P. Deangellis, C. Lay, J.L. McKay, A.V. Nurmikko, J.D. Donoghue, and B.W. Connors, "A microelectrode/microelectronic hybrid device for brain implantable neuroprosthesis applications," *IEEE Transactions on Biomedical Engineering*, vol. **51** (10), October 2004.
- [4] B. Eversmann, M. Jenkner, C. Paulus, F. Hofmann, R. Brederlow, B. Holzapfl, P. Fromherz, M. Brenner, M. Schreiter, R. Gabl, K. Plehnert, M. Steinhauser, G. Eckstein, D. Schmitt-Landsiedel, and R. Thewes, "A 128 × 128 CMOS bio-sensor array for extracellular recording of neural activity," *IEEE Journal on Solid-State Circuits*, pp. 2306 - 2317, vol. **38** (12), February 2003.
- [5] R. Genov, M. Stanacevic, M. Naware, G. Cauwenberghs, and N. Thakor, "VLSI Multi-Channel Track-and-Hold Potentiostat," in *Microtechnologies for the New Millennium, Bioengineered and Bioinspired Systems* 2003, Proc. SPIE vol. **5119**, May 2003.
- [6] M. Naware, A. Rege, R. Genov, M. Stanacevic, G. Cauwenberghs, N. Thakor, "Integrated Multi-Electrode Fluidic Nitric-Oxide Sensor and VLSI Potentiostat Array," *IEEE Int. Symp. on Circuits and Systems* (ISCAS'2004), Vancouver, May 2004.
- [7] R.R. Harrison, and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE Journal on Solid-State Circuits*, vol. **38** (6), pp. 958-965, June 2003.
- [8] C.C. Enz, and G.C. Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," *Proceedings of the IEEE*, vol. 84 (11), pp. 1584-1614, November 1996.