CMOS Current-Copying Neural Stimulator with OTA-Sharing

Ruslana Shulyzki, Karim Abdelhalim, Roman Genov
Department of Electrical and Computer Engineering
University of Toronto, Toronto, Canada
Email: {ruslana, karim, roman}@eecg.utoronto.ca

***Abstract*— We present a compact current mode stimulator for utilization in neural stimulation arrays. The stimulator is implemented in a 0.35μm CMOS technology and occupies an area of 50μm$\times$400μm. The memory in every current driver allows for simultaneous stimulation on multiple active channels when used as part of an array of stimulators. Circuit reuse in the stimulator and utilization of a single DAC yield a compact and low-power implementation. The current driver dissipates a quiescent power of 2.76μW. The stimulator can output current in the range of 10μA - 250μA.**

I. Introduction

Neural stimulation arrays have been employed in implantable medical devices such as cochlear and retinal prostheses [1]–[3]. Electrical stimulation of excitable neural tissue occurs whenever charge is delivered to the tissue through an electrode. Safety is a major concern in the design of implantable neural stimulators. Adverse chemical reactions such as electrolysis, pH changes and tissue and electrode damage can occur whenever the tissue is exposed to prolonged DC currents or anything else that results in charge accumulation in the tissue. It is therefore essential that the stimulator provides maximum control over the charge delivered and retracted to and from the tissue, respectively. The issue of charge balancing has been under extensive research and various schemes and approaches have been used towards this goal as summarized in [4].

Neural stimulators typically employ one of three approaches to transfer charge to neural tissue. Constant current stimulation establishes a well controlled current between pairs of electrodes for a short amount of time. Constant voltage stimulation establishes current flow by controlling the voltage at the electrode site. Charge based stimulation utilizes switched capacitor networks to deliver charge directly to the tissue.

Voltage controlled neural stimulation has the advantage of higher power efficiency [5] and was implemented in [6]. The main drawback of voltage controlled stimulation however is the lack of control over the charge delivered to the tissue. Tissue impedance varies from a nominal value of 10kΩ due to cellular reactions [7]. Also, since the electrode tissue interface has a capacitive component, the instantaneous current between electrodes is not well controlled. Current controlled neural stimulation offers direct control over the charge delivered to the tissue due to the linear relationship between charge and current. Currents in the range of 10μA - 1mA typically invoke a neural response [8]. Microstimulation currents typically range up to 250μA [9].

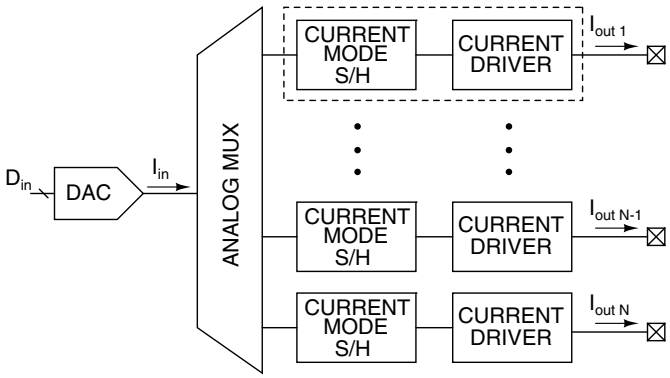

Fig. 1. Envisioned stimulation array.

It is desirable to have maximum control over the stimulation waveform. Stimulators usually contain a digital-to-analog converter (DAC) to control the output signal amplitude. Some designs use current mode DACs as the output stage of the stimulator [3], [10], [11], others use a voltage mode DAC and interface it with a voltage-to-current converter circuit [12]. For arbitrary waveform generation, which provides the highest functional flexibility, high signal resolution is required. The resolution is limited by the area allocated for the stimulator, since a DAC is commonly incorporated in every channel. A stimulator array that does not require a dedicated DAC at every output stage would reduce the area and the power consumption of a multi-channel neural stimulation system.

For maximum functional flexibility the stimulator array has to stimulate simultaneously at multiple electrode sites. This capability requires the incorporation of memory into every stimulator block. Stimulators that are integrated with DACs will need digital memory with an area that is proportional to the bit resolution of the DAC. Sharing a DAC among all the stimulators in the array requires an accurate method to store the output signal information in analog form.

We present a 0.35μm CMOS VLSI implementation of a current mode stimulator that can be easily integrated in a multi-channel stimulator array, as illustrated in Figure 1. The stimulator is fully programmable with square or arbitrary shape waveforms. The memory in the stimulator allows for si-

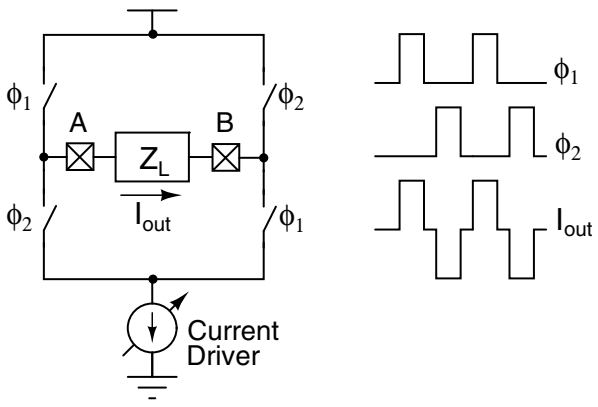

Fig. 2. A general implementation of biphasic stimulation.

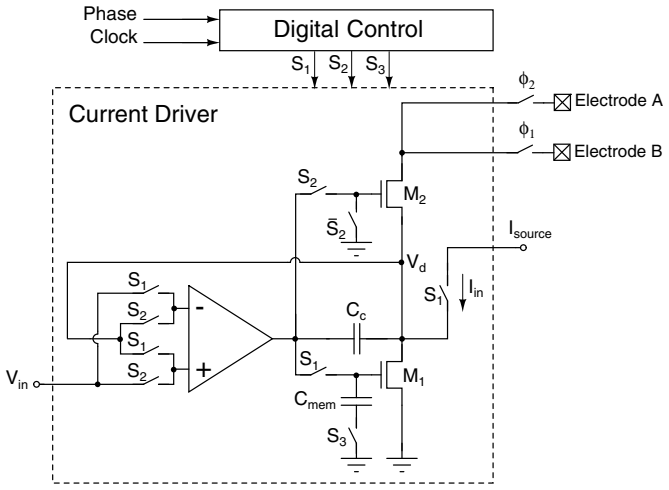

Fig. 3. Neural stimulator architecture.

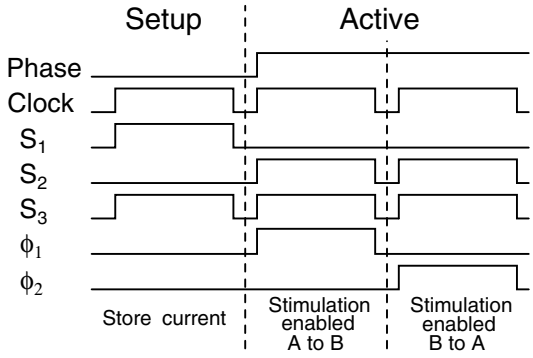

Fig. 4. Timing diagram for implementing a biphasic stimulus.

multaneous stimulation on multiple active channels when used as part of an array of stimulators, which can not be achieved with conventional time multiplexing. The neural stimulator occupies only $0.02mm^2$. This is achieved by re-using the opamp in the stimulator in two different configurations, and not requiring a local DAC. These techniques also result in low quiescent power consumption of 2.76μW per stimulator.

The rest of this paper is organized as follows. Section II describes current controlled biphasic stimulation. Section III presents the architecture of the neural stimulator. Section IV describes the design of the current driver used in the stimulator. Section V presents the experimental characterization of the stimulator.

II. Biphasic Current Controlled Stimulation

In this design current controlled stimulation was implemented due to the control it provides over the charge delivered to the tissue. The stimulator is designed to supply biphasic stimulation current to the tissue with impedance Z_L as illustrated in Figure 2.

During the anodic phase, ϕ_1 is high and the current is flowing from electrode A to electrode B. During the cathodic phase ϕ_2 is high and current is flowing from electrode B to electrode A. The amplitude and duration of the current pulses during the two phases need not be the same. As long as the area under the two waveforms is the same the charge that was delivered to the tissue is retracted from the tissue. The stimulator is fully programmable and the amplitude and the duration of each pulse can be set independently.

III. Neural Stimulator Architecture

Precise current control is essential in the current driver design. High accuracy and linearity are important design considerations. In addition, due to the variable nature of the load impedance the output impedance of the current driver has to be high in order to deliver a constant current under a wide range of conditions.

There are several approaches to setting the output current of the current driver. The design in [12] utilizes a voltage controlled resistor, whose gate voltage is controlled by the voltage-mode DAC. The design in [10] includes binary-weighted transistors acting as a current-mode DAC. Other designs, [13], [3], sink the current with the output stage of a current mirror, the input to which is set by a current-mode DAC. The common factor in all of these designs is the incorporation of a DAC in every current driver which requires larger area, and lack of storage which does not support truly simultaneous stimulation on all channels.

The choice of the neural stimulator architecture was dictated by the low area, low power and high output impedance design constraints. The neural stimulator consists of two major blocks: digital control and a current driver. This is illustrated in Figure 3.

The stimulator operates in two phases: setup phase and active phase. $Clock$ and $Phase$ inputs configure the switch network to put each site into its desired operation mode. During the setup phase the stimulation current is stored in the current driver memory. During the active phase the current driver is connected to one of the electrodes and current is allowed to flow through the load. One biphasic stimulation cycle is illustrated in Figure 4.

The current driver achieves the task of storing the stimulation current and stimulating through the same signal path, without requiring a DAC in every stimulator circuit. This

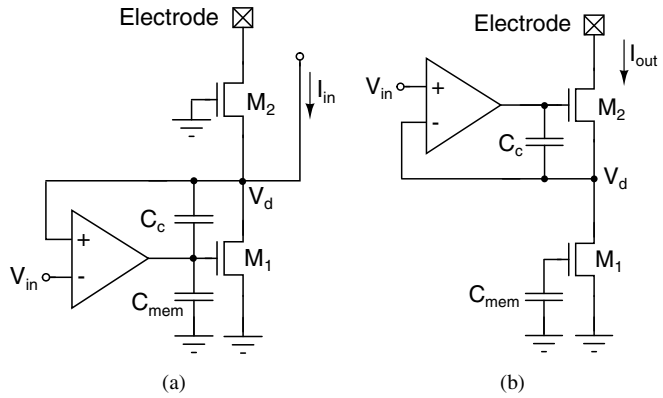

Fig. 5. Current sink configured in (a) storage mode and (b) stimulation mode.

provides an advantage in terms of accurate current copying, small area and low power consumption.

IV. Current Driver

The main components of the current driver are an operational transconductance amplifier (OTA), and two transistors M_1 (4×5.5μm/0.5μm) and M_2 (4×8μm/0.5μm). These components are configured with switches into two different circuits for the purposes of current storage (during setup phase) and current driving (during active phase). The two circuits can be seen in Figure 5.

Figure 5(a) shows the current driver configured for current storage. In this state the circuit is a constant V_{DS} current copier [14]. The desired current is flowing through transistor M_1 which is biased in saturation region. The drain voltage of transistor M_1 is held constant at the potential approximately equal to V_{in} through the OTA feedback, which prevents variation in the output current due to the effect of channel length modulation. The gate voltage of M_1 is driven by the OTA to the proper level corresponding to current I_{in} and is stored on capacitor C_{mem} (200fF).

Figure 5(b) shows the current driver during the active phase, configured as a typical current sink. The negative feedback around M_2 serves two purposes. First it boosts the output impedance of the current sink. This is a well established gain boosting technique that by increasing the output impedance of the current driver makes it less sensitive to the load impedance [10], [12]. Second, it forces the drain voltage of M_1 to the potential V_{in}. This together with the gate voltage that is set by C_{mem} ensures that the current that flows through it is as close as possible to the current during the storage phase.

Capacitor C_c (300fF) is a compensation capacitor and it is used to stabilize node V_d during the switching from one configuration to the other.

The incorporation of analog memory in the current driver has two benefits. First, area is saved because the DAC can be placed outside of the cell and shared by many channels. Second, stimulation can be performed on multiple sites simultaneously.

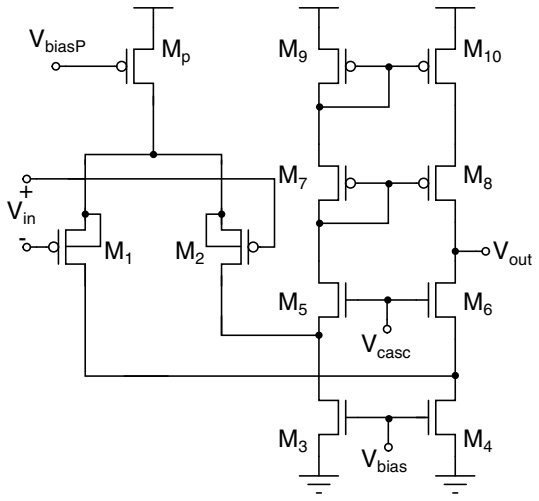

Fig. 6. Folded-cascode OTA in the stimulator current sink.

TABLE I
Stimulator OTA transistor sizing

Transistor	W/L (μm)
$M_{1,2}$	$2/4$
$M_{3,4}$	$1/5$
$M_{5,6}$	$1/6$
$M_{7,8}$	$1/4$
$M_{9,10}$	$1/4$
M_p	$1/5$

A. Operational Transconductance Amplifier

To maximize the output impedance of the current sink the OTA needs to have a large gain as seen from

$$R_{out} \approx A g_{m2} r_{o2} r_{o1}, \quad (1)$$

where A is the gain of the OTA, g_{m2} is the transconductance of transistor M_2, r_{o2} is the output impedance of transistor M_2 and r_{o1} is the output resistance of transistor M_1.

The OTA has a PMOS input folded-cascode configuration, as shown in Figure 6. It provides a gain of 93dB at a common mode input of $V_{in} = 300m$V. The OTA consumes a bias current of 0.88μA. The transistor sizes are given in Table I.

V. Experimental Characterization

The neural stimulator presented here was prototyped in a 0.35μm CMOS technology. It was experimentally characterized by loading through an external resistor connected between the current driver output and VDD. Figure 7 compares the experimentally measured and simulated input-output characteristics of the current driver. The output current is lower than the input current due to the effects of charge injection at the gate of transistor M_1. Due to the systematic nature of this error the mismatch can be compensated through calibration.

Figure 8 shows the simulated and measured output of the current driver under variable load conditions. The plot demonstrates the operating region of the current driver. The

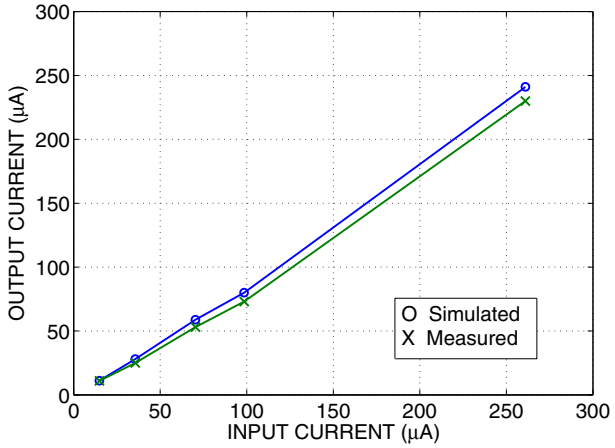

Fig. 7. Transfer characteristic of the current driver for 10kΩ load.

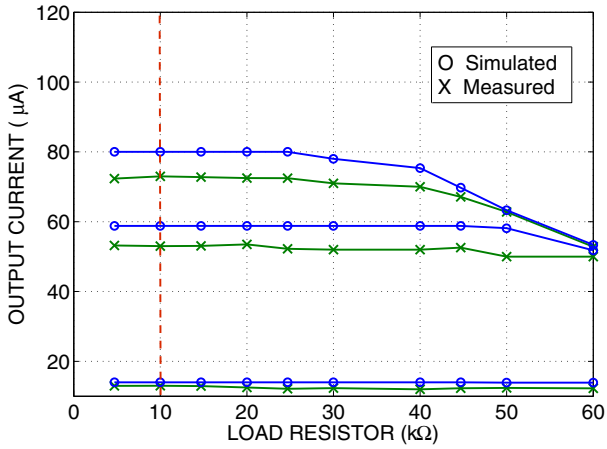

Fig. 8. Output of the current driver under variable load conditions.

voltage at the electrode site can be as low as 700mV, resulting in a voltage compliance of 2.6V if the supply voltage is set to 3.3V. Currents above 250μA will drive the circuit out of the linear region even for the nominal load of 10kΩ.

The experimental results for the neural stimulator are summarized in Table II.

VI. Conclusions

We have presented a current mode neural stimulator for utilization in neural stimulation arrays. Circuit reuse and incorporation of current memory in the stimulator result in a compact low-power design. The stimulator occupies a total area of $0.02mm^2$ and has a quiescent power consumption of 2.76μW. These attributes make the design suitable for use in high density stimulation arrays, where power and area are major constraints.

Acknowledgment

The authors thank the Canadian Microelectronics Corporation (CMC) for semiconductor fabrication services and Canada Foundation for Innovation (CFI) and Natural Sciences and Engineering Research Council of Canada (NSERC) for their financial support.

TABLE II
STIMULATOR EXPERIMENTAL CHARACTERISTICS

Technology	0.35μm CMOS
Area	0.02mm^2
Stimulation mode	Current
Supply voltage	3V
Output current	10-250μA
Voltage compliance	2.6V
Power dissipation (quiescent)	2.6μW

References

[1] L Theogarajan, J Wyatt, J Rizzo, B Dorhan, M Markova, S Kelly, G Swider, M Raj, D Shire, M Gingerich, J Lowenstein, and B Yomtov, "Minimaly invasive retinal prosthesis," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, p. 54, February 2006.

[2] J Coulombe, M Sawan, and J-F Gervais, "A highly flexible system for microstimulation of the visual cortex: Design and implementation," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 1, no. 4, pp. 258–269, December 2007.

[3] Y Y Yao, M N Gulari, J F Hetke, and K D Wise, "A low-profile three-dimensional neural stimulating array with on-chip current generation," *Proceedings of the 26th Annual International Conference of the IEEE EMBS*, pp. 1994–1997, September 2004.

[4] M Ortmanns, "Charge balancing in functional electrical stimulators: A comparative study," *IEEE International Symposium on Circuits and Systems*, pp. 573–576, May 2007.

[5] J Simpson and M Ghovanloo, "An experimental study of voltage, current, and charge controlled stimulation front-end circuitry," *IEEE International Symposium on Circuits and Systems*, pp. 325–328, May 2007.

[6] F Shahrokhi, K Abdelhalim, and R Genov, "128-channel fully differential digital neural recording and stimulation interface," *IEEE International Symposium on Circuits and Systems*, pp. 1249–1252, May 2009.

[7] J C Williams, J A Hippensteel, J Dilgen, W Shain, and D R Kipke, "Complex impedance spectroscopy for monitoring tissue responses to inserted neural implants," *Journal of Neural Engineering*, vol. 4, pp. 410–423, November 2007.

[8] E. J. Tehovnik, "Electrical stimulation of neural tissue to evoke behavioral responses," *Journal of Neuroscience Methods*, vol. 65, pp. 1–17, 1996.

[9] B K Thurgood, D J Warren, N M Ledbetter, G A Clark, and R R Harrison, "A wireless integrated circuit for 100-channel charge-balanced neural stimulation," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 3, no. 6, pp. 405–414, December 2009.

[10] X Liu, A Demosthenous, and N Donaldson, "An integrated implantable stimulator that is fail-safe without off-chip blocking capacitors," *IEEE Transactions On Biomedical Circuits and Systems*, vol. 2, no. 3, pp. 231–244, September 2008.

[11] T G Constandinou, J Georgiou, and C Toumazou, "A partial-current-steering biphasic stimulation driver for vestibular prostheses," *IEEE Transactions On Biomedical Circuits and Systems*, vol. 2, no. 2, pp. 106–113, June 2008.

[12] M Ghovanloo and K Najafi, "A compact large voltage-compliance high output-impedance programmable current source for implantable microstimulators," *IEEE Transactions on Biomedical Engineering*, vol. 52, no. 1, pp. 97–105, January 2005.

[13] J. Lee, H. Rhew, D. Kipke, and M. Flynn, "A 64 channel programmable closed-loop deep brain stimulator with 8 channel neural amplifier and logarithmic ADC," *IEEE Symposium on VLSI Circuits*, pp. 76–77, June 2008.

[14] S J Daubert and D Vallancourt, "Operation and analysis of current copier circuits," *IEE Proceedings G Circuits, Devices & Systems*, vol. 137, pp. 109–115, April 1990.