Similarity-Index Early Seizure Detector VLSI Architecture

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***Abstract*— A low power VLSI architecture implementing an algorithm for early seizure detection in epileptic patients using intracranial or scalp EEG data is proposed. The algorithm tested over more than 40 hours of recording from standard databases achieves a best-case result of 100% sensitivity at a false positive rate of 0.2 per hour. The algorithm is programmed on an FPGA and was experimentally validated along with a neural recording SoC chip to demonstrate a real-time seizure detection microsystem.**

I. Introduction

According to WHO statistics, over 50 million people worldwide are affected by epilepsy, a chronic disorder of the brain, characterized by recurrent seizures – physical manifestations of spontaneous and excessive electrical discharges in certain collections of brain cells. The unpredictable nature of seizures is a major reason for the morbid nature of this disease, causing extensive emotional trauma to the patients and their families, as the risk of premature death in epileptic patients is two to three times the average. Anti-epileptic drugs are the primary method of treatment, but are shown to be effective only in 70% of patients. Another option is the surgical removal of sections of brain functioning as epileptic centers. However such surgeries are not always effective and may lead to loss of memory or some other brain functions. Patients not responsive to either medical treatment are said to be afflicted by intractable epilepsy, and neurologists believe that stimulating the right neuronal cells with short electrical pulses, preferably before the seizure onset can mitigate and even eliminate the approaching seizure event [1], [2].

A number of algorithms have been proposed for seizure detection and prediction, though there is still some debate regarding the exact definitions of prediction, detection and early detection. This paper deals with 'early detection' of an electrical seizure onset (ESO) as long as the indication arrives shortly before the clinical-seizure onset (CSO) (i.e., physical manifestation). Several researchers have reported neural signal sensing and stimulation microsystems all on one chip, which hold potential for an implantable device [3]. Commercial products have also been brought into the market. A particular example is Neuropace, which first offered continuous stimulation and now the device comes with an algorithm which learns patient pathological brain states and stimulates accordingly. However there are still areas of improvement in detection performance and in low-power operation.

This paper presents an early seizure detector digital VLSI architecture based on similarity index that minimizes area and power making it suitable for an implantable device. The rest of the paper is organized as follows. Section II discusses the system-level VLSI architecture of the early seizure detector. Section III presents a classification of popular algorithms and describes in detail the concept of similarity index-based algorithm. Section IV describes the VLSI implementation of the algorithm. Section V shows simulation and experimental results.

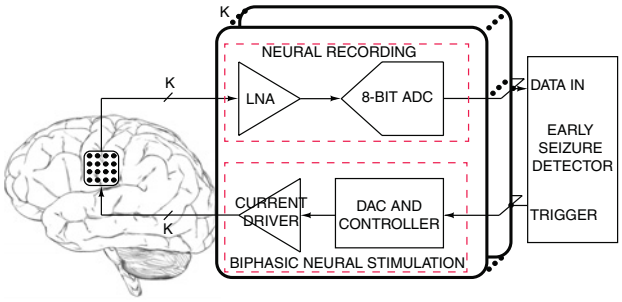

Fig. 1. Proposed early seizure detector and stimulator.

II. System Level VLSI Architecture

An electrode array such as ECoG connects to the closed-loop system as displayed in Figure 1 and consists of a set of K scalable channels which include a neural recording and biphasic neural stimulation interface. The neural recording interface uses a compact AC-coupled amplifier with an integrated noise below 10μV from 1Hz to 5kHz bandwidth and a gain of 60dB followed by an 8-bit low power ADC. All recorded neural signals are sent to an early seizure detector which is implemented in the digital VLSI domain.

For a large numbers of channels (greater than 64), data rates reach well above 1MB/s. Implementing an area and power-efficient seizure detector allows for the possibility of computing on all channels and remain in the power budget constraints for safe implantation. If the early seizure detector detects an event, a trigger signal is sent to the biphasic neural stimulator controller to evoke a biphasic current pulse stimulation. The biphasic current pulses are between 10μA and 1mA, with frequencies between 10Hz and 1kHz.

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III. Early Seizure Detection Algorithms

A. Categories of Algorithms

Most of the seizure detection or prediction schemes fall into two major categories: univariate and bi/multivariate algorithms. An example of a bivariate method is the phase synchrony based algorithm [6]. The main advantage of a bi/multivariate method is that the algorithm can incorporate the spatial information available as the discharge spreads across different regions of the brain, something not possible to extract from a single electrode. This usually results in more accurate detections, at the cost of increased chip area and power dissipation. These parameters are critical, especially when designing an implantable chip and have to be carefully minimized. This is where univariate methods are better, as the algorithms are simple and can be implemented at a very low hardware implementation cost.

Most of the univariate algorithms are based either on frequency and wavelet analysis [7] or on statistical and time series analysis [8] which extract certain features found prevalently in the pre-ictal (before the seizure onset) or ictal (during the seizure) periods. This paper explores one such attribute, the similarity index of a time series, which is related to the long and short term dependencies within the series.

B. Similarity Index and its Properties

Similarity index, sometimes known as the Hurst exponent or the Holder exponent *(H)* is used to characterize the long-term memory or dependence of a stochastic process, and is usually estimated using the time series as one of the realizations of the process. The definition of *H* for a time series $X_1, X_2, ..., X_n$ [4] is

$$H = \frac{log(R(n)/S(n))}{log(n)}$$

where *R/S* is called the rescaled range, *R* is the range and *S* is the standard deviation of the data in consideration. Both are measures of deviation, *R* is dependent on the range of the sum of data values and *S* is related to a sum of squares of the same. These can be calculated as

$$R(n) = max(Z_1, Z_2, ..., Z_n) - min(Z_1, Z_2, ..., Z_n)$$

$$S(n) = \sqrt{\frac{1}{n}\sum_{i=0}^{n}(X_i - m)}$$

where m is the mean of X_i, for i = 1, 2, ..., n,

$$Z_t = \sum_{i=1}^{t} Y_i,$$

and

$$Y_i = X_i - m.$$

Theoretically, the value of *H* lies between 0 and 1. For a Gaussian white process it is 0.5. Above this value, there is positive correlation in the series (a high positive value is likely to be followed by another large positive value) and a value below 0.5 indicates negative correlation (a high likelihood of switching). Typically, three methods are used to estimate the Hurst exponent based on historical data, from discrete second derivatives of the series [9], from discrete wavelet coefficients [5] or from log-log regression of detail variance versus level directly based on the definition [10].

In this paper, the method of discrete second derivatives was chosen due to its simplicity and ease of implementation in a VLSI architecture with minimum hardware resources. This estimate is inspired by the work of Istas and Lang [9] on point-wise Holder parameter estimation for fractional brownian motion, given by

$$H_e = \frac{1}{2}\left(1 + \frac{log\, V_N}{log\, N}\right),$$

$$V_N = \sum_{i=1}^{N-2}(X_{i+2} - 2X_{i+1} + X_i)^2,$$

where *N* is the number of discrete samples of process X_i available. A modification of this approach is

$$H_e = \frac{1}{2}\left(log(W_N/V_N)\right), V_N = \sum_{i=1}^{N-2}(X_{i+2} - 2X_{i+1} + X_i)^2$$

$$W_N = \sum_{i=1}^{N-4}(X_{i+4} - 2X_{i+2} + X_i)^2.$$

Both of these approaches were tested on human seizure data, and though they provide similar results the second one was chosen due to its slightly higher performance and the fact that an implementation of the latter encompasses the former.

Once the *H* value is estimated (H_e), it is averaged depending upon the noisiness of the estimate after which the information contained in it is converted into a seizure prediction or detection. For this, the incoming data is windowed and then an $H_e$value is calculated for each window, akin to finding a dynamical similarity index for the complete process. A large deviation from the long-term mean across windows signals a change in the dependence or correlation of the process, and can be thought of as an indication of an impending seizure [11]. To achieve this, current H_e value is compared against a running mean of past values, and if the value rises above or falls below a threshold, a trigger signal is activated. To correct for the effect of noise in the data, two thresholds are used, a fixed one and another pegged to the variance (or standard deviation) of the estimate. The higher the variance, the more likely the chance of deviations from the mean due to noise is (unrelated to any seizure activity), resulting in fewer false triggers. This introduces two key parameters into the algorithm, the fixed threshold parameter (ftp) and the amount by which threshold depends on the variance or the variance pegged parameter (vpp). These parameters determine the efficacy of the algorithms and should be adjusted for

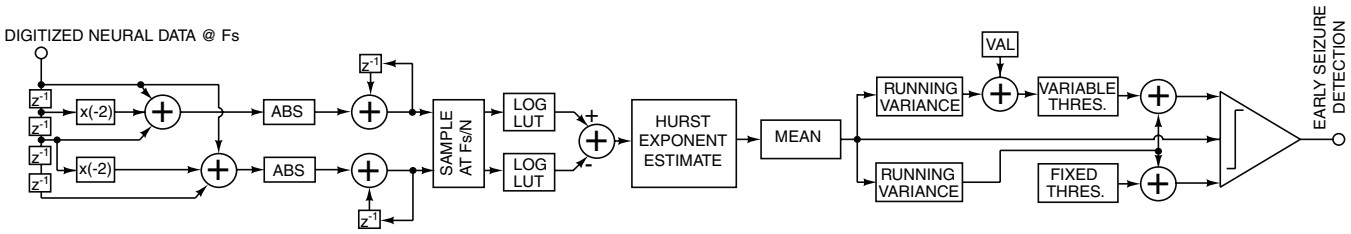

Fig. 2. VLSI architecture of the similarity index algorithm which sets the trigger signal based on the Hurst exponent estimate.

a particular patient and testing setup. Setting of the trigger indicates an impending seizure. The mean is given as

$$\hat{H} = \frac{1}{M}\sum_{i=1}^{M} H_e(i),$$

where i is the window index, M is number of windows used to find the mean. The variance is given as

$$Var = \frac{1}{M}\sum_{i=1}^{M}(H_e(i) - \hat{H})^2,$$

The trigger is set as follows

$$Trig = 1,\ if\ |H_e(j) - \hat{H}| > ftp\ and$$
$$|H_e(j) - \hat{H}| > vpp \times Var,$$

where j is the current window index.

IV. VLSI Implementation of Similarity Index Algorithm

To reduce hardware complexity, additional simplifications were added to the algorithm already described. They are replacing squaring by absolute value operation and restricting parameter values to powers of two to eliminate multipliers. The complete architecture shown in Figure 2 was designed for an 8-bit word length, based on the resolution of the on-chip ADC used to sample the neural data. It consists of first finding the second derivatives based estimate of similarity index using multiplier-less implementation of filtering-like operations followed by a look-up table (LUT) realization of the scaled log-function. The local estimate is then compared against the running mean of past values, for which the mean of a 128 or 256 (depends on patient, operating conditions and sampling frequency) past values is calculated and stored, using only one adder and an memory element. This method creates a maximum initial latency of up to a few seconds, but this can be safely ignored in continuous real-time operation of the system. The variance is calculated in a similar manner and the fixed threshold parameters are derived from simulation through the ROC plots. Finally the current value is compared with the mean to generate a trigger output which indicates a possible seizure occurrence.

This architecture was implemented and simulated in a VHDL logic synthesizer, to verify the accuracy of the design, followed by programming on an Altera FPGA included in the system. The resources used by the Altera FPGA are 361 logic elements, 199 dedicated registers and a memory of 64-bits for implementing a scaled version of a log LUT.

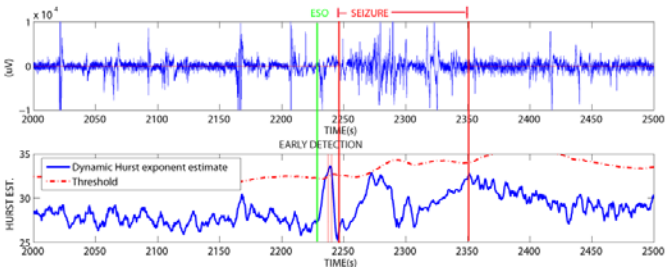

Fig. 3. The top plot shows the seizure data. The bottom plot shows the Hurst exponent estimate and its running mean, with computed trigger falling between ESO and CSO.

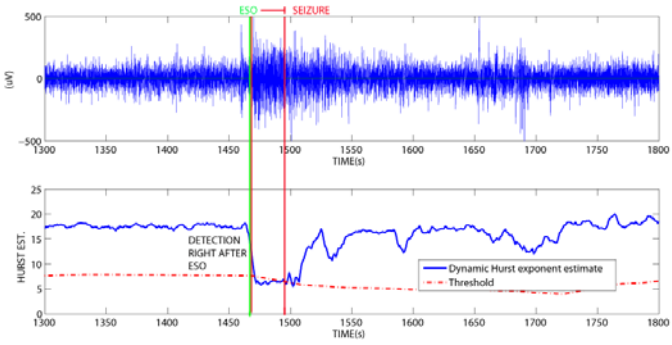

Fig. 4. The top plot shows the seizure data. The bottom plot shows the Hurst exponent estimate and its running mean, showing the computed trigger falling just after ESO is identified.

V. Simulated and Experimental Results

The VLSI architecture was first simulated in MATLAB, and tested over two data sets of labeled human data to create ROC plots and check the efficacy of the algorithm. The first set of results is from the Freiburg dataset [12] shown in Figure 3; tested segment consisting of 30 hours of intracranial EEG data from one patient. Out of these, 10 hours are purely interictal, while 20 hours contain 6 events of seizure activity. There were multiple electrodes, of which the one found to be the closest to the epileptic center was used in the algorithm. The second dataset is from MIT's Physionet bank [13] which contains scalp EEG data, with the corresponding results described in Figure 4. Here 10 hours of data containing 7 seizures from one patient were tested. There is no clear criteria for electrode selection, so a random choice was made as most of the

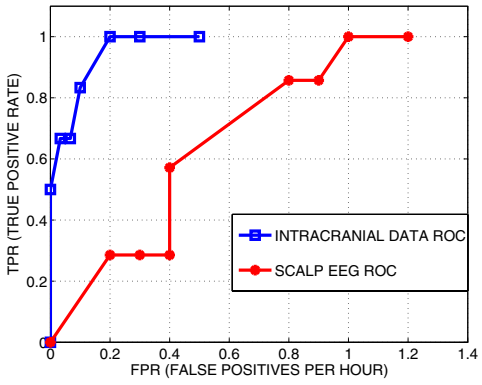

Fig. 5. ROC plots for Freiburg and MIT Physionet data sets.

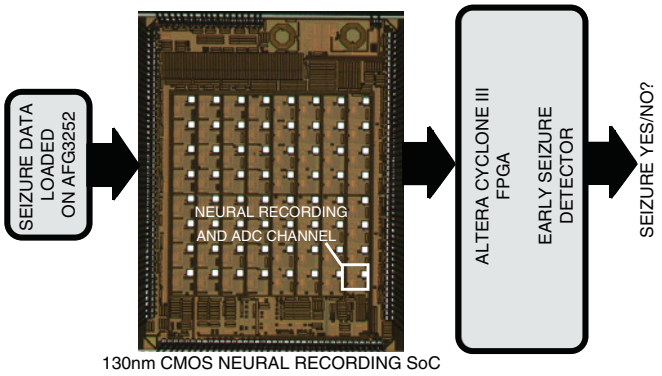

Fig. 6. Experimental setup of early seizure detector.

electrodes give similar results. This has a lower SNR compared to intracranial EEG data resulting in a decrease in performance which is reflected in the corresponding areas under the ROC plots in Figure 5.

The test setup is shown in Figure 6. The details of the neural recording SoC are described in [14]. The algorithm was programmed onto an FPGA and pre-recorded seizure data were played through an arbitrary signal generator. The signal levels were set to 100μV to enable low SNR measurements. The data was amplified by an amplifier on the SoC with an integrated noise of 6.5μV between 1 and 5kHz and digitized

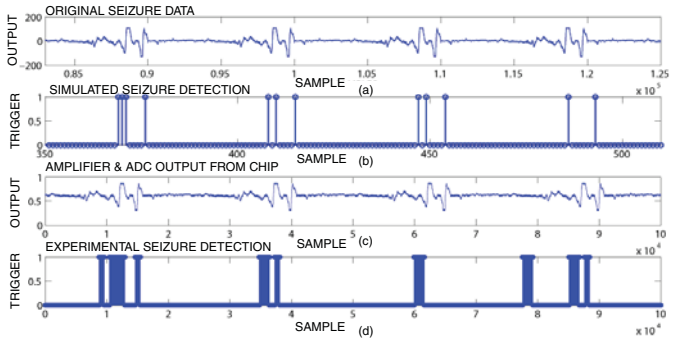

Fig. 7. (a) Original seizure data. (b) Simulated seizure detection results. (c) Output showing the seizure data after being amplified and digitized by the SoC. (d) Experimental seizure detection as a result of the neural recording data being fed by the SoC to the FPGA and processed on the FPGA.

using an ADC with an ENOB of 7.8-bits at 20kS/s. The seizure detection was performed in real time with one channel selected from the chip and its 8-bit ADC output connected to the input of the FPGA.

The seizure is shown in Figure 7(a) and the simulated VHDL result is shown for the seizure detection in Figure 7(b). The amplified and digitized output of the seizure recorded from the SoC as shown in Figure 7(c). This quantized signal was sent to the FPGA in real time resulting in the trigger output, as shown in Figure 7(d).

VI. Conclusions

A compact similarity-index based early seizure detector VLSI architecture was presented. The architecture was validated through RTL-level simulations with standard intracranial and scalp EEG databases and achieves 100% sensitivity with a false positive rate of 0.2 per hour and 1.0 per hour, respectively. It was also programmed on an Altera Cyclone III FPGA and experimentally validated together with a neural recording SoC.

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