16-CHANNEL SINGLE-CHIP CURRENT-MODE TRACK-AND-HOLD ACQUISITION SYSTEM WITH 100 DB DYNAMIC RANGE

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ABSTRACT

Testing of mixed-mode VLSI systems demands specialized instrumentation tools to simultaneously source and track multiple analog and digital signals. We present a single-chip solution for synchronous acquisition of 16 channels of independent currents, ranging five orders of magnitude in dynamic range over four scales. The digitally programmable chip is one component in an integrated system that we developed with 64 analog and 64 digital I/O channels, for timed instrumentation of micropower VLSI systems covering subthreshold and above threshold MOS regions of operation. We present circuits implementing the programmable current amplification, log-domain anti-alias filtering, and integrating differential current-to-voltage acquisition, and include experimental results from the 16-channel prototype fabricated through MOSIS in a 1.2 μm CMOS process.

1. INTRODUCTION

Testing of VLSI circuits has become increasingly complex as the maturing of the fabrication technology has enabled the design of chips of increasing size and complexity. Mixed-mode designs, with analog and digital circuitry side by side on the same chip, further complicate the effort that is needed to fully test a VLSI circuit for functional correctness and given performance specifications.

Testing of dedicated VLSI systems for signal processing, such as *e.g.* neural systems for sensory information processing [1] or other high-performance mixed-mode systems for signal processing [2], is only meaningful if the tests conducted approximate conditions of the environment in which they are designed to operate. To that purpose, the VLSI test station has to be capable of characterization of the features of the circuit under test. The most challenging characteristics of modern mixed-signal integrated circuits for functional and performance testing are bandwidth and precision. With modern trends in VLSI technology and systems design pushing performance levels towards lower power dissipation, increased speeds, and increased parallelism, the instrumentation tools needed for testing these systems become a serious problem, and the need to cover a wider dynamic range and a larger number of independent channels creates a demand for alternative, integrated solutions.

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A general purpose test station for multi-channel micro-power mixed-mode analog and digital VLSI systems, illustrated schematically in Figure 1, has been designed to address this need. It allows real-time testing and analysis of complex VLSI systems at a data throughput rate and signal operation levels that would be unattainable with conventional off-the-shelf data acquisition and signal processing tools. Interfaced through a PC I/O board, the test platform is capable of acquiring multiple channels of analog and digital data, storing analog and digital signal waveforms and generating user-defined single-shot and periodic waveform sequences. The custom interface supports a "vector" of 64 digital analog I/O channels, comprising 32 differential voltage I/O channels and 32 current-mode I/O channels, plus 64 digital I/O channels, and provides local storage of 128K vectors sampled at an internal rate of up to 30MHz for digital signals and 200KHz for analog signals per channel. With the use of a floating point representation over four decades of programmable scales, the dynamic range of analog signals under test covers five orders of magnitude, suitable for analysis of micro-power CMOS current-mode circuits operating in part of the subthreshold regime [3] (pA to nA range) to part of the above threshold regime (μA).

The track-and-hold integrated acquisition system presented here processes the incoming analog data of the test station, one chip used for 16 channels of current mode data, and one for 16 channels of voltage mode data converted through external V-to-I amplifiers. The acquisition chip integrates 16 current-mode inputs, 4 voltage references setting the voltage levels of the virtual-ground current inputs in groups of 4, and a single full-range differential voltage output. Each of the 16 channels is independently configured for a gain of attenuation covering four orders of magnitude allowing to acquire bidirectional currents in the range from 100pA to 50 μA, at a reference voltage ranging from 0 to 5V. Programmable cut-off frequencies ranging from 50Hz to 400kHz prevent aliasing of high frequency components and allow to decrease the level of noise generated prior to sampling. The maximum fully sustained sampling rate ranges from DC to 200KHz. The outputs of the system are pipelined and continuously valid, interfacing asynchronously to an external ADC on the PC host acquisition board for data post-processing. Thus, the acquisition chip interfaces between the device under test and a remote PC acquisition system, for fast synchronous measurements over a wide dynamic range.

2. ARCHITECTURE

The block diagram of the single-chip track-and-hold integrated acquisition system is presented in Figure 2. There are 16 data chan-

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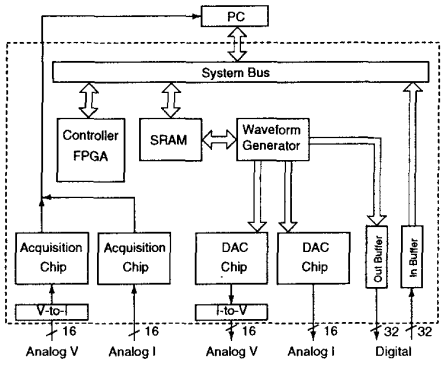

Figure 1: *Block diagram of the general purpose test station for micro-power mixed-signal VLSI system characterization.*

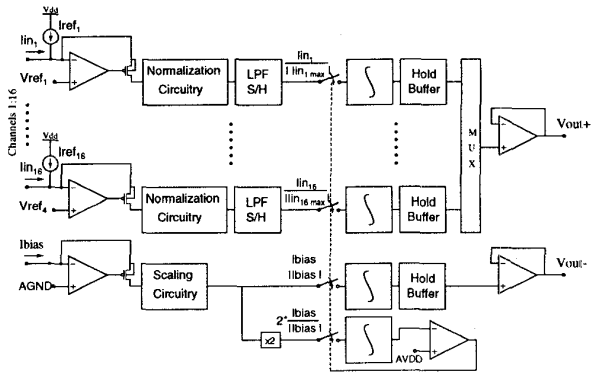

Figure 2: *Block diagram of the integrated track-and-hold acquisition system.*

nels that are controlled by the bias channel (bottom of Figure 2) which also supplies all bias and reference signals. An input signal to each data channel is summed with an appropriately scaled reference current I_{ref} to obtain a unidirectional input signal. This scaled reference current is digitally selected as one of the currents generated in the bias channel. The input to the bias channel is a 50 μA DC current. A transconductance amplifier drives a PMOS load transistor to provide a high input conductance input stage. The acquired input current is then fed into a scaling circuit which is programmed to normalize the signal to a fixed range over the interval [0, 1] μA. This range is chosen appropriately as a trade-off between signal-to-noise ratio and integration time constant further in the channel. The normalized current is fed into an anti-aliasing low-pass filter. Besides serving for anti-aliasing, the cut-off frequency of the filter can be programmed to match the integration time interval when the sample-and-hold is operated in the transparent mode.

The integrator at the end of the channel is used for current-to-voltage acquisition. Integration of 0.5 μA and 1 μA reference currents in the bias channel determine the conversion gain of all 16 channels. This is achieved by controlling the upper-bound voltage and the midpoint voltage of conversion, as set by an externally supplied reference. Once the integrated voltage of the upper-bound reference channel goes above the analog V_{ref} level, a trigger signal (STOP) is generated which completes integration in all channels (including the bias channels themselves). A 16-to-1 multiplexer selects the integrated signal of one of the 16 channels at the output. The midpoint voltage generated by the second reference channel is used as a 'zero-level' reference of the output signal, serving a differential output format for reduced sensitivity to noise and power supply variations. In hold mode, the differential output from the previous integration cycle is buffered and held at the output while the current integration process is taking place.

3. VLSI IMPLEMENTATION AND RESULTS

The integrated track-and-hold acquisition system was designed and fabricated in a 1.2 μm double-poly CMOS process, which includes a p-Base layer to implement vertical NPN bipolars. The chip micrograph is shown in Figure 3. The sections below focus on particular circuit design solutions and their experimentally observed performance.

3.1. Input Transconductance Amplifier

For precision acquisition of small currents, a transconductance amplifier was used, depicted in Figure 4, to provide a high input conductance virtual 'ground' at a user-selectable reference voltage. It constitutes a wide output range single stage differential amplifier with a PMOS differential pair and cascoded BiCMOS current mirrors. The differential pair transistors were laid out in a centroid configuration to lower input voltage offset. Higher accuracy current replication is obtained by using current mirrors base current compensation with MOS voltage followers. The choice of 7V for Vdd level and -2V for Vss level allows the reference voltage to range from 0V to 5V (a typical range of GND and V_{dd} for a mixed-mode VLSI device-under-test).

A PMOS load at the input, in the feedback loop of the amplifier, conveys the current at the supplied reference voltage as shown in Figure 2. The PMOS transistor has the well connected to the source to minimize the back-gate effect, as needed for a 5V range of the input reference voltage. Input impedance in the range from 500Ω to 10KΩ and DC input offsets in the range between 25mV and 5mV (for single ended input), for the maximum and minimum input current scales respectively, were measured. These offset figures are typical for the process used even for a centroid configuration, and higher precision, if so required, can be obtained by using a more advanced (and more expensive) fabrication process.

3.2. Current Normalization

The acquired input current of each of the data channels is normalized to a fixed range suitable for further processing. Normalization circuitry shown in Figure 5 performs this task. The programmable scaling selects between four input ranges of current, 100nA, 1 μA, 10 μA, 100 μA, independently for every data channel. This scaling function provides for a floating point representation, and drastically increased dynamic range. The four BiCMOS current mirrors can be configured to attenuate the input signal with a gain of 0.01, 0.1, 1 or 10 by means of switching of bipolar transistors bases. Vertical NPN and lateral PNP transistors were used in the design. Amplification of currents with gains other than one is performed using NPN vertical transistors, as the gain control by scaling of the emitter area is more precise and reproducible. The output current is a replica of the input current normalized to a range 0–1 μA.

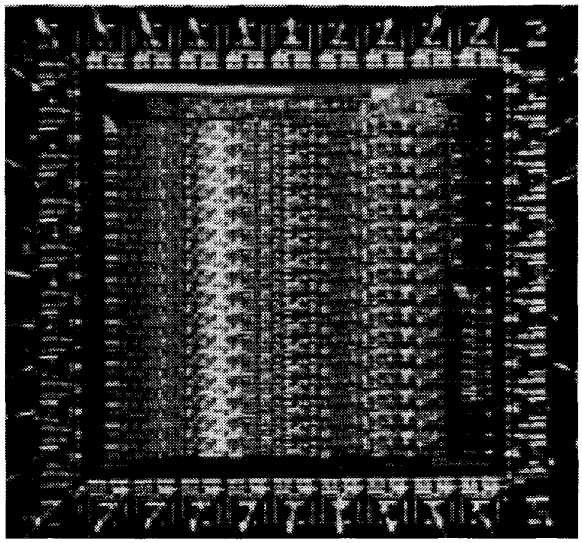

Figure 3: *Chip micrograph of the 16-channel integrated track-and-hold acquisition system. Die size is* 2.25 × 2.25 mm^2 *in 1.2 μm CMOS technology.*

Any nonlinear effects in the normalization, and in subsequent processing stages, can easily be accounted for by a look-up table type calibration in software. The main concern in the design is signal-to-noise performance.

3.3. Low-Pass Filter

To allow aliasing-free sampling of the normalized currents, a low-pass filter with selectable cut-off frequency is incorporated into the channel. A two stage log-domain LPF was designed as shown in Figure 6 [4, 5, 6]. It is composed of two basic first-order log-domain circuits, which use translinear circuits as their building blocks. A basic one-stage log-domain filter exhibits a global linear transfer function while internally consisting of non-linear exponential components. Each stage constitutes a single pole LTI system with unity DC gain if the bias currents are supplied as shown in Figure 6. As it can be observed from the circuit diagram, two single-stage log-domain filters are combined in such a way that the output common-base configuration NPN transistors of the first stage serve as the input transistor pair of the second stage [6]. The resulting two-stage filter has better defined pass-band corners. The cut-off frequency set by the current I_{bias} can be programmed and selectable in the range from 50Hz to 400kHz.

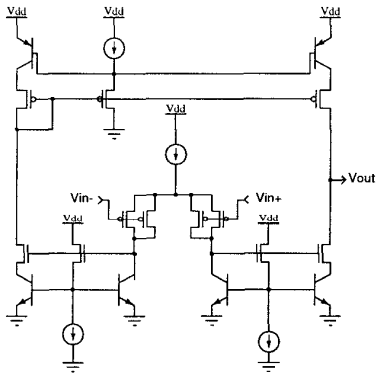

Figure 4: *Input transconductance amplifier with a differential pair in centroid layout configuration.*

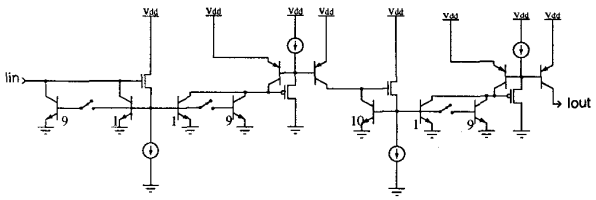

Figure 5: *Data channel current normalization circuitry. Normalization is performed over four orders of magnitude of the input current. The lowest input current scale is 0–100 nA, the highest is 0–100 μA.*

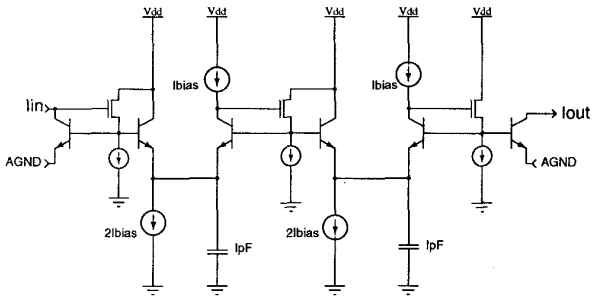

Figure 6: *Anti-aliasing two-stage log-domain LPF.*

The filter prevents aliasing and eliminates high-frequency noise and interference introduced prior to sampling, and additionally allows to bypass the subsequent current-mode sample-and-hold circuit before the integration stage, by selecting a time constant sufficiently larger than the integration time interval. The experimental noise measurements of the output filter current showed an input-referred RMS noise value of 46pA (for a measured attenuation factor of 13) at a 12kHz bandwidth. This indeed allows to resolve input currents as low as 100pA and establishes the dynamic range of the system well in excess of 100dB.

A current-mode sample-and-hold circuit, not shown, follows the anti-alias filter stage. Its operation is synchronized with the subsequent integration stage, and can be disabled (*i.e.,* made transparent) in software. The sample-and-hold can be used for high-speed acquisition at speeds exceeding the integration time interval of the integrator (5 μs), although signal-to-noise considerations (high frequency sampling noise) dictate this feature to be used only in the largest (50 μA) current scale.

3.4. Integration and Hold Buffer Circuitry

Integration circuitry described in this section performs conversion of normalized currents into differential voltage and produces a continuously available output signal. The system level operation

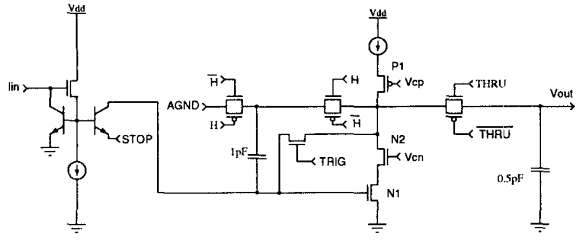

Figure 7: *Integration and track-and-hold circuitry.*

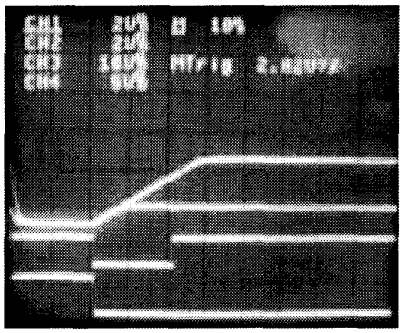

Figure 8: *Integrator control signals and example observed output voltages waveforms. From top to bottom:* V_{out-}, V_{out+}, *STOP, and TRIG.*

principle of the integrators is described in detail in Section 2. As described earlier, an integration circuit is employed once in every data channel, and separately in two reference channels, one to control the conversion gain factor, and the other to provide a zero-level reference for the converted output voltage signal.

The circuit diagram of one integrator channel is given in Figure 7. Transistors N1, N2 and P1 and a PMOS current source realize an inverting transconductance amplifier. The mirrored input current is integrated on a 1pF capacitor across the amplifier. The digital signal TRIG is a narrow pulse resetting the integrating capacitor on the rising edge, and also resetting the STOP signal (described in Section 2) on the falling edge. The digital signal $\overline{\text{H}}$ is a delayed version of TRIG. Once TRIG switches high, the integrating capacitor is reset. When TRIG turns low, the input current is activated, and is integrated on the capacitor. Duration of the integration process is determined by the width of the STOP pulse, which itself is determined by the time the integration takes to attain the nominal value, by the procedure explained above. This corresponds to a 5 μS integration time, or 200KHz maximum sustained sampling frequency. Higher conversion rates are achievable by activating the sample-and-hold cell included in the preceding stage. Figure 8 illustrates example waveforms of the signals described above for zero integrator input current and normalization range $[0, 4]$ μA.

In order to produce continuously available output voltage, during the previous integration cycle, the output voltage is sampled on a 0.5pF capacitor and held while a new current is integrated in pipelined fashion. The control of this feature is carried out in software by the digital signal THRU.

Table 1: Measured Chip Characteristics

Channels	16			
Max Sampling Rate	200KHz			
Input Current Range	-50nA-+50nA	-500nA-+500nA	-5uA-+5uA	-50uA-50uA
Input-Referred RMS Current Noise	46pA	1nA	8nA	25nA
Input Impedance	10 KOhm	4 KOhm	1 KOhm	100 Ohm
DC Offset	+/-5mV	+/-7mV	+/-10mV	+/-25mV
Power Dissipation	12.5mW			
Analog Volt. Range	0-5V			
LPF Cut-off Freq.	50 Hz - 400KHz			
Power Suppl. Volt.	-2V; +7V			
Technology	1.2um, BiCMOS (vertical NPN), double poly			
Die Size	2.25 mm x 2.25 mm			

3.5. Summary of Experimental Results

The measured characteristics of the integrated track-and-hold system are summarized in Table 1.

4. CONCLUSIONS

A 16-channel integrated acquisition system has been presented as part of a general purpose test platform. It has been tested to operate with a dynamic range of 100dB and allows to resolve analog currents as low as 100pA. The system features programmable current gain control, configurable anti-aliasing circuitry, triggered current integration and provides differential output ready for asynchronous external A/D conversion over a compressed dynamic range. With a sampling rate ranging from DC to 200KHz and dynamic range covering five orders of magnitude, the integrated acquisition system is intended for analysis of micro-power CMOS current-mode circuits and parallel systems operating both in weak and strong inversion. Larger bandwidths are available through internal S/H circuitry if required.

5. REFERENCES

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