27.3 All-Wireless 64-Channel 0.013mm²/ch Closed-Loop Neurostimulator with Rail-to-Rail DC Offset Removal

Hossein Kassiri[1,*], Reza Pazhouhandeh[1], Nima Soltani[1], M. Tariqus Salam[1], Peter Carlen[1,2], Jose Luiz P. Velazquez[1,3], Roman Genov[1]

[1]University of Toronto, Toronto, ON, Canada,
[2]Toronto Western Hospital, Toronto, ON, Canada
[3]Toronto Hospital for Sick Children, Toronto, ON, Canada
*Now with York University, Toronto, ON, Canada

Accurate capture and efficient control of neurological disorders such as epileptic seizures that often originate in multiple regions of the brain, requires neural interface microsystems with an ever-increasing need for higher channel counts. Addressing this demand within the limited energy and area of brain-implantable medical devices necessitates a search for new circuit architectures. In the conventional designs [1-5], the channel area is dominated by the bulky coupling capacitors and/or capacitor banks of the in-channel ADC, both unavoidable due to the channel architecture, and unscalable with CMOS technology. Additionally, channel power consumption, typically dominated by the LNA, cannot be reduced lower than a certain limit without sacrificing gain and/or noise performance. In this paper, we present a 64-channel wireless closed-loop neurostimulator with a compact and energy-efficient channel architecture that performs both amplification and digitization in a single $\Delta\Sigma$-based neural ADC, while removing rail-to-rail input DC offset using a digital feedback loop. The channel area and power consumption depend only on the active components and switching frequency, respectively, making the design both technology- and frequency-scalable.

Figure 27.3.1 (top) shows the block diagram of the $\Delta^2\Sigma$ (Δ+$\Delta\Sigma$) neural ADC. Because of the added Δ stage, the output bit-stream (Y) of $\Delta\Sigma$ modulator is equivalent to the derivative of the input signal. Consequently, after feeding Y to the feedback integrator, a reconstructed version of the previous sample of the input signal ($\overline{V}_{IN}$[n-1]) is obtained. As a result, the output of the first Δ stage (dV_{IN}) is the difference between the two consecutive samples of the input signal, which means any DC offset value (0 to VDD) is removed. Figure 27.3.1 (bottom) depicts how the architecture is made differential for an array of 64 channels. As shown, by dedicating a single copy of the described architecture as the reference channel, the derivative of the reference signal is taken (dV_{REF}) and subtracted from the derivative of input signal of each recording channel. Moreover, given the high oversampling ratio (OSR) and due to operating on signal derivatives only, this configuration has virtually no upper-limit for the input signal amplitude in the LFP range (<500Hz).

Figure 27.3.2 shows the recording channel circuit schematic. Positive-gain and negative-gain parasitic-insensitive integration are used to implement the Σ stage of the $\Delta\Sigma$ modulator for the input and reference signals, respectively. In each clock cycle, one integrator pulls and the other pushes charge to the shared accumulating capacitor (C2), resulting in differential integration. Correlated double sampling is implemented using C_{CDS} and one extra switch to remove the flicker noise and offset of the two-stage 10T amplifier A. The compact IMDAC (I-mode multiplying DAC) in the feedback integrator is comprised of two segments of 4b binary-weighted programmable push/pull current sources. The segments are biased by two currents, different by a factor of 16 for a total of 8b of resolution. The output bit-stream, which is a derivative of the input signal, is fed to a resettable (decimating) and a non-resettable (integrating + decimating) up/down counters, to obtain digital equivalents of the input signal ($M\times D_{OUT}$) and its derivative ($M\times\Delta D_{OUT}$), respectively. The 90° phase difference between the two outputs that comes at the cost of only one additional counter, makes them quadrature signals ideal for neural signal phase calculation in the digital signal processing backend. In-channel low-overhead digital-analog multiplication (×M) eliminates expensive signal weighting for tone-selecting FIR filters in the digital backend.

Figure 27.3.3 depicts the system VLSI architecture of the fabricated responsive neurostimulator SoC. It includes 64 closed-loop neuro-stimulators, a low-power DSP with a compact mixed-signal FIR filter, two UWB transmitters, and an inductive power and command receiver. The on-chip DSP calculates the phase synchrony among channels to detect an upcoming epileptic seizure. Five out of six animal subjects have become seizure-free in a recent study using phase synchrony [6], as compared to the 1-out-of-10 seizure-free outcome using conventional neurostimulators. Once a detection is made, an arbitrary-waveform current-mode biphasic stimulation is applied to a subset of the electrodes with a spatio-temporal profile specifically chosen for a given subject. During stimulation, the previously-introduced in-channel programmable IMDAC is reused for current-mode biphasic pulse generation. Thus, arbitrary-waveform stimulation enabled by analog-digital multiplication is performed at almost no extra area cost, and 64×64-tap power-hungry and area-inefficient digital multipliers are once again avoided. The recorded intracranial EEG/ECoG data and status signals are also transmitted out transcutaneously using either a low-power delay-based short-range (d<10cm) or a VCO-based long-range (d<2m) UWB transmitters. Energy is received by a single coil through a multi-coil cellular inductive link at 1.5MHz frequency. The power receiver outputs 30mW maximum power for the 15cm transmission distance with the overall power transfer efficiency of 40%. An ASK-demodulating command receiver reuses the same inductive link to recover transmitted commands and the clock.

Figure 27.3.4 depicts experimentally measured data for the neurostimulation channel. Figure 27.3.4 (top) shows the experimentally measured FFT of the ADC output with a 130Hz input sampled at 1MHz (with the input signal bandwidth of 500Hz). The measured input impedance remains above 100MΩ (sufficient for implantable intracranial recording), even with the maximum sampling frequency of 1MHz. The channel yields SNDR and ENOB of 72.2dB and 11.7b, respectively. Figure 27.3.4(middle) shows the input-referred noise spectrum with and without correlated double-sampling. Figure 27.3.4(bottom) shows three examples of waveforms generated by the arbitrary-waveform current-mode stimulator with a 1kΩ load.

Figure 27.3.5 (left, top and middle) shows the quadrature outputs of the channel for a multi-tone input, the phase error as compared to the ideal 90° phase difference, and the calculated phase using the on-chip processor. Figure 27.3.5 (top, right) shows how the power consumption of all the blocks scales linearly with the input signal bandwidth. As shown, the recording channel dissipates a total of 630nW for the ECoG band, the band used for seizure prediction. Figure 27.3.5 (middle, right) shows how the active-component-dominated channel area scales with the technology compared to a conventional AC-coupled channel [1]. Figure 27.3.5 (bottom) shows the power spectral density of the two UWB transmitters.

The 0.13µm CMOS SoC was validated in both early detection (experiment 1) and control (experiment 2) of seizures in temporal lobe epilepsy (rat model). Figure 27.3.6 (top, left) shows an example of *in vivo* online on-chip real-time seizure detection without stimulation. In the second experiment, the SoC was configured to automatically trigger the closed-loop electrical stimulation for the purpose of suppressing upcoming seizures. Figure 27.3.6 (top, right) illustrates the SoC-triggered stimulation upon a seizure onset detection. The SoC is compared with the state of the art both in terms of the channel performance (Fig. 27.3.6 (bottom)) and the system performance (Fig. 27.3.7(bottom)). The chip micrograph and the channel floorplan are shown in Fig. 27.3.7 (top).

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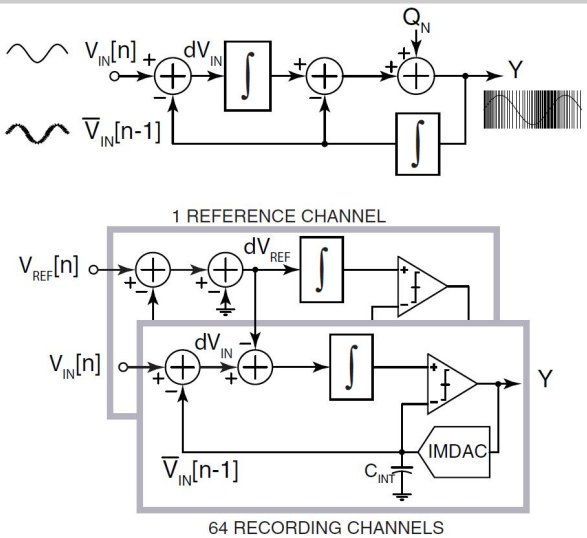


Figure 27.3.1: Block diagram of the ΔΣ-based neural recording channel in both single-ended (top) and differential (bottom) configurations.

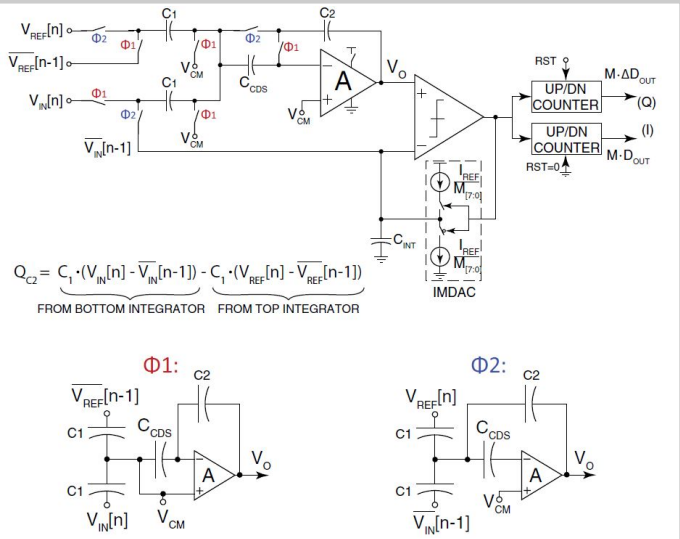


Figure 27.3.2: Circuit schematic of the recording channel (top); the input integrator during the two phases of a single clock cycle (bottom).

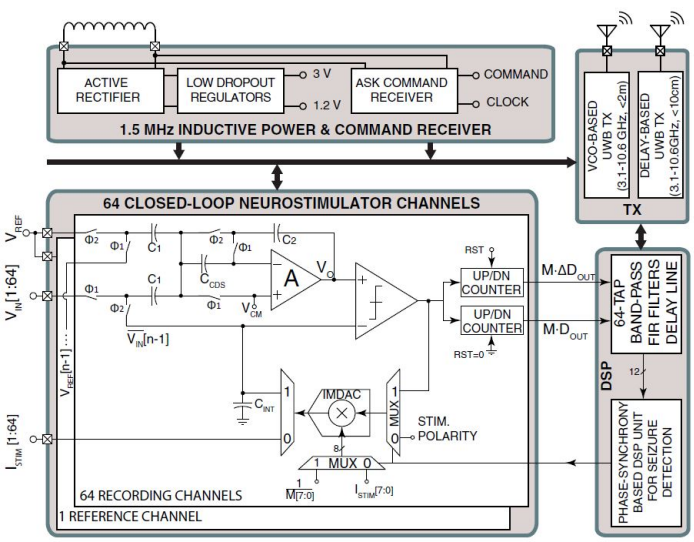


Figure 27.3.3: Block diagram of the fabricated neurostimulator SoC.

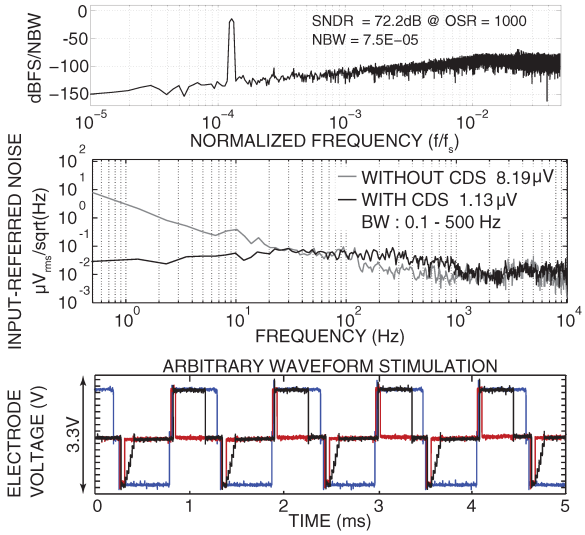


Figure 27.3.4: Experimentally measured performance characteristics of the neurostimulator channel.

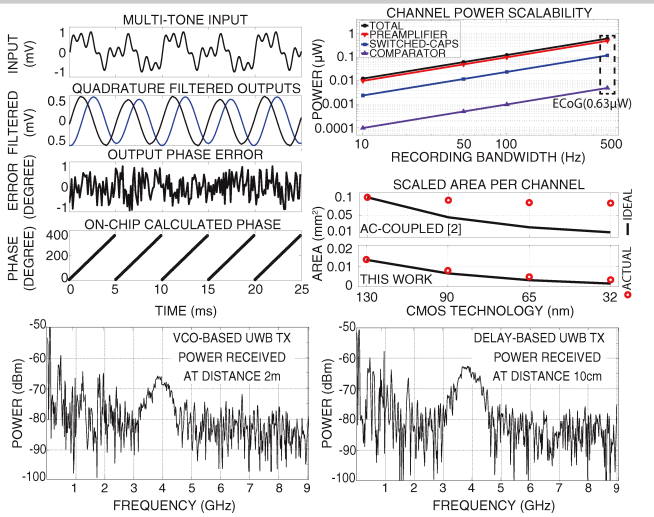
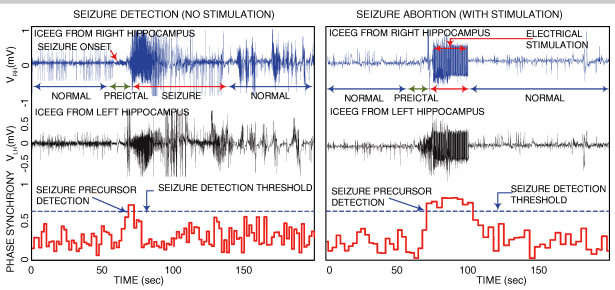


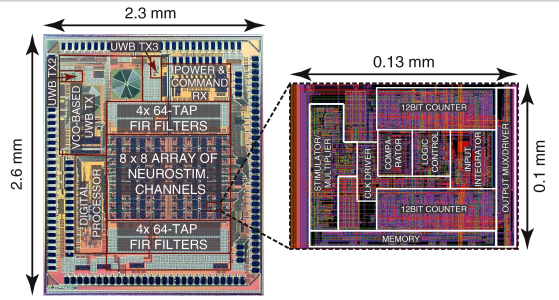
Figure 27.3.5: Experimentally measured performance: the on-chip phase calculation, power scalability with bandwidth, area scalability with technology, and wireless transmitters output spectra.



	JSSC'13 [1]	JSSC'14 [2]	JSSC'15 [3]	ISSCC'15 [4]	JSSC'16 [5]	THIS WORK
TECHNOLOGY (μm)	0.13	0.18	0.065	0.065	0.13	0.13
BANDWIDTH (Hz)	0.1 - 7k	0.1 - 7k	1 - 500	1 - 8.2k	1 - 5k	0.01 - 500
POWER/CH (μW)	10	53.7	2.3	2.8	9.1	0.63
NOISE BW (Hz)	10 - 5k	0.5 - 7k	1 - 500	1 - 8.2	1 - 1k	0.1 - 500
IR NOISE (μV_{rms})	4.7	5.23	1.29	4.13	4.2	1.13
NEF	4.4	1.77	4.77	2.93	6.9	2.86*
MAX OFFSET	AC-Coupled	AC-Coupled	± 50mV	AC-Coupled	± 50mV	rail-to-rail
AREA/CH (mm^2)	0.09	-	0.025	0.042	0.018	0.013
STIM. CURRENT (mA)	0.01-1.2	0.03	N/A	N/A	0.01-1	0.01-1.35

*FOR AMPLIFIER+ADC.

Figure 27.3.6: *In vivo* seizure detection and closed-loop stimulation results for a rat epilepsy model (top), neurostimulator channel performance comparison (bottom).



	JSSC'13 [1]	JSSC'14 [2]	JSSC'15 [3]	ISSCC'15 [4]	JSSC'16 [5]	THIS WORK
Tech. (μm)	0.13	0.18	0.065	0.065	0.13	0.13
Area (mm2)	12	13.47	5.76	-	16	5.98
Supply (V)	1.2 / 3.3	1.8	0.5	0.5	1.2 / 2.5	1.2 / 3.3
Power Diss. (mW)	1.4	2.8	0.225	-	2.17	1.07*
# of Rec. Chan.	64	8	64	16	64	64
Signal Processing	Yes	Yes	No	No	Yes	Yes
Closed-loop Stim.	Yes	Yes	No	No	Yes	Yes
Wireless Power	No	Yes	Yes	No	Yes	Yes
Range (cm)	-	-	1.6	-	15	15
Wireless Comm.	Yes	Yes	Yes	No	Yes	Yes
Range (m)	0.1	-	-	-	10	2

*Without the VCO-based UWB transmitter.

Figure 27.3.7: Chip micrograph and channel floorplan (top), and a system-level comparison table (bottom).

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