A CMOS-Microfluidic Chemiluminescence Contact Imaging Microsystem

Ritu Raj Singh, *Student Member, IEEE*, Lian Leng, Axel Guenther, and Roman Genov, *Senior Member, IEEE*

***Abstract*—A hybrid CMOS-microfluidic microsystem for chemiluminescence and electrochemiluminescence-based biochemical sensing is presented. The microsystem integrates a two-layer soft polymer microfluidic network and a CMOS imager fabricated in a standard 0.35-μm technology. The CMOS imager consists of a 64×128-pixel array interdigitated with a 32×64 electrolessly plated nickel–gold microelectrode array. A two-transistor reset path technique attenuates the subthreshold leakage current of the reset transistor which constitutes a significant portion of the dark current. An active reset technique, in-pixel flicker noise cancellation, and pixel binning contribute to noise reduction. The imager achieves a low dark current of 3.6 nA/cm^2 for photodiode reset voltages as high as 2.3 V, noise of 110 μVrms with maximum time of photon integration of 90 s, and a dynamic range of 67.8 dB. The CMOS-microfluidic microsystem is validated in on-chip chemiluminescence and electrochemiluminescence detection of luminol.**

***Index Terms*—Active-reset technique, chemiluminescence (CL), CMOS image sensor, contact imaging, dark current, electrochemiluminescence (ECL), electroless nickel-gold plating, in-pixel flicker noise cancellation, microfluidics, subthreshold leakage, two-transistor reset path.**

I. Introduction

THERE is a fast growing need for low-cost, small-form-factor biochemical sensory systems for applications such as on-site medical, environmental, and biothreat monitoring [1], [2]. Optical luminescence sensing techniques are widely popular in these applications [3][4]. In such techniques, the number of photons emitted is proportional to the amount of an analyte, which are then quantified to estimate the analyte concentration.

A simplified cross section of a conventional luminescence sensing system for optical imaging of biochemicals is shown in Fig. 1(a). It involves bulky and expensive magnifying optics and a photodetector, usually a photomultiplier tube (PMT) [6], [7]. A PMT is a single photodetector device which is high-cost, requires high voltage for operation, lacks portability, and has low sensory throughput. These disadvantages make conventional imaging systems unsuitable for on-site and point-of-care applications.

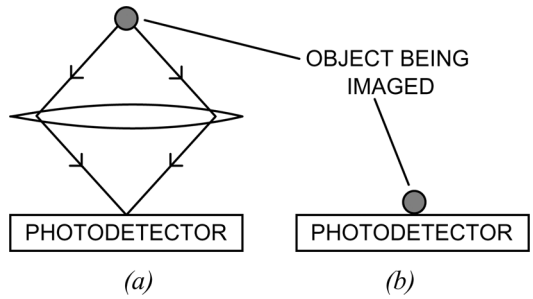

Fig. 1. Illustration of the principles of (a) conventional imaging and (b) contact imaging.

In contrast, contact imaging is a compact and low-cost luminescence sensing technique [8]. The object to be imaged is placed in close proximity to the photodetector array, usually just over the surface of the photodetector [6], [7] as depicted in Fig. 1(b). Contact imaging does not require intermediary optics, resulting in significant area and cost savings. Contact imaging also improves the light collection efficiency with orders-of-magnitude increase in sensitivity [9]. A higher sensitivity leads to lower consumption of costly specimens. These advantages make contact imaging employing luminescence detection attractive for on-site deployable, low-cost biosensors.

The two most common luminescence-sensing techniques are fluorescence and chemiluminescence sensing. Fluorescence sensing involves a significant background light component which is narrowband and can be removed utilizing an intermediary optical filter [5], [10], [11]. High-performance optical filters are required to attenuate background light and achieve high dynamic range. In chemiluminescence sensing, light is produced as a result of a chemical reaction and is proportional to the reacting analyte concentration. Unlike fluorescence sensing, chemiluminescence (CL) sensing involves negligible background light and, hence, there is no intermediary optical filter requirement [6], [7], [12]. With a simple contact imaging system design, the light emission can occur in immediate proximity to the sensing photodetector, yielding a high optical coupling efficiency.

Electrogenerated CL or electrochemiluminescence (ECL) sensing is an enhanced form of CL sensing. Luminescence occurs as a result of electrochemical excitation [7], [13], [14]. Electrodes are introduced into the chemical sample so that electrical excitation can be introduced exactly where the electrodes are placed. ECL sensing offers additional benefits of improved control over the chemical reaction rate and higher selectivity.

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R. R. Singh is with the Department of Electrical and Computer Engineering, University of Texas at Austin, Austin, TX 78705 USA.

R. Genov is with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4 Canada (e-mail: roman@eecg.utoronto.ca).

L. Leng and A. Guenther are with the Department of Mechanical and Industrial Engineering, University of Toronto, Toronto, ON M5S 3G8 Canada (e-mail: axel.guenther@utoronto.ca).

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II. Design Considerations

For high-throughput CL and ECL sensing, a parallel interdigitated microelectrode-photosensor array is desired. Charge-coupled devices (CCDs) are not ideally suited for biosensing applications due to the high cost. CMOS photosensory devices are an attractive choice. They are intrinsically parallel, have a low fabrication cost, and enable versatile on-chip integration along with peripheral circuits for signal conditioning and analyte detection. These advantages make the CMOS technology a good fit for low-cost portable biochemical sensor applications by leveraging their flexibility to build highly parallel integrated photodiode-microelectrode arrays.

Placing a luminous object such as a biochemical-sensitive light-emitting analyte onto an imaging array surface requires a compatible channel network for fluid delivery and removal. A parallel-structured, high-spatial-resolution fluidic channel network enables high-throughput biochemical analysis. Low-cost versatile soft lithography-based microfluidic channels are attractive for such applications.

Recently, several research groups reported integration of a microfluidic network with a CMOS photodetector. Costly non-CMOS custom silicon technologies integrated with expensive and elaborate microfluidic technology were reported in [15]–[17]. CMOS-microfluidics integration has been reported for applications in cell culture [18], flow-based cytometry [19], [20], capacitance-based fluid detection [21], and high-resolution imaging [22]. The flow cytometer in [19] integrates microfluidics over the CMOS image sensor with no access to the in-channel fluid. The microsystems in [18], [21], and [20] utilized low-spatial-resolution microfluidic channels. A high-resolution CMOS-microfluidic system was implemented in [22] which required high-computational processing resources for image reconstruction [22]. Noncontact sensing results in lower sensitivity and higher pixel crosstalk while low-spatial-resolution microfluidic channels do not fully utilize the intrinsic parallelism of a CMOS-microfluidic microsystem. These drawbacks lead to a lower throughput when performing multi-analyte chemical analysis.

Utilizing standard CMOS technology for microelectrode fabrication provides aluminum/1%-silicon electrode surfaces. Aluminum is prone to quick corrosion when exposed to fluidic analytes, necessitating a postprocessing process to deposit a noble metal on top of the aluminum electrodes. Gold stud bumping was employed to create gold electrode surfaces in [23] and [24]. However, gold stud bumping cannot be employed for small pixel sizes of the order of a few micrometers in dimension. Alternatively, an expensive cleanroom process to sputter gold can be employed [25], [26]. Electroless nickel-gold plating provides another good alternative to perform low-cost, non-cleanroom, low-operating-temperature, well-controlled, and uniform thin-layer gold deposition ideally suited for small-sized electrodes [27].

To enable the use of small analyte volumes and improve the detection limit of the resulting microfluidic contact imaging microsystem, the CMOS imager performance should be optimized for low-level light sensitivity. Optimization for slowly varying low-level light signals necessitates the reduction in the pixel dark current. Reducing the dark current enables a proportional increase in the photointegration time, thus improving imager sensitivity. Moreover, the pixel noise should be minimized.

Low dark currents have been achieved in CMOS technology by implementing large photodiodes [28]–[30]. High fill factor was achieved at the cost of spatial resolution. Reduction of the dark current of small standard CMOS photodiodes required for high-spatial-resolution image-microfluidics microsystem is challenging. The photodiode dark current does not decrease linearly with reduction in the photodiode area. Small photodiodes contain a significant perimeter component of the diode junction-leakage current [31]. Among the low dark-current techniques, an ultralow dark-current technique for small pixel sizes was proposed in [32]. It reduces the perimeter component of the dark current by implementing a big photodiode separated by polysilicon gates. Inadequate isolation of adjacent pixels resulted in degraded performance due to pixel blooming. Lower photodiode reset voltage techniques to reduce the dark current have also been utilized [30], [33]. Reset voltages approximately an order of magnitude lower than the supply voltage were utilized to significantly reduce the leakage current at the cost of reduced dynamic range. Special nonstandard CMOS technology was utilized in [30] to tailor pixel dark currents and achieve a long photointegration time of three minutes.

Another significant component of the pixel dark current is the subthreshold leakage current from the pixel reset transistor adjoining the photodiode [28]. A three-transistor T-switch was utilized to reduce the subthreshold leakage current [28]. The T-switch requires an operational amplifier, thus resulting in a small pixel fill factor. An average voltage concept to quantify low-level light is employed in [34]. The method has limited linearity and does not fully utilize the relaxed time constraints available in chemical analyte sensing.

To attenuate *kTC* noise, pixel-array fixed pattern noise, and flicker noise, correlated double sampling (CDS) has traditionally been employed. An in-pixel memory element was utilized to perform CDS in [35] and [36]. Column-level CDS circuit was employed in [37]. Digital frame subtraction of the reset frame from the signal frame is also employed at the cost of doubling the bandwidth required [30]. An in-pixel memory element occupies valuable area while column-level CDS circuits and frame subtraction increase the signal processing requirements. A disadvantage of utilizing CDS-based low-frequency noise cancellation is the doubling of the uncorrelated thermal noise power which may exacerbate the overall pixel noise [38]. Unlike conventional CDS, utilizing the threshold voltage of a unity-gain feedback amplifier as the photodiode reset voltage along with an active reset facilitates flicker noise and offset cancellation without significantly degrading the thermal noise component [38], [39].

In summary, developing a low-level light, slow-temporal variation, multi-analyte detection microsystem involves challenges in the image sensor design, microfluidics, and the integration of the CMOS-microfluidic microsystem. The sensor should provide a high-density, parallel photodiode–microelectrode interface. The image sensor pixel should be ultralow-level light sensitive, while occupying a small area for high resolution. The pixel fill factor should be maximized for high optical

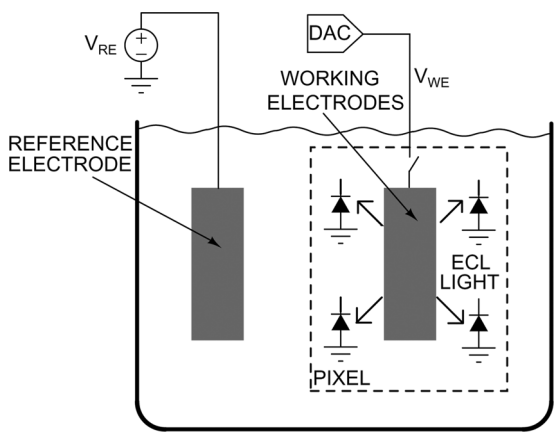


Fig. 2. On-CMOS ECL sensing method.

coupling efficiency. The pixel architecture should minimize the dark current and reduce its nonlinearity, facilitating larger well capacity, longer integration time, and thus improved photon-per-second sensitivity. The pixel reset and flicker noise performance should be optimized by employing area-efficient noise-reduction techniques. Low-cost, compatible post-processing steps should be employed to accommodate ECL sensing.

We present a CMOS-microfluidic microsystem for direct-contact, high-spatial-resolution CL/ECL-based optical sensing of chemical analytes. Preliminary results have been reported in [40]. The CMOS chip integrates a 64×128 photodiode array interdigitated with a 32×64 microelectrode array. Leveraging the benefits of ECL with highly parallel integrated photodiode-microelectrode arrays offers significant advantages by facilitating spatial and temporal control over the sensing reaction along with the selectivity to detect multiple analytes in a solution.

Fig. 2 illustrates the implemented ECL sensing mechanism suitable for highly parallel integrated photodiode–microelectrode arrays. It involves a reference electrode (RE) and many working microelectrodes (WEs; one is shown). The microelectrodes can be chemically coated to facilitate analyte selectivity and the potential at the microelectrodes controlled to electrically modulate the chemical reaction rate occurring at the microelectrode surface. Light emitted by the chemical reaction is captured by the photodiodes located in close proximity to each working microelectrode.

The image sensor achieves high pixel fill factor for the small pixel size of 19 μm $\times$ 19 μm by employing a transistor-sharing architecture [41]. A fairly constant ultralow dark current of 3.6 fA is achieved at a high diode junction voltage of 2.3 V by utilizing a two-transistor reset path to block the significant subthreshold leakage current of the reset transistor. The peripheral leakage current of the photodiode is reduced by employing a polysilicon bias ring structure [42]. An integration time of as long as 90 s can thus be achieved, enhancing input photocurrent sensitivity. Noise reduction to 110 μVrms from 422 μVrms is attained by implementing the in-pixel active reset technique [43], [44] and in-pixel flicker noise and offset cancellation without introducing additional transistors in the pixel [38].

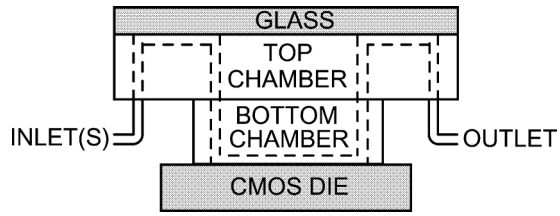


Fig. 3. Side-view visualization of the CMOS-microfluidic contact imaging microsystem.

Supply noise and switching signal coupling are reduced by utilizing differential signaling [30]. On-chip 2×2 pixel binning can be employed to yield high image signal-to-noise ratios (SNRs) at the cost of image resolution [45].

The remainder of this paper is organized as follows. Section III provides a brief overview of the CMOS-microfluidic microsystem. Sections IV and V describe the design and implementation of the microsystem components, the CMOS imager, and the microfluidic network, respectively. Section VI discusses the experimental results validating the imager-microfluidics microsystem.

III. Microsystem Integration

Fig. 3 depicts the cross section of the proposed assembly of the microfluidic channel network over a CMOS chip to perform contact imaging. A two-layer microfluidic structure is utilized. The top-layer microfluidic network contains the inlet and outlet interfaces for the system. The liquid analytes enter through the inlets of the top layer. The bottom layer fluidic network faces the CMOS chip. It contains a fine spatial resolution microfluidic network. Routing the microfluidic channels directly over the CMOS chip results in an increased sensitivity and reduced crosstalk [9], [46]. The top-layer and bottom-layer microfluidic channels are bonded to face away from each other and form channel networks with the glass layer and the CMOS die, respectively. The entire microfluidic structure is glued to the glass substrate and compression sealed over the CMOS chip. The individual components of the microsystem are discussed next.

IV. CMOS Imager

Fig. 4 shows the micrograph of the CMOS contact imager fabricated in a standard 0.35-μm CMOS technology. It consists of a 64×128 pixel array interdigitated with a 32×64 array of microelectrodes. A bank of 128 column-parallel correlated double sampling amplifiers along with signal conditioning exist at the bottom (not discussed in this paper). Fig. 5(a) shows a close-up chip micrograph showing a pixel group consisting of four pixels sharing a single aluminum microelectrode. Each pixel has a dimension of 19 μm $\times$ 19 μm. The electrode size is 7 μm $\times$ 30 μm. A post-processing step to deposit a noble metal is required to render the electrode surface chemically inert. Low-cost, low-operating-temperature electroless nickel–gold deposition is employed to deposit a thin 0.5-μm gold layer on top of the electrodes. An intermediate 2-μm-thick nickel layer is employed for adhesion of gold to aluminum. Fig. 5(b) shows the SEM photograph, and Fig. 5(c) depicts the cross section of the electrolessly nickel–gold-plated electrodes. As depicted in

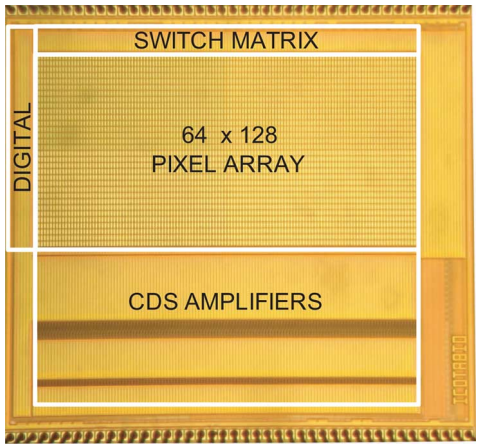


Fig. 4. Micrograph of the 2.9 mm × 2.7 mm contact imager prototype fabricated in a standard 0.35-μm CMOS technology.

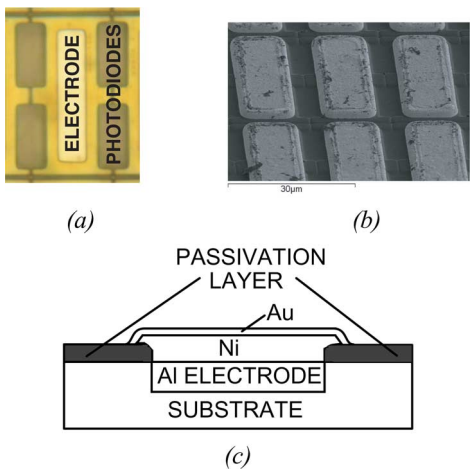


Fig. 5. (a) Closeup chip micrograph showing the photodiode/electrode arrangement. (b) SEM micrograph of the electroless nickel–gold-plated electrodes. (c) Cross section of the electroless nickel–gold-plated electrode.

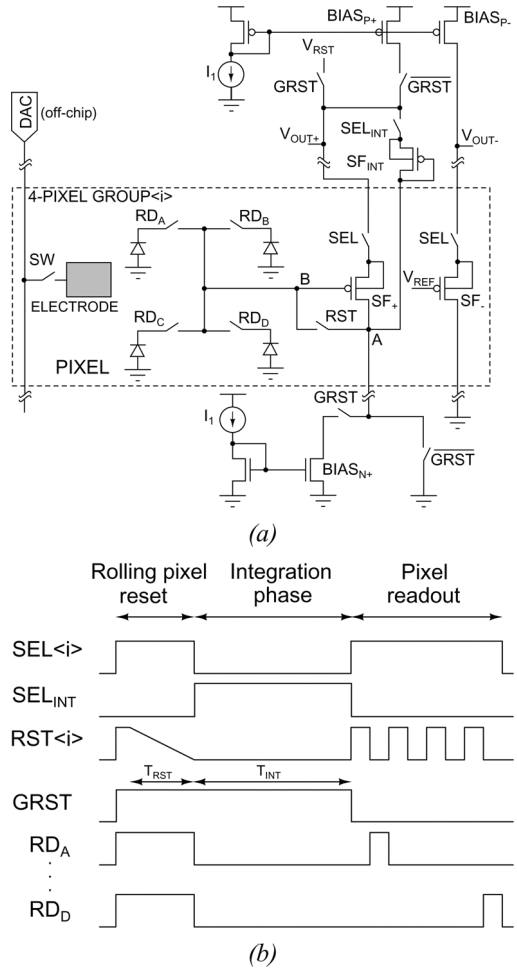


Fig. 6. (a) Pixel circuit and its column biasing circuit. (b) Pixel timing diagram.

Fig. 2, these electrodes function as working electrodes and can be individually selected utilizing a switch array matrix.

The choice of 0.35-μm technology node achieves a reasonable tradeoff between the degrading effect of dark current and quantum efficiency versus a high fill factor [47], [48]. The photo-charge collection efficiency in a CMOS photodetector is dependent upon the number of photons collected in the depletion region and the bulk substrate. The junction depth, the mobility, and the minority carrier lifetime of charged carriers decrease with higher doping concentrations which are a characteristic of smaller gate-length technologies. The quantum efficiency thus degrades with smaller gate technologies [47], [48]. The off/leakage current of the reset transistor in a conventional photopixel architecture is a significant contributor to the pixel dark current [28]. The off-leakage current degrades in smaller gate-length technologies.

Fig. 6(a) and (b) depicts the pixel circuit and the timing diagram of the control signals, respectively. Photodiodes were employed as photodetectors due to better linearity compared with bipolar phototransistors [49]. Avalanche photodiodes were not considered due to the necessity of high voltages for operation [50], [51]. Among photodiodes, n^+-p-substrate photodiode was chosen due to its compact layout area and high capacitance density. A compact layout yields a high fill factor while the higher capacitance reduces charge injection errors and increases the maximum possible SNR in the shot-noise-limited scenario. The SNR achieved when the input photocurrent has just saturated the photodiode is shot-noise-limited [34]. Due to the requirement of a small pixel size, the photodiode intrinsic capacitance has been utilized to store the photosignal charge rather than employing a large in-pixel amplifier-based architecture [28], [52].

As shown in Fig. 6(a), each pixel contains four photodiodes that share the differential common source followers $\mathrm{SF}_{+/-}$, select transistors *SEL* and the reset transistor *RST*. The pixel output is read out using a column circuitry consisting of the biasing transistors $\mathrm{BIAS}_{P+/-}$ and the switches controlled by the global reset signal *GRST*. Access transistors $RD_{A\text{-}D}$ are used to select and read one photodiode at a time [41]. Sharing the transistors across several photodiodes results in a smaller effective unit pixel size and an increased fill factor. It also decreases the column capacitance, significantly improving the column readout speed. The transistor sharing architecture can also be utilized to perform on-chip pixel binning [53] to achieve higher imager SNRs, at the cost of reduced spatial resolution [45]. The SNR improves due to the higher integrating photocapacitance.

TABLE I
PIXEL CIRCUIT TRANSISTOR SIZING

Transistor	W/L (μm/μm)
RD_A-RD_D	0.4/0.35
RST	0.4/0.35
$SEL/SEL_{INT}(PMOS)$	2.05/0.35
$SEL/SEL_{INT}(NMOS)$	0.7/0.35
SF_+ / SF_- / SF_{INT}	3.0/1.5
$BIAS_{P+}$ / $BIAS_{P-}$	2.0/3.7
$BIAS_{N+}$	1.7/3.4
$GRST(NMOS)$	0.7/0.35
$GRST(PMOS)$	2.1/0.35

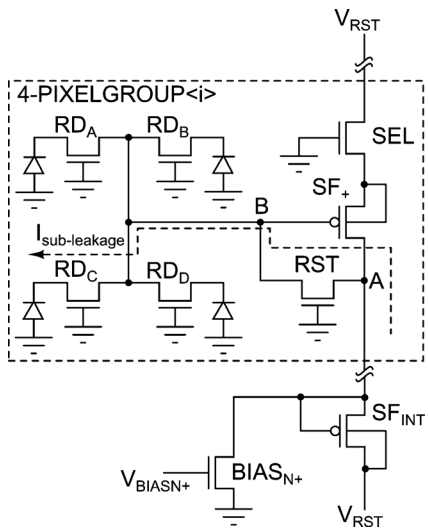


Fig. 7. Pixel circuit diagram during the integration phase.

The access transistors $RD_{A\text{-}D}$ can all be switched on to form a larger photodiode. These transistors are minimum-size to reduce charge injection and clock feedthrough errors. Their noise contribution in the pixel readout noise is minimal. The transistor sizes for the source follower $\mathrm{SF}_{+/-}$, the bias circuitry $\mathrm{BIAS}_{(\mathrm{P/N})+}$, and the global reset switches *GRST* were optimized for pixel readout noise minimization. To reduce the intrinsic flicker noise of the $\mathrm{SF}_{+/-}$ transistors and to subdue the effect of excessively noisy pixels at minimum gate lengths [54], the transistor area and length were chosen bigger than the minimum size. All transistor sizes are listed in Table I.

Minimization of the photodiode dark current is crucial for improved low-level light sensitivity. Subthreshold leakage current from the adjoining reset transistor source/drain junction can contribute significantly to the dark current [28]. Fig. 7 shows a simplified circuit diagram of the pixel during the integration phase. The circuit involves transistor switches *RST* and *RD*, forming a two-transistor reset path. During the integration time, these two transistors are turned off. Charge developed due to the incident photons causes the voltage across the photodiode to drop. This results in a corresponding increase in the voltage drop between the reset voltage and the photodiode. In the case of a conventional active pixel, the voltage drop is present across the drain–source terminal of a single reset transistor in an off-state. In contrast, the proposed architecture distributes the voltage drop across the drain–source terminals of the two reset transistors. Distribution of the voltage drop results in a negative gate-source voltage across the *RST* transistor and, thus, a decrease in the subthreshold leakage component of the dark current [33], [55]. The amount of dark current reduction depends on the voltage division across the two transistors. A rectangular photodiode layout was used to minimize the dark current degradation due to edge effects [31]. To further reduce the peripheral dark current component, a polysilicon ring was placed at the edge of each photodiode to separate the defect prone periphery [42].

The pixel architecture in Fig. 6(a) implements the active-reset technique [38], [43], [44], [56] to reduce the fundamental kTC capacitive reset noise limit of the photodiode capacitance. The technique reduces the thermal reset noise through bandwidth control by utilizing an amplifier with a controlled time-varying resistive feedback. In the reset phase, the SF_+ transistor is configured to form a common-source amplifier by controlling the *GRST* signal driven switches. In the reset configuration, the SF_+ transistor along with the BIAS_{N+} current source together form a common-source amplifier. During reset, the *RST* transistor is kept closed to form a unity-gain feedback common-source amplifier. The amplifier output is the pixel reset voltage given by

$$V_{\mathrm{PDRST}} = V_{\mathrm{RST}} - \sqrt{\frac{2I_1}{\beta}} + |Vtp| + V_{\mathrm{fl\_RST}} \tag{1}$$

where V_{PDRST} is the reset voltage of the photodiode, Vtp and β are the threshold voltage and the device transconductance parameter respectively, $V_{\mathrm{fl\_RST}}$ is the instantaneous flicker noise of the common-source amplifier modelled as a voltage offset at the gate of the SF_+ transistor, and V_{RST} and I_1 are the supply voltage and the bias current of the common-source amplifier respectively.

At the end of the reset cycle, the *RST* transistor is gradually opened, by slowly ramping down the *RST* signal, thus increasing its resistance. For noise reduction, the noise bandwidth of the resistive feedback must be kept lower than the noise bandwidth of the common-source amplifier for a sufficiently long period of time [56]. The thermal noise voltage stored onto the photodiode capacitance σ_{PDrst} at the end of the tapered reset can be written as [38]

$$\sigma^2_{\mathrm{PDrst}} \approx \frac{kT}{4C_{\mathrm{PD}}(1+\eta)} \tag{2}$$

where C_{PD} is the individual photodiode capacitance and η is a function of the reset switch resistance. From (2), the stored noise offset is less than the conventional kTC offset encountered in a hard reset. Taking advantage of the relaxed imager timing constraints available when imaging biochemical analytes, T_{RST} can be of the order of several milliseconds, significantly attenuating σ_{PDrst}.

Once the *RST* transistor is turned off, the integration phase begins. At the end of the integration phase, *GRST* is switched to configure SF_+ as a source-follower amplifier transistor for

pixel readout. The source follower voltage $V_{\rm SF}$ read at the end of the integration phase is given by

$$V_{\rm SF} = V_{\rm RST} + V_{\rm fl\_RST} - \frac{Q_{\rm SIG}}{C_{\rm PD}} - V_{\rm fl\_INT} \tag{3}$$

where $Q_{\rm SIG}$ is the total photocharge accumulated during the integration phase and $V_{\rm fl\_INT}$ is the instantaneous flicker noise of the source follower amplifier modelled as a voltage offset at the gate of the $\rm SF_+$ transistor. From (1) and (3), the effect of the threshold voltage and its variation over the pixel array are negated, thus reducing fixed pattern noise (FPN).

Assuming the main contribution in the flicker noise is from the $\rm SF_+$ transistor, for small integration time $T_{\rm INT}$, flicker noise terms $V_{\rm fl\_RST}$ and $V_{\rm fl\_INT}$ are correlated and cancel each other out [38]. However, for the targeted application of imaging biochemical analyte reactions, $T_{\rm INT}$ can be several hundred seconds, and thus the flicker noise terms are uncorrelated. To negate flicker noise, frame-by-frame addition is performed off-chip to cancel flicker noise of consecutive frames. The result of the summation is the total amount of photons collected over several frames $Q_{\rm total}$ given by

$$Q_{\rm total} = \sum_{i=1}^{N} \left(Q_i + (C_{\rm PD} + C_P)\left(V_{{\rm fl}(i)} - V_{{\rm fl}(i+1)}\right)\right) \tag{4}$$

which simplifies to

$$Q_{\rm total} = \sum_{i=1}^{N} Q_i + (C_{\rm PD} + C_P)\left(V_{{\rm fl}(1)} - V_{{\rm fl}(N)}\right) \tag{5}$$

where $V_{{\rm fl}(i)}$ and $V_{{\rm fl}(i+1)}$ are the instantaneous flicker noise at the start and end of the ith frame and Q_i represents the total photocharge captured in the ith frame. It should be noted that $Q_{\rm total}$ is the parameter of interest for the targeted application that yields the total amount of analyte present in a biochemical reaction.

In conventional CDS [30], the kTC offset and the flicker noise are reduced at the expense of doubling the thermal noise contribution. The noise voltage in conventional CDS $\sigma_{\rm conv\_rst}$ can be approximated as

$$\sigma^2_{\rm conv\_rst} \approx \frac{kT\!\!\!/}{C_{\rm PD}\!\!\!/} + \sigma^2_{\rm rd} - \frac{kT\!\!\!/}{C_{\rm PD}\!\!\!/} + \sigma^2_{\rm rd} \tag{6}$$

where $\sigma_{\rm rd}$ is the integrated thermal noise voltage of the source-follower output. Utilizing the combination of active reset along with tapered reset, improved noise $\sigma_{\rm tr}$ is attained, given by

$$\sigma^2_{\rm tr} \approx \frac{kTC_{\rm PD}}{4(C_{\rm PD} + C_P)^2}\left[\frac{4+3\eta}{(1+\eta)} + \frac{4C_P}{C_{\rm PD}}\right] + \sigma^2_{\rm rd} \tag{7}$$

where C_P is the parasitic capacitance at node B. During pixel binning, the noise performance $\sigma_{\rm tr\_bin}$ is given by

$$\sigma^2_{\rm tr\_bin} \approx \frac{kT}{4C_{\rm PD}(1+\eta)} + \sigma^2_{\rm rd}. \tag{8}$$

The maximum SNR attained can be expressed as

$$\rm SNR_{max} \approx \frac{\left(V_{\rm PDRST} - \frac{i_{\rm dark} t_{\rm INT}}{C_{\rm PD}}\right)^2}{\sigma^2_{\rm tr} + \frac{q i_{\rm max} t_{\rm INT}}{C^2_{\rm PD}}} \tag{9}$$

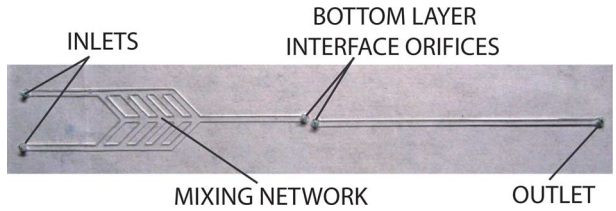


Fig. 8. Top-layer microfluidic device. The dimensions are 7.62 mm × 2.54 mm.

where $i_{\rm dark}$ is the pixel dark current and $i_{\rm max}$ is the maximum current that avoids pixel saturation.

Contact imaging a luminous object placed on the silicon die surface can lead to significant optical crosstalk due to capturing of oblique light rays. The luminous object emits light in all directions. The emitted oblique rays are blocked by utilizing a vertical metal-walled ringed enclosure placed around the photodiode. The top metal provides light shielding of pixel circuits other than the photodiode. On-chip substrate crosstalk is minimized by placing a $\rm p^+$-substrate ring tied to ground around the $\rm n^+$-p-substrate photodiode. A body-connected PMOS source follower transistor is used to improve the pixel readout linearity.

Read lines are shared between consecutive rows [41]. A modified pixel readout scheme involving pixel readouts from two consecutive rows is employed to achieve same throughput as that of a conventional 3-T pixel architecture [41]. The column readout circuit uses two PMOS transistors to provide a pseudodifferential output. A pseudodifferential input reduces the effect of mixed-signal noise coupling from the substrate and surrounding switching signals. Digital noise can be prominent in imagers where compact layout necessitates noisy digital signals existing in the vicinity of sensitive analog nodes [30]. An optimal voltage value for $V_{\rm REF}$ is chosen equal to the average of the lowest and the highest voltage level at the input of the source follower $\rm SF_+$.

V. Microfluidic Network

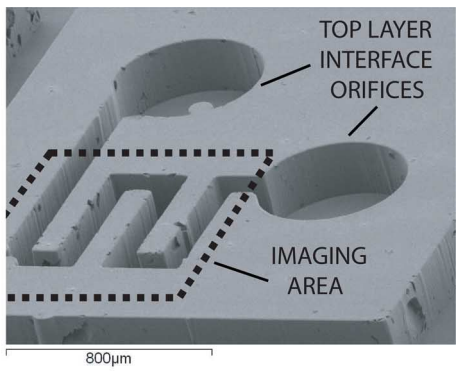
The on-chip microfluidic network consists of a glass layer, the top polydimethylsiloxane (PDMS) layer, and the bottom PDMS layer. The microfluidic structure is compression pressed over the CMOS chip to provide sealing. The top-layer microfluidic device shown in Fig. 8 contains a mixing chamber for the intake fluids. Diffusion-based mixing is slow and requires a channel length of the order of several centimeters for homogeneous mixing. To reduce the mixing distance, a mixing network was used. The inlet breaks into several equidistant channels which manually transport the fluid evenly across the width of the mixing chamber.

On-chip mixing to perform *in situ* chemical reaction enables the microsystem to perform recordings from time-sensitive chemistries. The mixed fluids are transported from the top layer to the bottom-layer microfluidic network and over the CMOS sensory array. Due to the short distance between the site of reaction and sensory detection, the transient byproduct of the chemical reaction, which is the emitted light in our case, can be easily detected by the photosensors. Hand-driven syringes were used to transport the liquid analytes through the inlets.

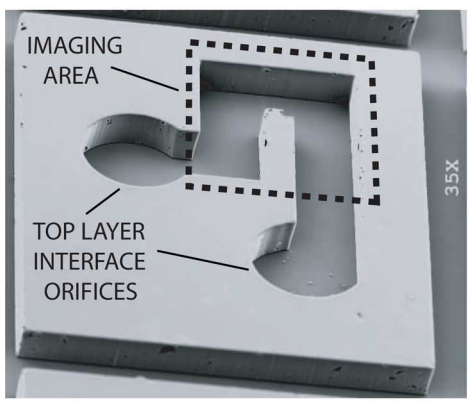
Fig. 9(a) and (b) shows SEM micrographs of two examples of the bottom layer of the microfluidic network. The depth

TABLE II
MEASURED PIXEL DARK CURRENT COMPARISON

Case	No. of transistors in the reset path	Voltage at node A	Condition in Integration Phase (0=LOW, 1=HIGH)	Dark current (mV/sec)	Dark current (fA)	Nonlinearity
(a)	1	V_{PDRST} (=2.3V)	SEL=0, G_{RST}=1, SEL_{INT}=1, RST=0, RD=1	38.1	3.8	High
(b)	1	0 V	SEL=0, G_{RST}=0, SEL_{INT}=0, RST=0, RD=1	178.9	17.9	High
(c)	2	0 V	SEL=0, G_{RST}=0, SEL_{INT}=0, RST=0, RD=0	102.0	10.2	Low
(d) (This work)	2	V_{PDRST} (=2.3V)	SEL=0, G_{RST}=1, SEL_{INT}=1, RST=0, RD=0	36.2	3.6	Low



(a)



(b)

Fig. 9. SEM micrographs of two samples of the bottom layer of the microfluidic network.

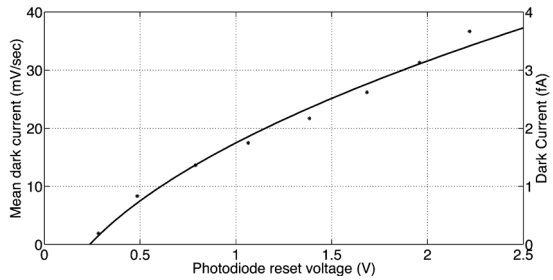


Fig. 10. Experimentally measured photodiode dark current at room temperature as a function of its reset voltage (V_{PDRST}).

of the channel in the top and bottom layers is approximately 270 μm. The channel width for the top and bottom layers are 600 and 120 μm, respectively. The inlet and outlet on the bottom-layer microfluidics measure 600 μm in diameter and are placed 300 μm away from the edge to form a good seal with the CMOS die surface. The footprint of the bottom layer microfluidic was designed to be smaller than the CMOS die to keep a clearance from the bonding pads.

Soft lithography [57] was used to fabricate each layer of the microfluidic devices. A 1:10 ratio of curing agent and prepolymer PDMS, respectively, was poured onto a master mold. The two master molds were fabricated by spincoating on cleaned glass slides two layers of negative photoresist SU8 2100 at 1750 rpm, resulting in a total layer thickness of approximately 270 μm. After soft baking the SU8 on hot plates at 65 °C and 95 °C, the designs were lithographically patterned onto the photoresist by UV exposing for 24.5 s through a transparency mask. The exposure time was determined for a Karl Suss MA6 with a 365-nm lamp with intensity 15.5 mW/cm^2 and a 405-nm lamp with 31.0-mW/cm^2 intensity. Upon molding, the two layers were treated in an oxygen plasma for 30 s and subsequently bonded after alignment. Needles were pressed to puncture holes in the PDMS layers. Metal tubes connect to the inlets and outlet on the top layer.

VI. EXPERIMENTAL RESULTS

A. Circuit-Level Experimental Results

Table II provides a comparison of the dark current recorded under various operating states of the transistors during the integration phase. The table illustrates the significant contribution of the reset transistor subthreshold leakage to the pixel dark current in a conventional 3-T pixel architecture and its reduction when utilizing a cascade of two transistors for reset. Case (a) involving a single transistor reset path with node A voltage of V_{PDRST}, illustrates the scenario present right after the release of reset in a conventional 3-T pixel architecture. The dark current observed is small due to similar voltages on the source and drain of the *RST* transistor. The subthreshold leakage however significantly degrades as the photodiode voltage decreases, making the net dark current significantly nonlinear. The worst-case dark current an order of magnitude higher was measured in case (b) that involves a single transistor reset path with node A voltage set

TABLE III
MEASURED NOISE PERFORMANCE COMPARISON WITH AND WITHOUT ACTIVE RESET

	No In-Pixel Binning		In-Pixel Binning	
T_{RST}	Active reset	Hard reset	Active reset	Hard reset
30.00ms	238 μV	480 μV	113 μV	422 μV
10.00ms	239 μV	473 μV	110 μV	422 μV
6.67ms	267 μV	477 μV	122 μV	425 μV
3.33ms	294 μV	478 μV	155 μV	424 μV
1.67ms	360 μV	472 μV	215 μV	424 μV
1.11ms	427 μV	476 μV	257 μV	422 μV
0.83ms	445 μV	474 μV	290 μV	421 μV

TABLE IV
SUMMARY OF CMOS IMAGER CHARACTERISTICS

CMOS Technology	0.35μm
Supply Voltage	3.3V
Die Area	2.9 $\times$ 2.7mm^2
Array Dimensions	64 $\times$ 128 pixels
Pixel Size	19.0 $\times$ 19.0μm^2
Fill Factor	27%
Conversion Gain	1.6 μV/e^-
Quantum Efficiency @ 480nm (with passivation)	30%
Quantum Efficiency @ 480nm (without passivation)	32%
Dark Current @ Poly-ring Bias = 0V)	36.2 mV/sec (3.6 fA)
Dark Current @ Poly-ring Bias = 3.3V)	37.7 mV/sec (3.7 fA)
Source Follower Gain (V_{REF} = 0 to 2V)	0.94 V/V
Dark Current ($V_{RST} = 2.3V$)	3.6fA
Noise with Active Reset without Binning (T_{RST}=10.0ms)	239μV
Noise with Active Reset with Binning (T_{RST}=10.0ms)	110μV
Noise at $V_{OUT}-$ (readout amplifier)	52μV
Full Well Capacity (T_{INT}=13.47sec)	1222800 e^-s
SNRmax (calculated)	60.1dB
Dynamic Range (calculated)	67.8dB
Maximum Integration Time	90 sec
Total Power	2.3 mW
Pixel Array Power	2.0 mW
Digital Power	0.3 mW

TABLE V
SUMMARY OF MICROFLUIDIC NETWORK CHARACTERISTICS

Technology	Soft lithography
Substrate	PDMS
Configuration	2-layer stacked with open channels
Sealing	Compression-sealed with CMOS die
Top Layer	
Die Area	2.54cm x 7.62mm
No. of Inlets	2
No. of Outlets	1
Inlet, Outlet Diameter	1mm
Channel Width	600μm
Channel Depth	270μm
Bottom Layer	
Die Area	2.25mm x 2.75mm
No. of Inlets	1
No. of Outlets	1
Inlet, Outlet Diameter	600μm
Channel Width	120μm
Channel Depth	270μm

to ground. This condition illustrates the scenario present at the end of the integration phase in a conventional 3-T pixel architecture, when the photodiode is completely discharged. Case (c) involves an additional off transistor in the path to ground. Comparing (b) and (c) the efficacy of the two transistor reset path in attenuating the nonlinear leakage current is demonstrated.

Employing a two-transistor reset path which is inherent to the employed shared pixel readout architecture, cases (c) and (d) demonstrate that the dark current has less spread and, thus, better linearity for the operating range of the photodiode voltage. The net reduction in the subthreshold leakage is dependent on the actual voltage division between the *RST* and *RD* switches. The low dark current achieved in case (d) enables a long integration time of as long as 90 s for $V_{\mathrm{PDRST}} = 2.3$ V. Long integration times facilitate enhanced input photocurrent sensitivity for integrating slowly varying low-level light emitted from biochemical analytes.

TABLE VI
CMOS IMAGERS DARK CURRENT COMPARISON

	Feature size (μm)	CMOS process type	Photodetector type	Photodiode area (μm^2)	Fill factor (%)	Dark current density (pA/cm^2)	Pixel blooming
[11]	0.35	standard	n^+–p-substrate	66	42.6	47000	nominal
[60]	0.18	standard	n^+–p-substrate	16	-	25000	nominal
[35]	0.5	standard	n-well–p-substrate	400	-	5000	nominal
[61]	0.6	standard	n^+–p-diffusion	600	70	420	nominal
[31]	0.18	custom	p^+–n-well and n-well–p-substrate	225000	-	390	nominal
[62]	0.5	standard	-	250000	93	80	nominal
[33]	0.35	standard	n^+–p-well	56.25	42.6	8.4	significant
[29]	0.5	standard	n-well–p-substrate	1470000	37	0.010	nominal
This work	0.35	standard	n^+–p-substrate	98	37	3620 @ $V_{RST} = 2.3V$	nominal

Fig. 10 shows the experimentally recorded dark current as a function of the reset voltage. The plot suggests significant presence of the depletion-region induced current [33] and the negligible subthreshold leakage current due to the stacked transistor reset path [55].

For noise measurements, the pixel output was fed to an external high-gain low-noise amplifier (SR560), before quantizing it utilizing a 18-b data acquisition card (NI6289). Table III provides a comparison of noise observed at $V_{\mathrm{OUT+}}$ for varying periodic reset time periods for active-reset and conventional hard-reset cases. The pixel source-follower gain was measured to be 0.94 V/V. Noise reduction with in-pixel binning and no-pixel binning cases was measured. In the active-reset case, a ramp was employed at *RST* for the time period duration T_{RST}. The active-reset technique reduces the thermal reset noise for the duration when the noise bandwidth exceeds the common-source amplifier bandwidth [38], [43]. Slower ramp speed or longer T_{RST} translate to better noise reduction. In the conventional hard-reset case, *RST* was kept high during T_{RST}. V_{RST} employed was 2.45 V to ensure switch *RST* can be hard reset [58]. As observed from the table, the measured noise does not depend on the pixel resetting frequency for the conventional hard reset case. When active reset is employed, the noise observed is much lower. The noise reduction improves with increasing T_{RST}. Better reduction is observed in the binned pixel scenario due to a higher capacitance and no switching at $RD_{A\text{-}D}$.

Tables IV and V summarize the experimental characteristics of the CMOS imager chip and the microfluidic network, respectively. The dimensions of the pixel group shown in Fig. 6 are 38 μm × 38 μm. Each individual subpixel consisting of one photodiode $RD_{A\text{-}D}$ and a part of the shared pixel transistors measures 19 μm × 19 μm. The pixel fill factor or the percentage of the photosensitive area in a pixel is 37%. The quantum efficiency of the photodiodes was measured by utilizing an external photometer device to calculate the amount of incident photons. The designed CMOS chip has two different types of pixel layouts, one with the passivation layer on top of the photodiodes and the other without the passivation layer. A 2% increase in the photosensitivity was measured in the pixels that did not have a passivation layer on top of them. A slight improvement in the dark current is observed when the polysilicon ring surrounding the photodiode is grounded. Grounding the ring, reduces the perimeter dark current while also reducing the perimeter photodiode capacitance. Full well capacity decreases with increasing T_{INT} due to integrating the dark current. The maximum SNR and dynamic range were estimated at $T_{\mathrm{INT}} = 13.4$ s utilizing the experimentally measured noise floor, dark current, and the full well capacity.

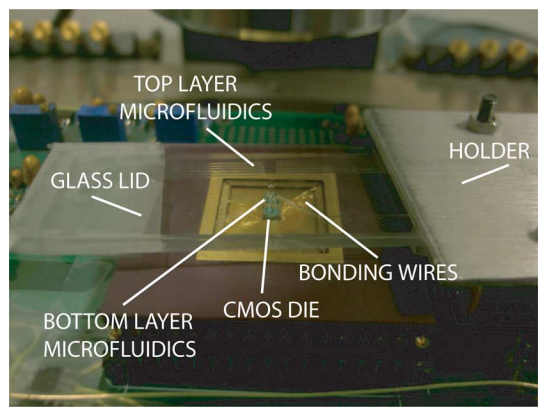


Fig. 11. Closeup image of the microfluidic-imager assembly.

Table VI provides a comparison of the dark current of various CMOS imagers designed for low-light sensitivity. The dark current increases as the minimum channel length decreases due to higher doping concentrations which degrade diode junction leakage currents. As observed from the table, the dark current worsens with the decrease in the photodetector area, as the perimeter component of the photodiode dark current contributes significantly in small photodiodes. The implemented imager achieves a very low dark current of 3.6 nA/cm^2 for a small pixel area of 98 μm^2. The only other design with both smaller pixel and lower dark current density [32] suffers from pixel blooming due to the utilization of a millimeter-sized photodiode demarcated utilizing polysilicon lines to create an array. Additionally, unlike in [28] and [30], the low dark current in the presented design is achieved for the reset voltage across the photodiode equal to 2.3 V. A high reset voltage ensures a high

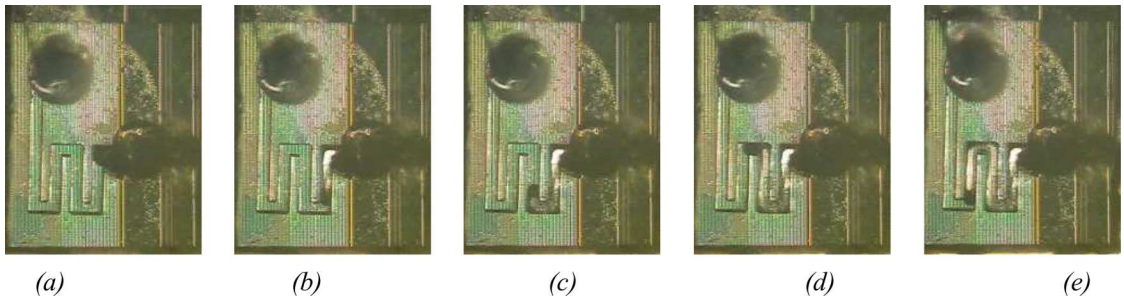


Fig. 12. (a)–(e) From left to right, top-view microscopic capture of liquid flow patterns inside the CMOS/microfluidic microsystem.

well capacity, which in turn improves the input photocurrent sensitivity. A custom CMOS technology was used in [30] to reduce the dark current.

B. System-Level Experimental Results

Fig. 11 shows the microfluidic network attached to the CMOS die. The microfluidic network glass slide is clamped by the holder which is mounted on a micromanipulator. The micromanipulator provides microscale precision alignment in X, Y, Z, and Θ directions. The alignment of the bottom-layer microfluidic network over the CMOS die is done under a microscope. For alignment ease, the bonding pads of the CMOS die are placed only on two sides. The microfluidic device is compression-sealed against the CMOS die. Fig. 12 shows the top-view microscopic capture of a drop of liquid flowing inside the microfluidic channel on the top of the CMOS die.

To validate the functionality of the integrated microsystem, an on-chip CL detection experiment using luminol was performed. Upon reaction with hydrogen peroxide, luminol generates an excited aminophthalate state, which relaxes to the ground state, emitting a blue light. The reaction is short lived, lasting only a few seconds. For optimal chemical reaction kinetics, the reaction base is kept basic with a pH of 13.0 along with a cuprous sulphate solution. A luminol enhancer is used to improve the efficiency of the light reaction. The luminol concentration used was 1 mM. 3% hydrogen peroxide solution was employed. The equations governing the chemical reaction are as follows:

$$\text{luminol} + H_2O_2 \longrightarrow \text{3-aminophthalate}^* + N_2 + 2H_2O$$
$$\text{3-aminophthalate}^* \longrightarrow \text{3-aminophthalate} + \text{blue light (480 nm)}.$$

In the CMOS-microfluidic microsystem, the two reactants, luminol and hydrogen peroxide, are fed in using the two inlets on the top layer of the microfluidic structure. The reactants mix through diffusion-based mixing, close to the entrance to the bottom layer microfluidic device. The short-lived chemiluminescence reaction produces light which is detected by the imager. The light glowing mixture flows over the pixel array. The volume of the microfluidic channel over one pixel is approximately one microliter, which corroborates the sensitivity of the microsystem. The time of integration to collect sufficient amount of chemiluminescent light was set between 1 and 52 s. The bottom layer of the microfluidic network was placed over one half of the pixel array. The pixel architecture was configured

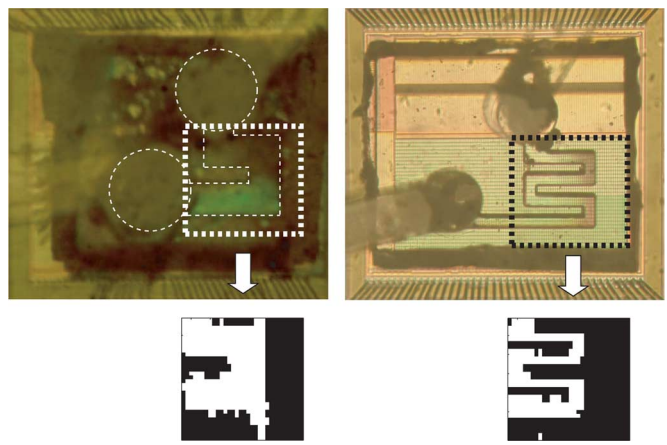


Fig. 13. Experimentally captured luminol CL patterns detected in the microfluidic channels on the CMOS die.

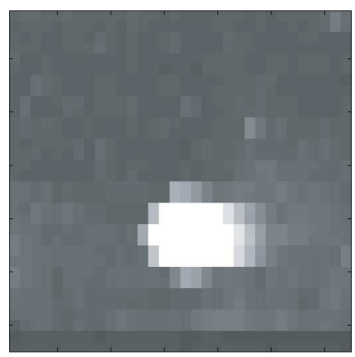


Fig. 14. Half-pixel array capture of low-level light ECL ($T_{\mathrm{INT}} = 13.47$ s).

in the binning mode to provide a 32×32 pixel array resolution. The top of Fig. 13 shows the micrographs of the fluidic chambers of Fig. 9(a) and (b) attached to the surface of the CMOS die. The bottom of Fig. 13 shows the experimentally recorded luminol CL in the microfluidic channel over the CMOS die. Note that the channel footprint as recorded by the CMOS imager is irregular due to scattering of light from the vertical edges of the fluidic channel, which are 270 μm high.

Fig. 14 shows a half-pixel array capture of ECL occurring on top of the CMOS chip, validating its usability in imaging low-level light chemical reactions. To create a large chemical event shape to be imaged by multiple pixels, the ECL was generated utilizing two off-chip gold electrodes with a diameter of 400 μm. The tip of the gold working electrode placed on the top of the CMOS die surface illuminates. The time of integration set for the imager was 13.47 s. The luminol concentration was

2 mM in a pH 13.0 solution containing a drop of cuprous sulphate (CuSO4). The ECL light decay associated with a stagnant analyte was avoided by applying an alternate excitation and cessation voltage via an off-chip digital-to-analog converter [62]. Pixel binning was employed along with subdark current measurements. Subdark current measurements involve subtracting off-chip the captured frame from the stored dark signal frame recorded for the same integration time. The uneven pixel illumination in the background can be attributed to the imaging of light refraction from the liquid meniscus and the background light. The lower half of the pixel array is brighter due to the removal of the passivation layer opening on top of the photodiodes from the bottom half of all pixels. This experiment functionally validates the utility of the microsystem in biochemicals detection.

VII. Conclusion

A hybrid CMOS and microfluidic microsystem for optical contact imaging of biochemical analyte reactions has been presented. It performs direct-contact imaging at a high pixel resolution, enabling the usage of multiple microfluidic channels for a higher throughput. The two-transistor reset path technique has been successfully demonstrated to achieve fairly constant ultra low dark currents at photodiode reset voltages close to the supply, thus significantly enhancing the integration time and the input photocurrent sensitivity. An active reset technique along with in-pixel flicker noise cancellation have been employed for noise reduction. The microsystem has been experimentally validated in on-chip luminol CL and ECL The present work successfully demonstrates the potential of the proposed microsystem in the development of a low-cost, small-form-factor, accurate chemical analyte sensing technology.

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Ritu Raj Singh (S'08) received the B.Tech. degree in electrical engineering from the Indian Institute of Technology, Kanpur, India, in 2005, and the M.A.Sc. degree in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 2009. He is currently working toward the Ph.D. degree from the University of Texas at Austin.

His research interests include biosensors, CMOS integrated sensors, and analog and mixed-signal integrated circuits and systems. He has held engineering positions at Insilixa, Sunnyvale, CA, Silicon Laboratories, Austin, TX, Granite SemiCom Inc., Toronto, ON, Canada, Mentor Graphics, India, and Texas Instruments, India.

Lian Leng, photograph and biography not available at the time of publication.

Axel Guenther, photograph and biography not available at the time of publication.

Roman Genov (M'96–SM'02) received the B.S. degree (first rank) in electrical engineering from Rochester Institute of Technology, Rochester, NY, in 1996, and the M.S. and Ph.D. degrees in electrical and computer engineering from Johns Hopkins University, Baltimore, MD, in 1998 and 2002, respectively.

He has held engineering positions with Atmel Corporation, Columbia, MD, in 1995, and Xerox Corporation, Rochester, NY, in 1996. He was a Visiting Researcher with the Laboratory of Intelligent Systems, Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 1998 and with the Center for Biological and Computational Learning, Massachusetts Institute of Technology, Cambridge, in 1999. He is presently an Associate Professor with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada. His research interests include analog and digital VLSI circuits, systems, and algorithms for energy-efficient signal processing with applications to electrical, chemical, and photonic sensory information acquisition, biosensor arrays, brain–silicon interfaces, parallel signal processing, adaptive computing for pattern recognition, and implantable and wearable biomedical electronics.

Dr. Genov received the Canadian Institutes of Health Research (CIHR) Next Generation Award in 2005, the Brian L. Barge Award for excellence in microsystems integration in 2008, the DALSA Corporation Award for excellence in microsystems innovation in 2006 and 2009, and the Best Paper Award on sensors and Best Student Paper Award, both at the IEEE International Symposium on Circuits and Systems in 2009. He is an associate editor of IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, and IEEE SIGNAL PROCESSING LETTERS.