

915-MHz FSK/OOK Wireless Neural Recording SoC With 64 Mixed-Signal FIR Filters

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Abstract—A system-on-chip (SoC) neural recording interface with 64 channels, 64 16-tap programmable mixed-signal FIR filters and a fully integrated 915 MHz OOK/FSK PLL-based wireless transmitter is presented. Each recording channel has a fully differential amplifier with 54 dB gain and utilizes a tunable low-distortion subthreshold MOS-resistor to reject DC offsets with an input-referred noise of $6.5 \mu\text{V}$ and a CMRR of 75 dB. Each channel contains a modified 8-bit SAR ADC with an ENOB of 7.8-bits and can provide analog-digital multiplication by modifying the the sampling phase of the ADC. It is used in conjunction with 12-bit digital adders and registers to implement 64 programmable transposed FIR filters. The 915 MHz FSK/OOK transmitter offers data rates up to 1.5 Mbps and a maximum output power of 0 dBm. The $4 \times 3 \text{ mm}^2$ chip fabricated in a $0.13 \mu\text{m}$ CMOS process dissipates 5.03 mW from a 1.2 V supply. Experimental measurements characterize the electrical performance of the wireless SoC. *In vivo* measurement results from freely moving rats are also presented.

Index Terms—Extracellular recording, implantable wireless SoC, mixed-signal FIR filters, multi-channel neural recording, neural recording SoC.

I. INTRODUCTION

MONITORING neuro-electrical activity in the brain is a vitally important method in diagnostics and evaluation of various neurological disorders such as epilepsy. A number of non-invasive techniques are employed for brain function testing such as scalp surface EEG, MEG, fMRI and PET scans. These methods are complementary to each other and often have limited applicability and efficacy. Intracranial electrical recordings known as electrocorticography (ECoG) record local field potentials (LFPs) on the cortex surface and provide better signal-to-noise ratio, higher bandwidth, up to 500 Hz of signal content, as well as increased spatial resolution compared to scalp surface EEG. The 64-site ECoG is currently the gold standard procedure for seizure localization in most patients with intractable epilepsy, who are candidates for resective

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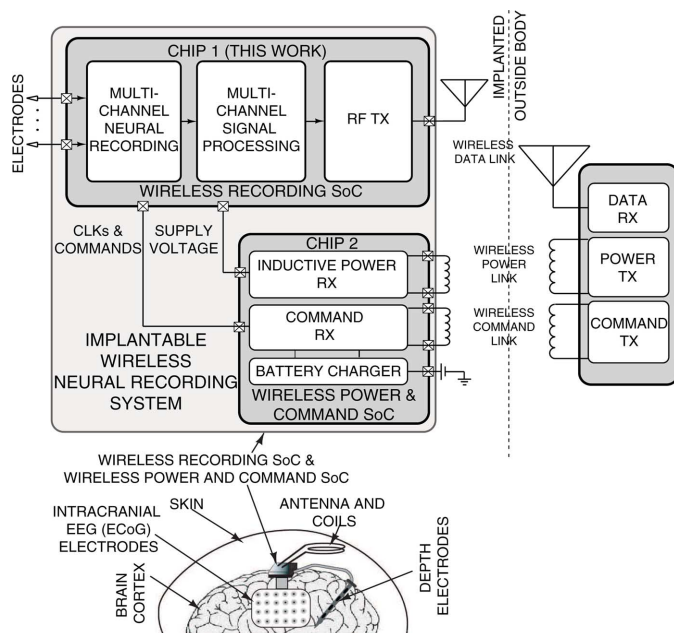


Fig. 1. System diagram of the envisioned implantable wireless neural recording system.

surgery. Other invasive methods include neural recording from microelectrodes, such as Utah electrode arrays. They allow for recording of wider-bandwidth single neuron activity (neural spikes) in addition to LFPs. Typically for ECoG recordings, the signals are in the range of $10 \mu\text{V}$ to 5 mV with frequencies below 500 Hz. For microelectrodes, signals include frequencies up to 7 kHz [1]. Currently most of the methods for recording neural activity involve tethered wires connecting the electrodes to bench-top neural amplifiers. Tethered wire connections restrict the freedom of movement for a patient, are more sensitive to artifacts and interference, and increase the risk of an infection.

A conceptual view of a fully integrated wireless implantable neural recording microsystem is shown in Fig. 1. Two chips are combined in one encapsulated package which connects to an RF antenna, inductive coils, an electrode array and a battery. The first system-on-chip (SoC) (chip1) provides multi-channel neural recording for LFPs and neural spike signals, signal processing and a low-power RF wireless link to the baseband receiver located outside the human body. The second SoC (chip2, not described in this paper) includes a wireless inductive power link and a command link to deliver energy and commands, respectively, to the first SoC. The wireless interface enables the freedom of movement for a patient, reduces artifacts and noise in the recording data and reduces the risk of an infection. The

implantability requirement imposes the constraints of a small overall form factor for the device and low power dissipation. Low power dissipation is important in order to avoid thermal damage to the tissue and to minimize the power transmitted to the device inductively. By integrating the neural recording, signal processing and RF transmission functions into a single SoC, both the size and power dissipation of the device can be significantly reduced.

The power and area constraints imposed by an implantable device have restricted on-chip signal processing to simple algorithms, such as spike detection or to computing on a few recording channels [2]–[5]. Adding advanced, customizable on-chip signal processing algorithms such as FIR filters capable of operating on many recording channels can significantly expand the functionality of an implant. When recording from a large number of channels, the wireless data transmission rate can be reduced by data compression. Noise and interference can be suppressed. Precise bandpass filtering of neural signals such as LFPs or neural spikes can be implemented. Other advanced tasks such as feature extraction and data classification enable a closed-loop system implementation such as that with locally triggered neural stimulation or drug delivery. Lastly, on-chip signal processing can be utilized to power down the RF transmitter and further reduce the power dissipation of the implantable device.

Recently, a number of neural recording SoCs have been reported which combine multi-channel neural recording, digitization, signal processing and/or RF transmission on a single chip. Our previous work in 0.35 μm CMOS resulted in microsystems with 256 neural recording channels with on-chip data compression [6], 128 neural recording and stimulation channels with 16 column-parallel ADCs [7] and 256 neural recording and 64 stimulation channels with in-channel ADCs [8], but without advanced signal processing or a wireless interface.

Integration of 96 recording channels and in-channel ADCs in 0.13 μm CMOS was demonstrated in [9]. The large area and power dissipation constrain the system and make further integration of signal processing and an RF transmitter difficult. The 0.18 μm CMOS neural recording SoC in [4] demonstrates neural stimulation on 64 channels and recording on eight channels with a single FIR filter. A low-power 0.13 μm neural recording system in [10] demonstrates eight neural recording channels digitally multiplexed to a single 8-channel SAR ADC. For lower bandwidth scalp surface EEG applications (<200 Hz), the SoCs in [11], [12] demonstrate low-noise front-ends with a single high-resolution ADC. The single-channel design in [11] also integrates FIR filters and signal processing. The design in [12] integrates eight channels with a single high-resolution ADC. The previously reported designs in [9], [4], [10], [11] and [12] do not integrate a wireless transmitter, and either have a low number of recording channels or low-complexity signal processing, or both.

The requirements of a large number of recording channels (64 or higher) and a wide signal bandwidth (7 kHz) translate to a high output data rate (>1 Mbps) of the transmitter. As discussed earlier, tissue heating and available inductive power budget severely limit the transmitter output power and data rate. Existing SoC designs overcome this limitation by transmitting only neural spikes on most or all channels [2], [3] and by utilizing simple low-power transmitter architectures [2],

[13] and [14]. Spike detection results in a loss of vital information such as neural oscillations in the gamma band present in patients with epilepsy, schizophrenia, Alzheimer's disease and other neurological disorders. Simple wireless transmitter architectures for neural recording have shortcomings and are typically not fully integrated. Open-loop VCO designs [2], [13], [5] suffer from temperature sensitivity and frequency drift. A closed-loop transmitter architecture addresses these issues by ensuring the output frequency is locked to a precise reference crystal oscillator. Closed-loop wireless transmitters for neural SoCs were implemented in [3] and [15]. The wireless transmitter in [3] suffers from high power dissipation and requires off-chip components, limiting its ability to operate as an implantable device. The design in [15] consists of only a single neural recording channel and also requires off-chip components. Lastly, the SoC in [16] integrates 128 neural recording channels, column-parallel ADCs and FIR filtering with a basic UWB wireless transmitter, resulting in a wireless link that is susceptible to interference and noise making it impractical for a chronically implantable device.

We present an implantable SoC that densely integrates 64 neural recording amplifiers and ADCs, 64 programmable 16-tap FIR filters, an on-chip digital controller and a fully-integrated closed-loop wireless transmitter on a 4 mm \times 3 mm 0.13 μm CMOS die. This paper extends on an earlier reported 64-channel neural recording wireless interface system-on-chip (SoC) described in [17]. The SoC performs versatile signal filtering individually configurable for each channel to extract information of interest such as beta, gamma or other frequency bands, local-field potentials (LFP) and spikes. It also performs interference suppression, spike detection, precise bandwidth control and a variety of other filtering tasks. A mixed-signal FIR filter implementation eliminates the need for 512 conventional 8-bit digital multipliers by efficiently implementing the multiplication within the ADC conversion cycle. This results in over an order of magnitude savings in the power-area product. In summary, by minimizing both the area and power dissipation, an SoC that successfully integrates a large number of neural recording channels with advanced signal processing and a robust fully integrated wireless link onto a single chip is demonstrated.

The rest of the paper is organized as follows. Section II discusses the VLSI architecture of the neural recording SoC. Section III presents the circuit implementation of the key functional blocks in the SoC. Section IV presents experimental results of the individual blocks, the full system and in vivo characterization in rodents.

II. SYSTEM ARCHITECTURE AND VLSI IMPLEMENTATION

The full system VLSI architecture with 64 neural recording amplifiers is shown in Fig. 2(a). The SoC connects to a 64-electrode ECoG grid or a microelectrode array to record neural signals with frequencies as low as 0.1 Hz and as high as 7 kHz and with signal amplitudes between 30 μV and a 1–2 mV [18]. This requires the analog front-end to have an integrated noise below 10 μV and an ADC resolution of at least 8 bits to enable enough dynamic range between 30 μV and 1–2 mV.

Each channel contains a programmable mixed-signal 16-tap FIR filter. It has two modes of operation. In the first mode, the amplified signal is digitized by an in-channel ADC. In the

second mode, the neural amplifier output is digitized and filtered using an in-channel mixed-signal FIR filter. The FIR filtering mode reuses the same in-channel ADC as an analog-to-digital multiplier to perform the bulk of the FIR computations with a minimal area and power overhead.

Design requirements for some commercial implantable medical transmitters are limited power dissipation of 6 mW (due to peak current limitations in small implantable batteries), minimum external passive components due to a small form factor (less than 10 mm²), reasonable data rates (higher than 20 kb/s), high reliability and a 2 meter minimum transmission range [19]. Losses due to the small form factor of the antennas, body tissue absorption and fading are approximately 40–45 dB [19]. The FCC allocates the Medical Implant Communication Service (MICS) frequency band (402–406 MHz) for wireless implantable medical devices. This band has a 300 kHz maximum bandwidth and a maximum output power of –16 dBm [19]. The industrial, scientific and medical (ISM) radio bands are also frequently used for implantable medical transmitters. These include the 902 MHz to 928 MHz, the 2.4 GHz to 2.4835 GHz and the 5.725 GHz to 5.875 GHz frequency bands and have transmission ranges as high as 10 meters and an allowable output power of 0.5 mW [20]. Lower frequencies require larger antennas, where as higher frequencies have higher losses due to tissue absorption. The optimum frequency band for wireless implantable transmitters was previously determined to be approximately 900 MHz [20]. To ensure robust frequency control due to temperature and frequency drift and minimal form-factor for implantability a fully integrated PLL-based transmitter is selected.

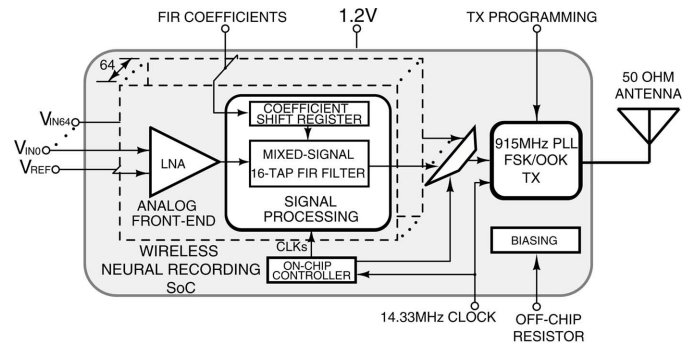
The digital data are modulated using either Manchester encoded frequency-shift keying (FSK) or on-off keying (OOK) and are sent to the 915 MHz PLL-based transmitter. On-chip shift registers are programmed externally and store coefficients for the FIR filters, and program modes for the RF transmitter. Bias currents can be tuned through an external on-board bias resistor. A single off-chip 14.32-MHz crystal oscillator acts as the reference clock for the RF transmitter and is also used to generate all on-chip clocks for the ADC, FIR filters and data modulation.

Fig. 2(b) shows the micrograph of the 4 × 3 mm² wireless neural recording SoC fabricated in a standard 1P8M 0.13 μm CMOS technology. An array of 8 × 8 neural recording channels and in-channel 8-bit ADCs is organized on a 300 μm pitch grid to be flip-chip bonded to a 8 × 8 trace carrier or directly to an electrode array. Digital logic to implement the add-and-delay functionality of 64 8-bit FIR filters are split above and below the 64-channel array. The fully integrated RF transmitter and digital control logic are located at the top of the chip.

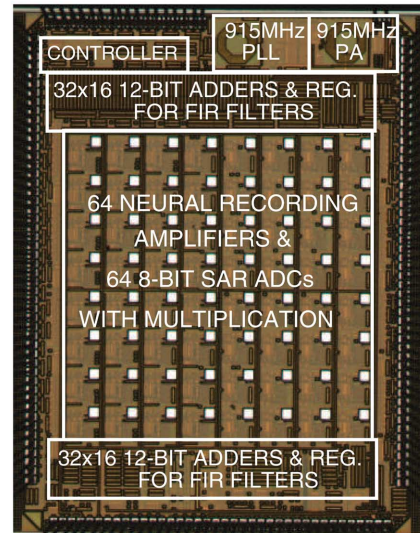
III. VLSI IMPLEMENTATION

A. Mixed-Signal FIR Filter

In the FIR filtering mode a 16-tap transposed FIR filter architecture depicted in Fig. 3(a) is employed. Conventionally this architecture requires 16 8-bit digital multipliers for each recording channel. This number can be reduced by half when there is symmetry in the filter coefficients $|M_i| = |M_{15-i}|$ for



(a)



(b)

Fig. 2. (a) Simplified system diagram of the wireless neural recording SoC. (b) Micrograph of the 4 mm by 3 mm 0.13 μm CMOS SoC.

$i = 0, 1, \dots, 15$ so only eight filter coefficient absolute values are utilized in the multiplication. We use a bank of eight adjacent channel ADCs to implement this computation in parallel as depicted in Fig. 3(b). As shown in Fig. 3(c) the outputs of eight LNAs are multiplexed and each output is sampled by eight ADCs in parallel. Each ADC output is fed to two simple digital sign multipliers in the corresponding two slices of the 16-tap add-and-delay line. Eight add-and-delay lines corresponding to the eight input channels are clocked cyclicly by the on-chip digital controller. The simplified control signals for the ADC and FIR filters are shown in Fig. 3(d). The SAR logic within the ADC operates at 625 kHz and is divided by 11 to sample its input at 56.8 kS/s. The ADC sampling clock is further divided by 8 to generate 7.2 kHz for the FIR filters. A 3-bit counter output, *SELECT*, is synchronized with the ADC sampling clock and cycles the output of the neural recording amplifier and its corresponding FIR filter clock. The cyclic operation of the FIR filtering is further detailed in Figs. 3(e) and (f) for two different channels. The total latency of a single FIR filter operating at 7.2 kS/s is 1.5 ADC samples (17.6 μs) and 1 FIR filter sample (139 μs).

This architecture is tiled eight times for a total effective number of 64 FIR filters. In this mixed-signal FIR implementation the 512 digital multipliers (8 for each of 64 channels)

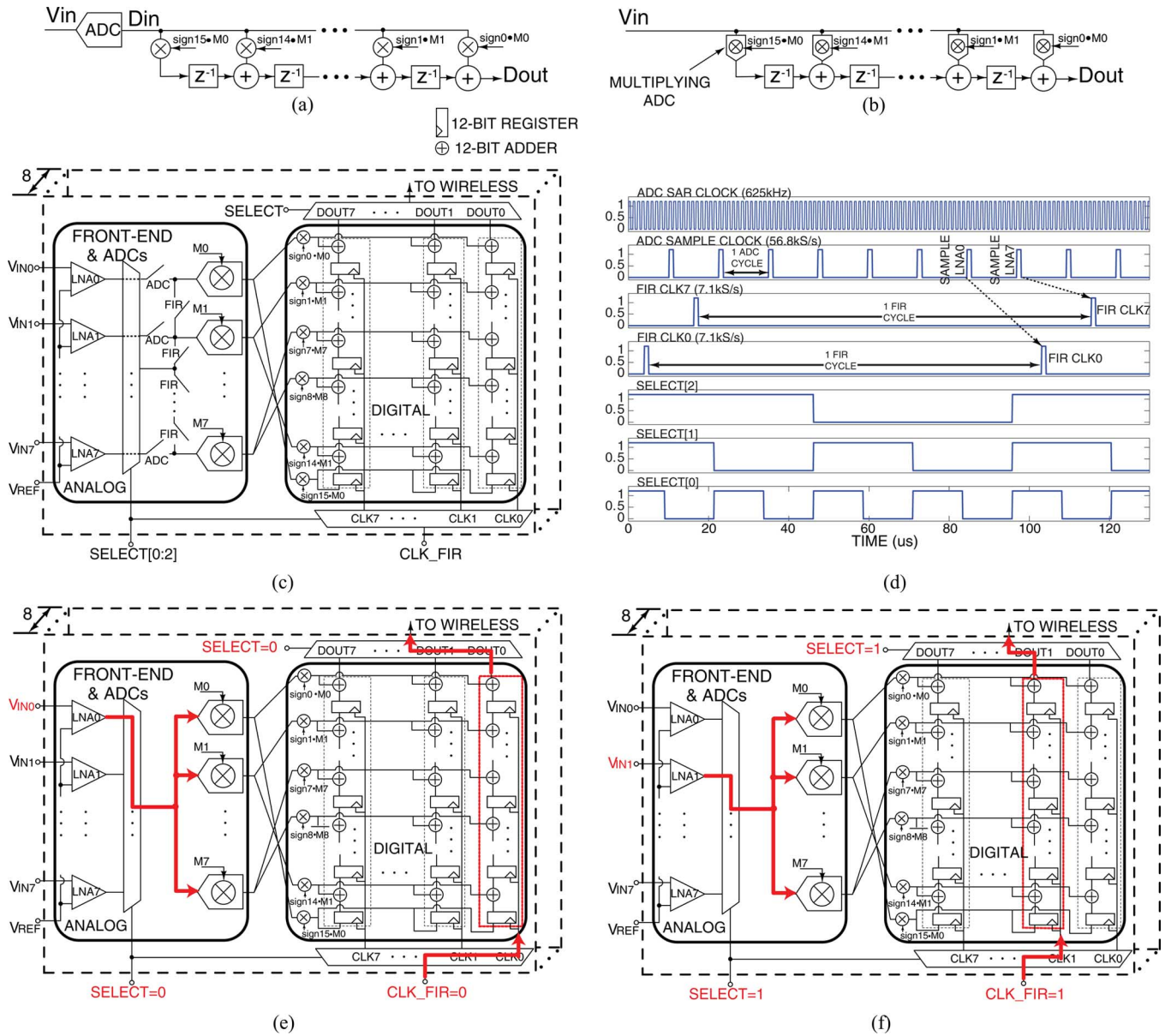


Fig. 3. (a) Conventional 16-tap transposed FIR structure. (b) Mixed-signal 16-tap transposed FIR filter structure. (c) Schematic of 64 implemented mixed-signal 16-tap symmetric transposed FIR filters. (d) Control signals for FIR filter. (e) Schematic of 64 implemented mixed-signal 16-tap symmetric transposed FIR filters with control signals and clocks enabled to output *channel0*. (f) Schematic of 64 implemented mixed-signal 16-tap symmetric transposed FIR filters with control signals and clocks enabled to output *channel1*.

as depicted in Fig. 3(a) (for 1-channel) are eliminated from the system, while the ADCs are clocked 8 times faster ($8f_s$) than the in-channel sampling rate (f_s). The scalable implementation allows for in-channel analog-to-digital conversion of raw recorded data on 64-channels at a ADC sample rate of f_s per channel, FIR filtering on 8-channels at a ADC sample rate of f_s per channel or FIR filtering on 64-channels at a ADC sample rate of $8f_s$ per channel. The implemented 64-channel mixed-signal FIR approach adds a 20% area and 2X power overhead when compared to an SoC with an in-channel ADC without FIR filters or signal processing. Our approach yields 10 times less area and 1.5 times less power dissipation for the 16-tap FIR filters when compared with a fully digital 16-tap FIR filter implementation (estimated through place-and-route tools in the same $0.13 \mu\text{m}$ CMOS technology) with 512 multipliers

for a savings in the power-area product of a factor of 15. The digital switching noise of digital multipliers is also eliminated.

In this design, the 16-tap length was selected for each FIR filter. Each channel requires eight parallel MADCs (each MADC yields two multiply operations due to symmetry in a transposed FIR filter implementation). To obtain higher band selectivity in lower frequency bands such as the alpha, beta and gamma neural bands, the system sample rate can be lowered and the pass band of the 2nd stage of the neural recording amplifier can be decreased to match that of the FIR filter. This results in steeper band rolloffs. Power dissipation of the FIR filter decreases linearly with the sample rate.

Furthermore, for this mixed-signal VLSI FIR filter architecture, it is possible to scale up the tap count by utilizing more parallel MADCs per channel to increase the length of the FIR

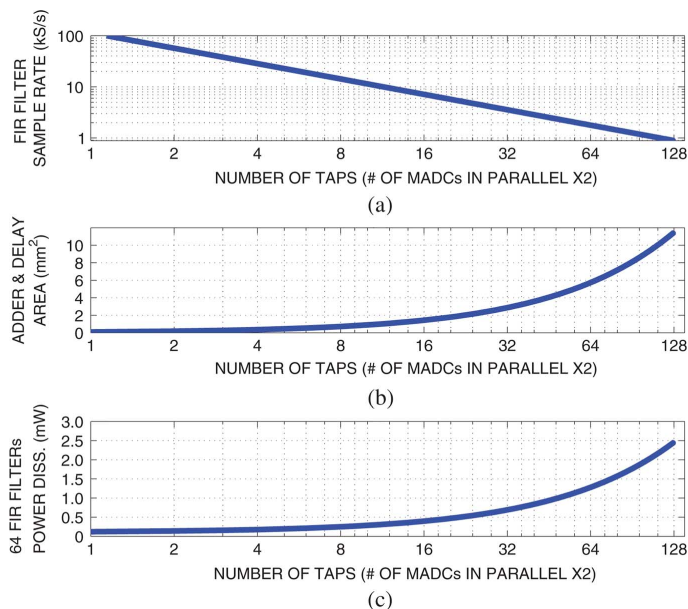


Fig. 4. Scalability of the proposed FIR filter in terms of: (a) input sample rate, (b) integration area and (c) power dissipation.

filter (up to 64 128-tap FIR filters) in order to further increase the FIR filters selectivity. Increasing the FIR filter length by utilizing more parallel MADCs per channel impacts the sample rate, area and power dissipation. Based on experimental results and area utilization in this prototype SoC, the estimated sample rate, area and power dissipation for 64 FIR filters with respect to the number of filter taps are shown in Fig. 4(a), (b) and (c), respectively. Maintaining the same ADC sample rate per channel decreases the FIR filter sample rate due to the cyclic timing of the architecture. The area and power dissipation also increase as more digital adders and registers need to be integrated onto the SoC.

B. Neural Recording Amplifier

Each LNA in Figs. 2(a) and 3(c) implements a neural recording amplifier. The schematics of the neural recording amplifier and the two OTAs are shown in Fig. 5. Amplification and filtering are performed over two stages with a total gain of 54 dB set by the input to feedback capacitor ratio. The first stage uses a fully differential architecture to ensure a high CMRR, which is important for dense analog-digital SoC implementations. The first stage uses a fully differential folded-cascode OTA with a gain of 60 dB. To minimize the flicker noise of the input differential pair M1/M2, large PMOS devices are utilized. To minimize the thermal noise, the input-pair transistors are biased in the sub-threshold region to maximize their g_m/I_D ratio, while transistors M3/M4 and M5/M6 are biased in the saturation region to minimize their g_m/I_D ratio. Common-mode feedback (CMFB) is implemented by modulating the tail current of the first stage of the folded-cascode OTA using a continuous-time CMFB amplifier while maintaining the common-mode voltage at 0.6 V. The OTA requires a total of 2.4 μA of current which includes 1.6 μA into the input pair, and 0.8 μA into the cascode transistors. The second stage

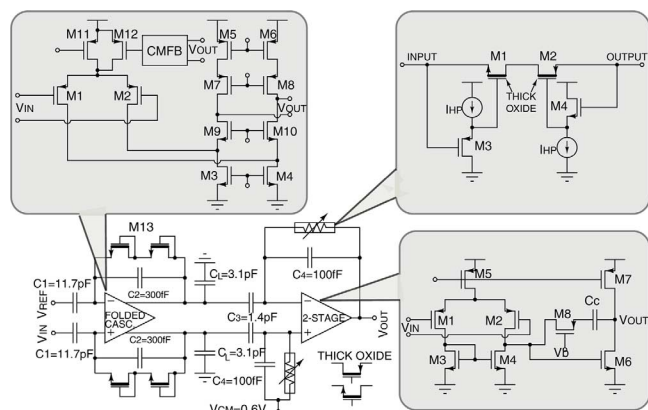


Fig. 5. Schematic of the analog front-end.

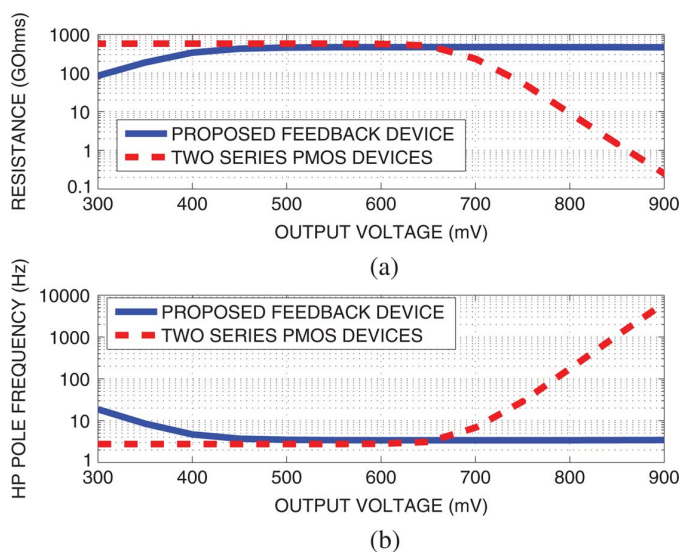


Fig. 6. (a) Simulated resistance across the amplifier output range for the proposed feedback device and for two series PMOS devices with a constant V_{GS} . Both cases have V_{GS} of 0.1 V. (b) Simulated high-pass frequency pole across the amplifier output range for the proposed feedback device and for two series PMOS devices, based on a 100 fF feedback capacitor.

OTA requires a high output swing and thus is implemented using a 2-stage OTA. The single-ended OTA has 60 dB of gain and utilizes PMOS input devices. A total of 350 nA of current is consumed by the OTA, with 100 nA in the input stage and 250 nA in the second stage. All OTAs utilize standard thin-oxide transistors.

The first stage has a small output swing and uses two long thick-oxide NMOS pseudo-resistors as feedback elements. Along with C_2 they yield a high-pass pole set at 0.1 Hz. It is important to be able to tune to the bandwidth allowing attenuation of the low frequency drift or DC offsets and also to shift the high-pass pole to correct for process variation. The pseudoresistor in the first stage can be made tunable by setting the gate of the MOS transistor to a programmable DC voltage [6] and operating the device in subthreshold. Setting the V_{GS} of the feedback device too low leads to leakage issues and bias drifts often saturating the OTA. The pseudoresistor, as implemented in the first stage, exhibits distortion if large output

TABLE I
TRANSISTOR SIZES OF THE TWO OTAS AND THE FEEDBACK ELEMENT (F.E.)
OF THE NEURAL AMPLIFIER AND THE COMPARATOR OF THE ADC

Transistor (OTA1)	W/L (μm)	Transistor (OTA2)	W/L (μm)
$M_{1,2}$	$25 \times 2/1.5$	$M_{1,2}$	$4 \times 0.5/5$
$M_{3,4}$	$4 \times 0.5/15$	$M_{3,4}$	$2 \times 0.5/10$
$M_{5,6}$	$4 \times 1/10$	M_5	$2 \times 0.8/3$
$M_{7,8}$	$4 \times 0.6/1$	M_6	$2 \times 1.0/3.8$
$M_{9,10}$	$4 \times 0.6/1$	M_7	$5 \times 0.8/3$
M_{11}	$4 \times 1/2$	M_8	$2 \times 2.5/1$
M_{12}	$1 \times 1/2$	C_c	1pF
M_{13}	$2 \times 0.5/5$		
Transistor (F.E.)	W/L (μm)	Transistor (Comparator)	W/L (μm)
M_1	$1 \times 0.5/15$	$M1$	$1 \times 0.5/2$
M_2	$1 \times 0.5/15$	$M2$	$4 \times 2.5/1$
M_3	$2 \times 2.5/0.5$	$M3$	$2 \times 0.5/8$
M_4	$3 \times 1.0/0.5$	$M4$	$4 \times 2.5/1$
—	—	$M5$	$2 \times 0.3/5$
—	—	$M6$	$2 \times 2.5/1$
—	—	$M7$	$1 \times 1/0.24$
—	—	C_{OFF}	170fF

swings were to be present. Thus it is not suitable for use in the second stage [2], [21].

These issues are addressed by implementing the feedback resistor in the second stage by dynamically adjusting the gate voltages of two MOS transistors using two source-followers. This ensures a constant V_{GS} on the subthreshold feedback devices for large output swings as shown in Fig. 5 (top, right). The resistance can be reduced by increasing the bias current in the source followers and thus increasing the $|V_{GS}|$ of the MOS devices. The area is minimized by utilizing low-threshold devices to allow $|V_{GS}|$ tunability between approximately 0.1 V and 0.3 V without requiring a wide device. Utilizing both NMOS and PMOS devices ensures at least one device has the proper $|V_{GS}|$ to implement a large resistance across the full output swing of 0.6 V. Additionally, compared to the conventional approach [6], this feedback resistance achieves more accurate biasing by guaranteeing a controlled resistance (i.e., with a $|V_{GS}| > 0$ V) on the devices in the feedback. A 10–15 dB improvement in distortion at sub-Hz frequencies was observed experimentally when using the implemented approach in Fig. 5 (top, right) over the conventional subthreshold transistor when used in the second stage.

This is illustrated by the simulation result shown in Figs. 6(a) and (b). In this simulation one node of the feedback device is tied to the common-mode (CM) node of 0.6 V, while the output node is swept from 0.3 V to 0.9 V representing the output range of the amplifier. The proposed feedback device had a V_{GS} of 0.15 V and was compared with two PMOS devices in series [6] with a V_{GS} of 0.15 V. The proposed feedback device had its high-pass pole shift from 3.4 Hz to 20 Hz which would introduce distortion at low frequencies (below 20 Hz). This occurs when the output signal is low as a result of large output swings such as 0.4 V or higher. The case with two series PMOS devices had its high-pass pole shift to above 6 kHz when the output is at full swing resulting in much higher distortion than the proposed case.

All transistor sizes for the neural recording amplifier are listed in Table I.

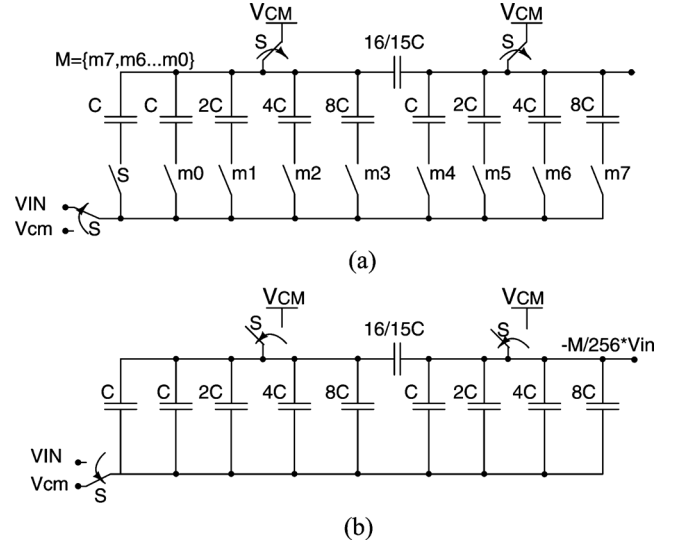


Fig. 7. (a) Sampling phase of multiplying SAR ADC. (b) Hold phase of multiplying SAR ADC.

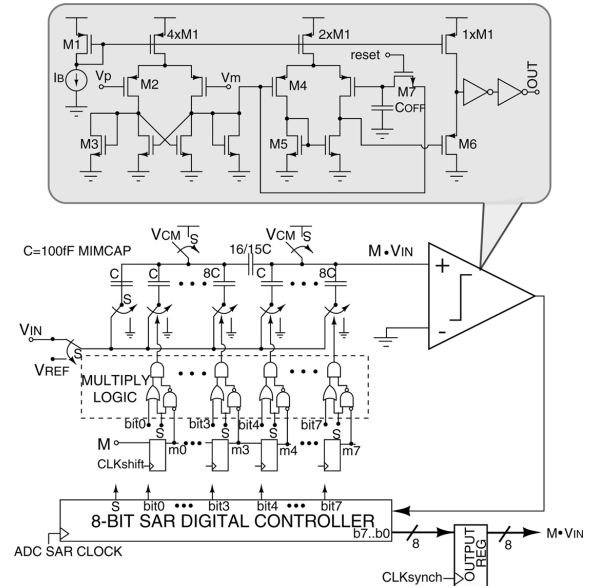


Fig. 8. Schematic of the in-channel multiplying SAR ADC and comparator.

C. Multiplying SAR ADC

Each channel in the 8×8 array has an 8-bit ADC to provide the most power-efficient and scalable architecture. The in-channel architecture relaxes the settling limitations of the neural recording amplifier and maintains a fixed sample rate per ADC. As introduced in Section II, each channel can be configured in one of the two modes of operation: raw data analog-to-digital conversion, and FIR filtering which is implemented as shown in Fig. 3(c). The in-channel ADC is an 8-bit capacitive charge redistribution SAR ADC. The same ADC circuits are reused in both modes. In raw data analog-to-digital conversion mode, the output of the neural amplifier is sent directly to the ADC. The FIR filtering mode requires the ADC to perform analog-digital multiplication as part of the conversion cycle. The successive approximation register (SAR) ADC

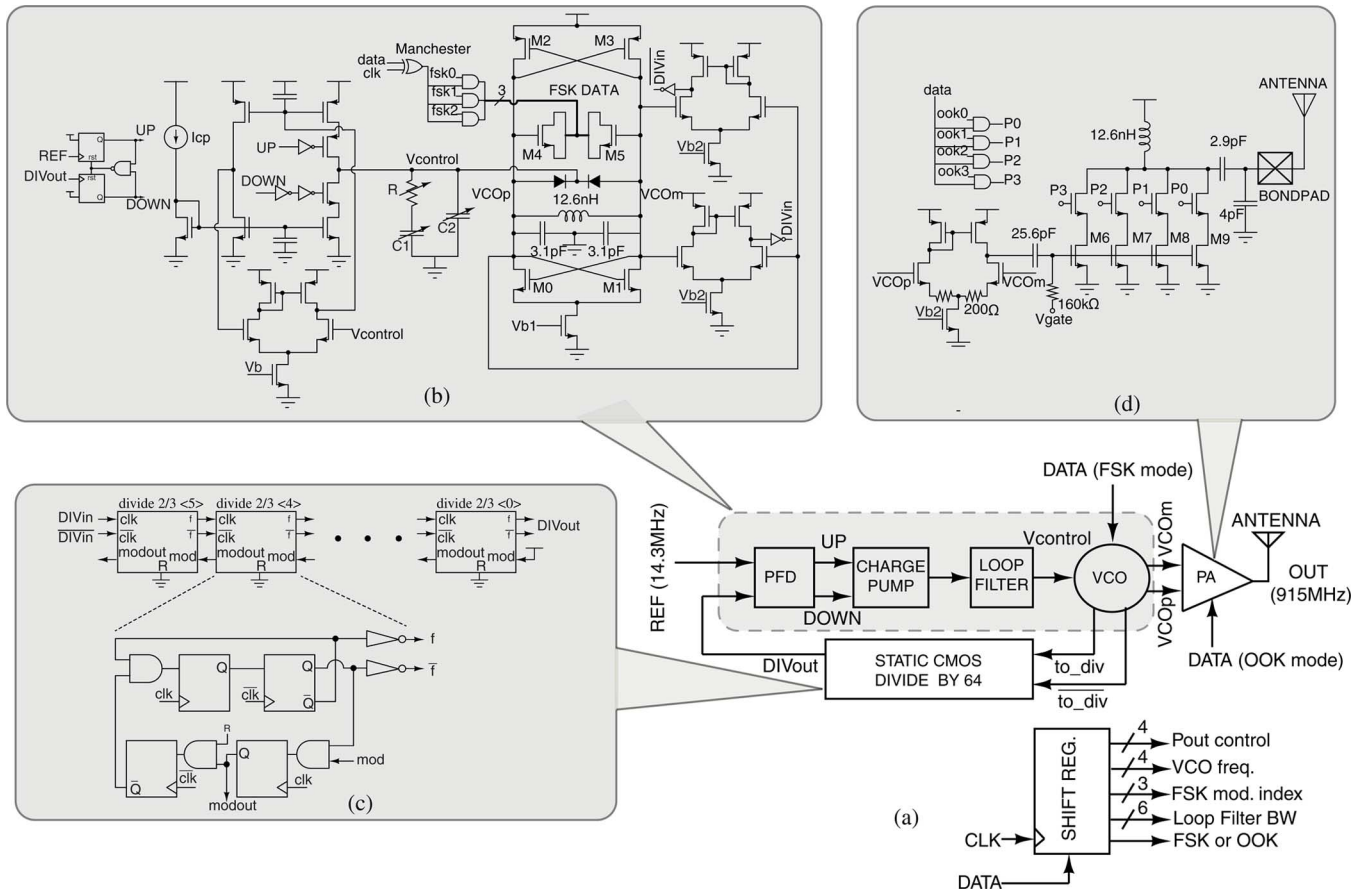


Fig. 9. (a) Block diagram of the fully integrated FSK/OOK wireless transmitter. (b) Schematic of the phase-frequency detector, charge pump and loop filter. (c) Schematic of the static-CMOS divide by 64. (d) Schematic of the output driver and power amplifier.

architecture can be modified to implement such computation with a small area and power overhead.

Analog multiplication within the ADC is introduced by modifying the digital SAR logic to perform multiplication during the sampling phase as shown in Fig. 7(a). During the sampling phase, the capacitors in the array are disabled or enabled which is equivalent to performing a multiplication by 0 and 1, respectively. The hold phase is similar to that in a conventional SAR ADC as shown in Fig. 7(b). Selective sampling to perform FIR filtering was implemented by utilizing multiple sampling cycles and a duplicate capacitor array to perform the SAR conversion [22]. The approach described in [22] requires additional area for the duplicate capacitor array and is unable to compute with negative FIR filter coefficients that are required for bandpass and highpass FIR filtering.

The SAR ADC architecture is shown in Fig. 8 and utilizes a split-capacitor array to minimize area and power dissipation. Each unit capacitor is implemented using a (metal-insulator-metal) MIM capacitor with a unit size of 100 fF. The split-capacitor value of 70 fF was determined through post-layout simulations. The comparator shown in Fig. 8 utilizes two stages with offset correction followed by a level-shifter and digital buffers. The ADC has an input range of 0.6 V and operates from a 1.2 V supply. Transistor sizes are listed in Table I.

The ADC mixed-signal multiplication requires only a few extra digital gates in the SAR logic, as shown in Fig. 8. The bits (bit0, bit1, ..., bit7) are the outputs from the conventional SAR digital controller logic. Multiplication coefficients (m_0, m_1, \dots, m_7) are loaded into an in-channel shift register. In the raw data analog-to-digital conversion mode, all the multiplication bits are set to high. In the FIR mode they are programmed to the value of the binary bits of the coefficient M . During the sample phase ($S = 1$), each bit at the output of the multiplication logic as shown in Fig. 8 represents a one-bit binary multiplication by 0 or 1. After the sampling phase ($S = 0$), the ADC operates as a conventional SAR ADC, logically equivalent to the charge-sharing switches being controlled by bits (bit0, bit1, ..., bit7). An output register synchronizes the ADC output data. Two sign coefficients (not shown) are also programmed to implement two's complement multiplication. The outputs are sent to the add-and-delay logic of the FIR filter, as shown in Fig. 3(c). The ADC dissipates $1.8 \mu\text{W}$ at 57 kS/s from a 1.2 V supply.

D. Fully Integrated 915 MHz FSK/OOK Transmitter

The digital data are serialized and encoded on-chip and transmitted wirelessly using either on-off keying (OOK) or frequency-shift keying (FSK) modulation at up to 1.5 Mb/s.

Each data packet is 16-bit, consisting of 10 bits of digitized neural data and a 6-bit channel address. This results in sending 64 channels of FIR-filtered neural data at a data rate of 1.5 kS/s per channel or at higher data rates on fewer channels. The closed-loop PLL transmitter prevents the VCO frequency from drifting allowing for a robust wireless channel without the addition of any off-chip passive components. The full wireless transmitter schematic is shown in Fig. 9(a). The output power (4 bits), VCO center frequency (4 bits), FSK modulation index (3 bits), PLL loop filter bandwidth (6 bits) and modulation type (1 bit) are programmed by loading an on-chip shift register.

1) *PFD, Charge Pump, Loop Filter and VCO*: The schematics of the phase-frequency divider (PFD), charge pump and loop filter are shown in Fig. 9(b). The PFD is implemented using a conventional three-state digital circuit [23]. The charge pump provides a current of 10 μ A and uses a regulated current mirror to minimize mismatch in the current sources [24]. Thick-oxide devices are used at the output to maximize the output impedance. The on-chip programmable RC loop filter has 3-bit tuning for both the capacitors and the resistor to allow for various PLL bandwidths and 50 degree phase margin in the PLL loop. The capacitor C1 can be programmed from 50 pF to 200 pF, C2 from 2.5 pF to 10 pF, and R from 25 k Ω to 200 k Ω . For FSK modulation, the bandwidth of the PLL was set to 50 kHz.

The voltage-controlled oscillator (VCO) was implemented using a cross-coupled architecture [25] with a 12.6 nH on-chip spiral inductor in the thick copper top-level metal. A large varactor implemented using a P+/N-junction diode was connected to the control voltage of the VCO to lock the PLL to 916.3 MHz. Additional programmable MIM capacitors (labeled as 3.1 pF in Fig. 9) were added to the tank to allow 3-bit binary tuning of the VCO center frequency to account for process variation. Two OTA buffers and digital inverters within the PLL loop convert the differential VCO output to a rail-to-rail level that is sent to the frequency divider. The differential VCO output (VCOm and VCOp) is sent to the power amplifier.

To prevent low frequency signals in the data to be filtered out by the PLL, the data is modulated with a clock operating at twice the data rate to implement Manchester-encoded FSK. The Manchester-encoded data is connected to the smaller NMOS VCO varactors as shown in Fig. 9(b). They consist of binary-weighted transistors M4, M5 and have 3-bit programming to adjust the FSK modulation index. The bandwidth of the PLL must be significantly lower than the data bit-rate to prevent the data from being filtered out by the PLL [26]. Transistor sizes for the VCO are shown in Table II.

2) *Frequency Divider and Power Amplifier*: The VCO output frequency is divided by 64 and the output of the divider is then fed back to the PFD. As shown in Fig. 9(c), the divider uses six cascaded divide-by-2/3 stages. The division ratio of each stage is set to 2 which locks the division ratio of the six cascaded dividers to 64. Static CMOS logic is used operating at up to 1.5 GHz in the slowest corner (in post-layout simulation), allowing for enough margin to function with the supply voltages as low as 0.8 V (experimentally confirmed).

TABLE II
TRANSISTOR SIZES OF THE VCO AND POWER AMPLIFIER

Transistor	W/L (μ m)
$M_{0,1}$	$15 \times 2/0.12$
$M_{2,3}$	$45 \times 2/0.12$
$M_{4,5}$	3T binary weighted bank, $(2, 4, 8) \times 2.5/0.12$
M_6	$40 \times 2/0.12$
M_7	$20 \times 2/0.12$
M_8	$10 \times 2/0.12$
M_9	$6 \times 2/0.12$

The differential output of the VCO is buffered by an OTA with resistive degeneration and sent to the power amplifier as shown in Fig. 9(d). The interface between the VCO buffer and the power amplifier is AC-coupled which allows the input of the power amplifier to be adjusted for class-A or AB operation. More power-efficient power amplifiers such as class-D, E or F were not selected as they require at least one extra inductor and thus significantly more area. Also these power amplifiers require full scale rail-to-rail operation for maximum power efficiency and high-Q inductors. In this case, the output power exceeds the requirements of an implanted wireless transmitter and the Q-factor of the inductors in this technology degrades at 915 MHz. The PLL also dissipates nearly 50% of the total transmitter power dissipation. With these issues, the extra area and complexity overhead of implementing a more power-efficient power amplifier would yield small overall benefit.

The power amplifier utilizes a 12.6 nH on-chip spiral inductor and a capacitive matching network to match to a 50-Ohm antenna. The output transistor size is programmed by enabling or disabling output transistor fingers with binary weighted widths through the cascode transistors by signals P_0 to P_3 . This allows the output power to be adjusted from -20 dBm to 0 dBm in 16 levels in FSK mode. For OOK modulation, the PLL is locked to the carrier frequency and the cascode transistors of the power amplifier are turned on or off. For OOK modulation, the PLL bandwidth can be made larger as it does not have to be limited as in the FSK mode. Transistor sizes of the power amplifier are listed in Table II.

IV. EXPERIMENTAL RESULTS

A. Analog Front-End

The experimentally measured amplitude frequency response and the input referred noise of the neural recording channel are shown in Fig. 10. Fig. 10(a) shows the high-pass corner frequency being adjusted from approximately 0.1 Hz to 1 Hz by programming the bias current of the source follower and adjusting the V_{GS} of M3 and M4 in Fig. 5 (top, right). Fig. 10(b) shows the frequency response of eight different channels across the chip showing a voltage gain spread between 53.3 dB and 54 dB. Fig. 10(c) shows the experimentally measured input-referred noise from eight different channels across the chip. The integrated noise between 10 Hz and 5 kHz is between

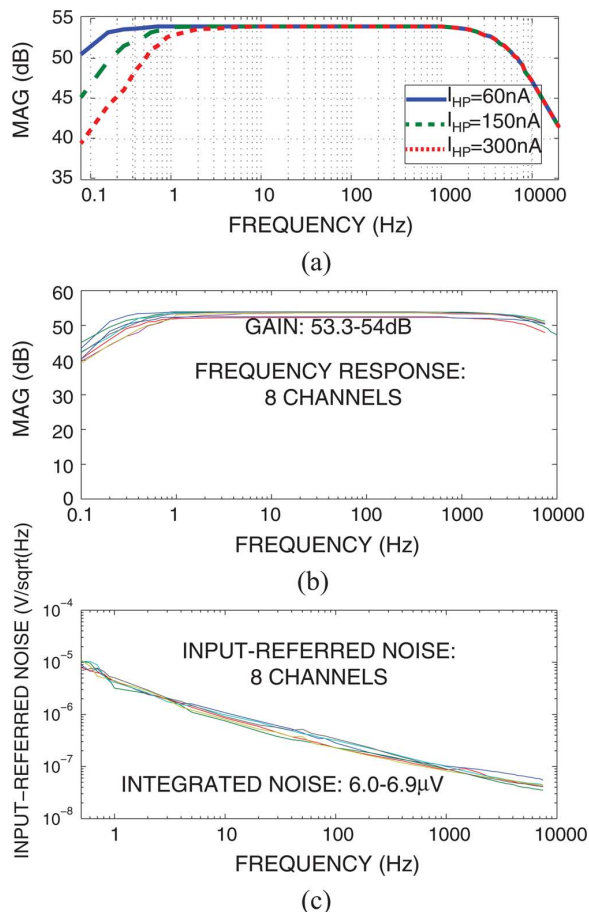


Fig. 10. Experimentally measured (a) amplitude response of the analog front-end showing tuneability of the high-pass pole (by varying source follower bias current, I_{HP}), (b) frequency response of eight different channels and (c) input-referred noise of eight different channels.

$6.0 \mu\text{V}_{rms}$ and $6.9 \mu\text{V}_{rms}$, resulting in an NEF of approximately 7.2. The experimentally measured common-mode rejection ratio (CMRR) across eight channels between 1 Hz and 1 kHz is at least 75 dB.

The THD was measured with an amplifier input amplitude of 1.4 mV (output of 0.7 V) for different input frequencies as shown in Fig. 11(a). A distortion of approximately 0.27% (-51.3 dB) at frequencies above 100 Hz was observed and a worst-case distortion of 3.2% (-29.9 dB) at 0.2 Hz. Tuneability of the high-pass pole is shown in Fig. 11(b) for two different neural recording amplifiers. The source follower current, I_{HP} , was set to 25 nA, 50 nA and 125 nA. The 3 dB high-pass cutoff frequencies between the two channels are in close agreement. The proposed feedback element yielded up to a 14 dB improvement in linearity at low frequencies as compared to the conventional pseudoresistor feedback [6]. As shown in the simulation result of Fig. 6(a) and (b) the high-pass pole in the conventional case changes significantly with output voltage amplitude. Experimentally, two PMOS devices can be activated on-chip in the feedback of the neural recording amplifier (included on the same chip for comparison purposes), and the proposed feedback element can be disabled.

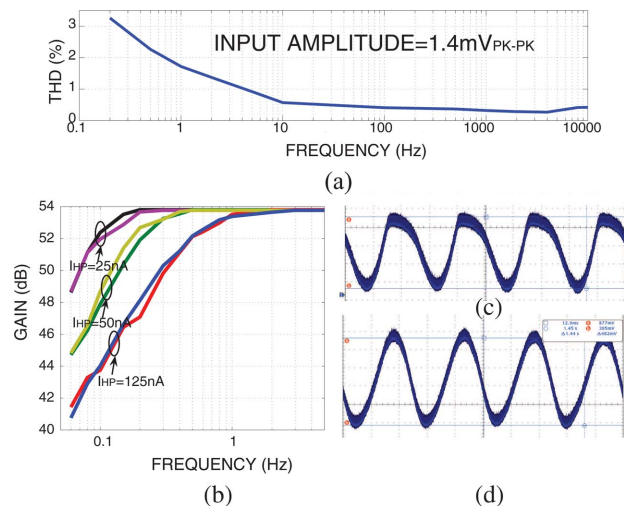


Fig. 11. (a) Experimentally measured THD of the analog front-end. (b) Experimentally measured high-pass filter frequency response for three different values of I_{HP} on two different channels on the chip. Experimentally measured output waveforms for a 1 mV_{pk-pk} 1 Hz sinusoid input comparing (c) conventional and (d) proposed feedback elements performance.

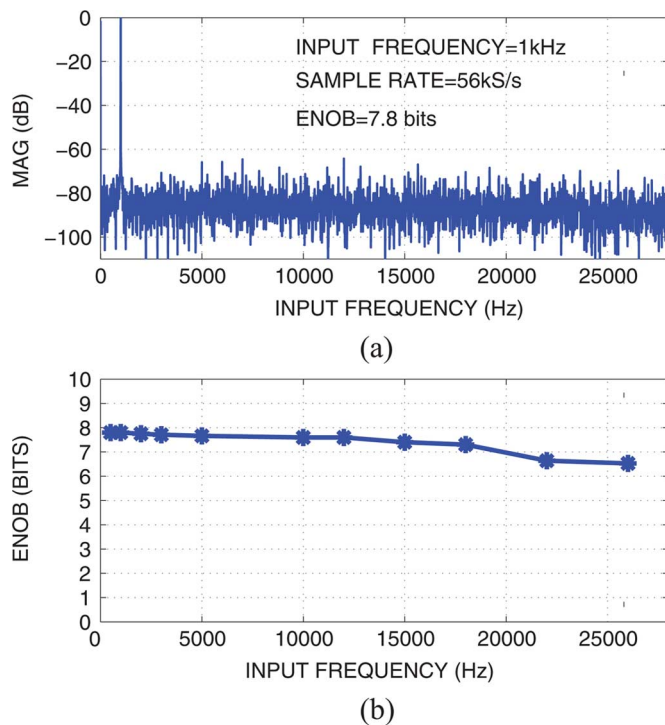


Fig. 12. (a) Experimentally measured FFT of an in-channel ADC output for 1 kHz sinusoid input at 54 kS/s. (b) Experimentally measured ENOB versus input frequency for an in-channel ADC.

The high-pass pole was set to the same frequency in both cases and the THD was experimentally measured for both cases. This linearity improvement is also visible in the time domain as shown in Fig. 11(c), (d). Fig. 11(c) shows the distorted output of the neural amplifier at a frequency of 1 Hz when utilizing the conventional feedback element. The less distorted output of the neural amplifier with the implemented feedback element is shown in Fig. 11(d).

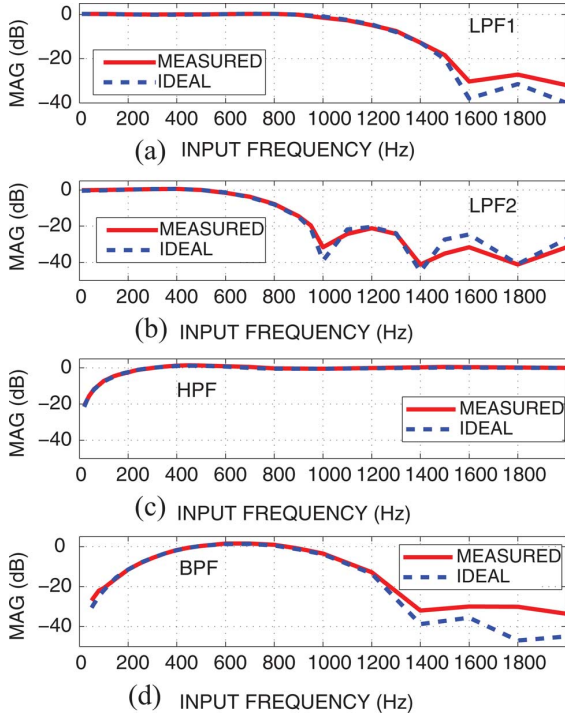


Fig. 13. Ideal and experimentally measured frequency responses of various programmable FIR filter configurations at 7.1 kSps.

B. ADC and Mixed-Signal FIR Filter

The experimentally measured ADC performance is shown in Fig. 12(a) and (b) with an ENOB of 7.8 and close to 7 bits over the full Nyquist bandwidth when sampled at 56 kS/s. The performance was consistent across all on-chip ADCs. The figure-of-merit of the ADC is 140 fJ/conversion-step.

Four different 16-tap FIR filter configurations were programmed on-chip and clocked at 7.1 kS/s (two different low-pass, one high-pass, and one band-pass filter). The results shown in Figs. 13(a)through(d) demonstrate a good match between the experimental result and the ideal filter response in Matlab. Two different FIR filters with their frequency responses shown in Fig. 14(a) were programmed on two different channels. Simultaneously, one channel had a 200 Hz sinusoid input and the other channel had a 500 Hz sinusoid input, both with 90% full-scale amplitude and a DC offset of 0.6 V. The digitized output of the two different channels is shown in Fig. 14(b). The high-pass FIR filter has the DC offset filtered out and has 2 dB attenuation, and the lowpass FIR filter shows 10 dB attenuation.

The FFT of a FIR filter output (programmed as a low-pass filter) sampled at 7.2 kS/s is shown in Fig. 15(a). It yields an SNDR of 46.5 dB and an SFDR of 56.9 dB. Both the SNDR for the stand-alone FIR filter and the SNDR for the FIR filter including the analog front-end is shown in Fig. 15(b). The SNDR for different input amplitude levels for a 100 Hz sinusoid is shown for the two cases. A 6 dB drop in SNDR (46.5 dB versus 40 dB) is observed when the analog front-end is utilized due to the additional in-band flicker noise, thermal noise and distortion of the amplifier. The gain of the amplifier was set to 470 V/V

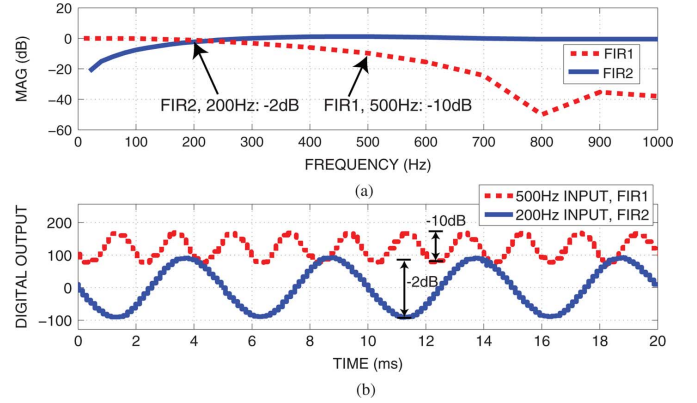


Fig. 14. (a) Two FIR filter frequency responses, FIR1 and FIR2 that are programmed in different channels on the chip. (b) The experimentally measured output of the two FIR filters with 200 Hz (FIR2) and 500 Hz (FIR1) sinusoidal inputs with an amplitude of 90% of the full-scale and sampled at 7.1 kSps.

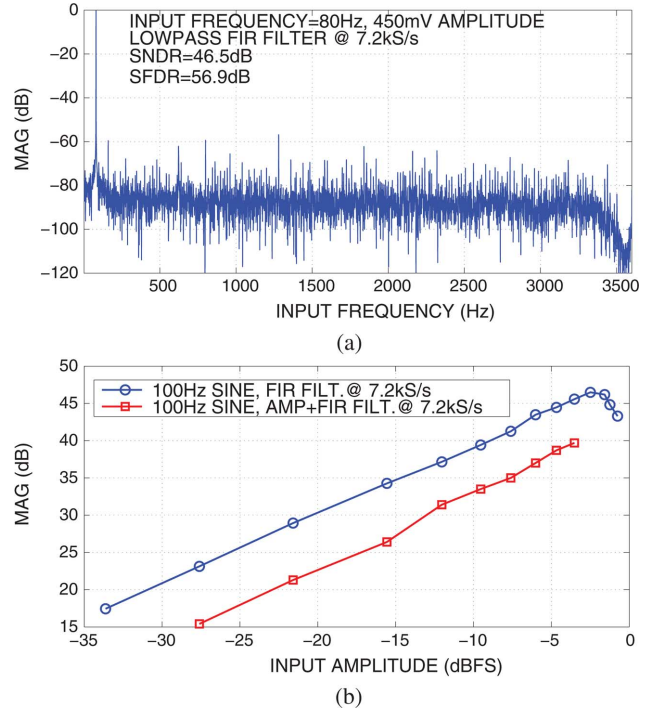


Fig. 15. (a) Experimentally measured output spectrum of the FIR filter. (b) Experimentally measured SNDR versus input amplitude with a 100 Hz sinusoid input to the FIR filter and to the FIR filter including the analog front-end.

and the input range of the ADC is 0.6 V. For an input-referred noise of 6.0–6.7 μV_{rms} (depending on channel) and a gain of 470 V/V this yields an SNR of approximately 40 dB.

A comparison of the mixed-signal FIR filter with previously published 12–16 tap analog and digital FIR filters with 7–8 bit resolution is given in Table III. The area-optimized digital FIR filters [27] implemented in a 90nm CMOS technology utilize the distributed arithmetic or look-up table implementations to reduce the area of the FIR filter. This approach yields an area much smaller than conventional FIR filters using digital multipliers [27]. The analog FIR filters [28] and [29] require more area than the digital approaches in [27] but include a built-in ADC. The

TABLE III
COMPARISON OF PUBLISHED FIR FILTERS

Reference	FIR Filter Type	Number of Taps	Resolution (bits)	CMOS Technology (nm)	Area (mm ²)
[27] (no ADC)	Digital LUT	16	8	90	0.033
[27] (no ADC)	Digital DA	16	8	90	0.04
[29] (includes ADC)	Analog	16	7	350	0.13
[32] (no ADC)	Analog	12	7	130	0.68
[28] (includes ADC)	Analog	16	8	45	0.14
This Work (no ADC)	Mixed	16	8	130	0.02
This Work (includes ADC)	Mixed	16	8	130	0.04

FIR filter approach covered in this paper has an overall equivalent area as the optimized digital approaches in [27], but this work also includes an ADC and is implemented in an older technology node.

Analog filter implementations utilizing switched capacitor filtering and Gm-based filtering [30], [31] for neural recording interfaces have also been reported. The switched capacitor bandpass filtering implementation [31] requires 10.8 μ W per channel and 2.8 mm² of silicon area to implement a single recording amplifier and four bandpass filters in 0.13 μ m CMOS without an integrated ADC. The tuning is performed by varying the sample rate and the capacitor ratios. The Gm-based epileptic filter reported in [30] is sensitive to the transconductance value and requires large on-chip passives. Tuning is achieved by varying the transconductance of the Gm cells and different filtering implementations (low-pass, high-pass and band-pass) would require extra overhead. A single recording channel and bandpass filter in 0.6 μ m CMOS utilizes 0.45 mm² and dissipates 7 μ W without an integrated ADC. The mixed-signal FIR filter presented here utilizes 0.04 mm² (including an on-chip ADC) and dissipates 14.5 μ W (includes amplifier, ADC and FIR filter) at 7.2 kS/s. The filter response can easily be modified by programming the on-chip shift registers to implement all-pass, band-pass, low-pass or any general-purpose 16-tap FIR filter implementation. To achieve higher selectivity filtering at lower frequency (such as in the alpha, beta and gamma bands), the system sample rate can be lowered and the FIR filter power dissipation linearly decreases. Scaling the FIR filters for a center frequency of 30 Hz requires lowering the sample rate to 500 S/s. In this case, the experimentally measured power dissipation (amplifier, ADC and FIR filter) is decreased from 14.5 μ W to 8 μ W per channel. Furthermore for higher selectivity, the FIR filter architecture scales to higher taps (up to 128) by only increasing the number of digital adders and registers reasonably impacting the sample rate, area and power dissipation as shown in Figs. 4(a), (b) and (c), respectively and discussed in Section III-A.

C. 915 MHz FSK/OOK Transmitter

Experimental results for the wireless transmitter are shown in Fig. 16. Fig. 16(a) shows the output spectrum of the FSK transmitter with 1.2 Mbps Manchester-encoded input data. Fig. 16(b) shows transmitted and received data at a distance of 1 m. Fig. 16(c) shows OOK-modulated data on an oscilloscope and Fig. 16(d) shows transmitted and received OOK data

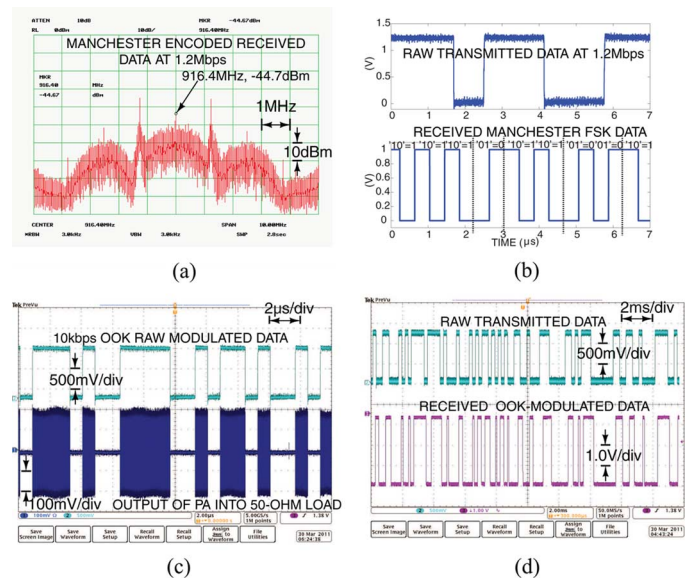


Fig. 16. Experimentally measured (a) spectrum of FSK-modulated data at a 1 m distance, (b) transmitted and received data from 1 m distance at 1.2 Mbps using FSK modulation, (c) OOK-modulated data into 50 Ω termination resistor and (d) transmitted and received data from a 1 m distance at 10 kb/s using OOK modulation.

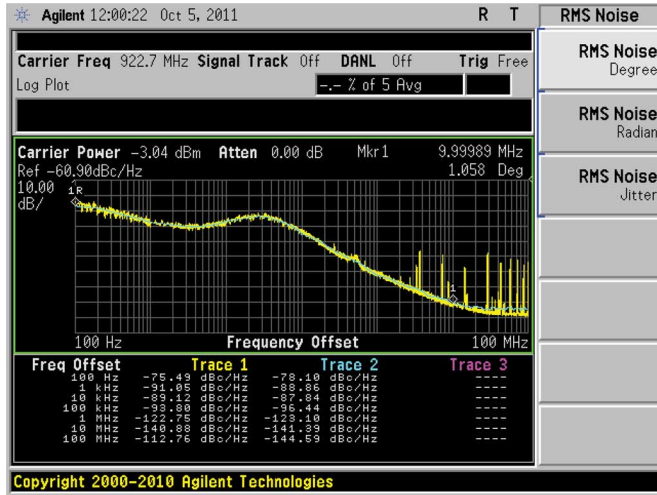
TABLE IV
COMPARISON OF ISM-BAND FSK TRANSMITTERS

Spec.	[33]	[34]	[35]	[36]	THIS WORK
CMOS Tech. (μ m)	0.18	0.18	0.13	0.25	0.13
Supply (V)	1.5	1.8	1.5	1.3	1.2
Frequency (MHz)	402	900	915	433	915
Data Rate (Mb/s)	1.5	1.0	0.05	0.1	1.5
Phase Noise @10kHz (dBc/Hz)	-88.6	-	-	-75	-89.1
Phase Noise @100kHz (dBc/Hz)	-85.8	-	-97	-	-93.8
Phase Noise @1MHz (dBc/Hz)	-110.1	-107.9	-	-	-122.8
Max. Output Power (dBm)	-9	-14.5	-6	0	0
DC Power (mW)	19.5	20.7	2.7	5.0	6.6
Area (mm ²)	1.6	3.0	1.5	4.8	0.42

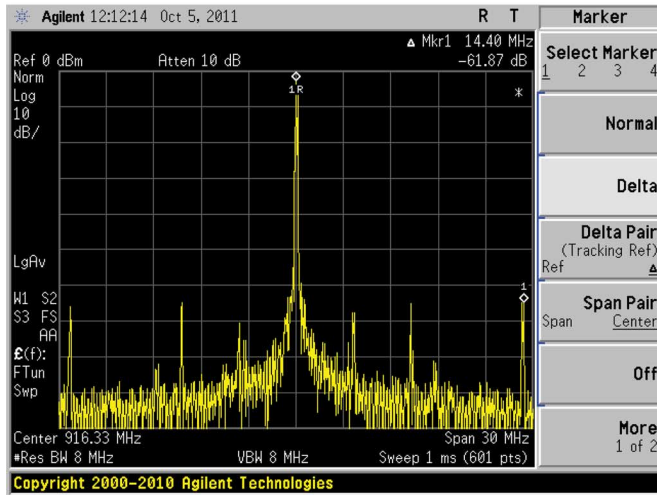
from a distance of 1 m. The wireless link demonstrated robust performance at distances up to 10 m.

The phase noise and output spectrum of the full transmitter at the output of the power amplifier with a 50 Ohm load are shown in Fig. 17(a) and (b) respectively. The spectrum analyzer was the Agilent E4448A. The phase noise at 1 MHz offset is -123 dBc/Hz, the integrated jitter over a 10 MHz bandwidth is 1.06 degrees and the reference spur (14.33 MHz) is -62 dB below the fundamental.

For wireless testing, the receiver was the RFM 868 MHz to 960 MHz TRC103 transceiver. The transmitter used a quarter-wave 915 MHz antenna and the receiver used a



(a)



(b)

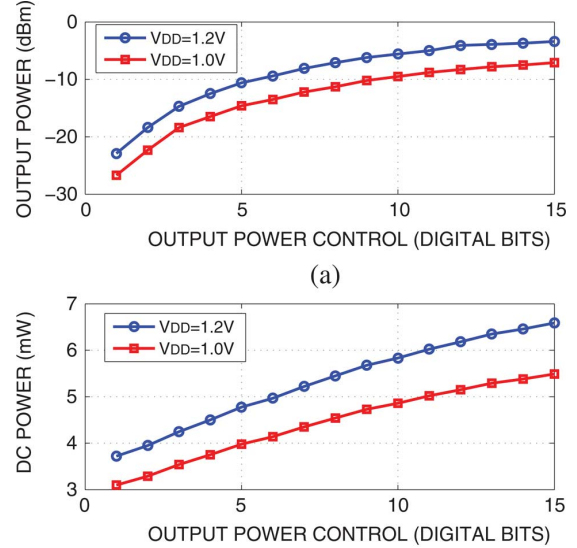
Fig. 17. (a) Experimentally measured phase noise of the RF transmitter. (b) Experimentally measured output spectrum showing the reference spur of the RF transmitter.

half-wave 915 MHz antenna, both connected through SMA connections. The full transmitter dissipates 3.7 mW and 6.6 mW in FSK-mode for an output power of -20 dBm and 0 dBm, respectively and 5 mW for 0 dBm OOK modulation. The experimentally measured output power and DC power of the transmitter with a 1.0 V and 1.2 V supply for different power amplifier program settings are shown in Fig. 18(a) and (b). The experimentally measured power efficiency of the full RF transmitter with 0 dBm output power is 18% and 24% when operating with FSK and OOK modulation, respectively. This includes the power amplifier, the VCO, the PLL circuits and additional clocking and serialization circuits.

A comparison to other ISM-band FSK RF transmitters is given in Table IV.

D. Application Example: Noise Suppression and Spike Detection

The full neural recording channel with the FIR filter programmed to suppress high frequency noise was experimentally



(a)

(b)

Fig. 18. Experimentally measured (a) TX output power and (b) DC power for the RF TX when connected to a 50Ω termination resistance for different power-levels.

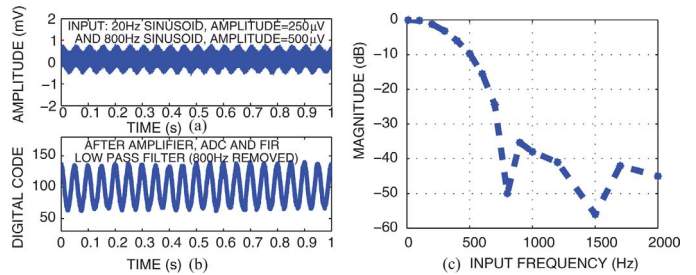


Fig. 19. (a), (b) Example of experimentally measured signal band separation using full recording channel (with LP FIR filter). (c) Experimentally measured frequency response of the programmable FIR filter at 7.1 kSps used to obtain the result in (b).

characterized as shown in Figs. 19(a) and (b). In Fig. 19(a), the input to the amplifier consists of a 20 Hz sinusoid with an amplitude of $250 \mu\text{V}$ and an additional high frequency noise at 800 Hz with a larger amplitude of $500 \mu\text{V}$. The FIR filter was programmed for low-pass filtering as shown in Fig. 19(c). It removes the 800 Hz interference, resulting in the output depicted in Fig. 19(b) showing the amplified and FIR filtered 20 Hz signal.

The functionality of the analog front-end, ADC and FIR filters was verified with pre-recorded neural activity of epileptic seizure events. Seizure-like events were induced in an intact hippocampus from Wistar rats by immersing it in a low-Mg²⁺ solution. The signals were recorded with a conventional bench-top low-noise amplifier and then programmed onto an arbitrary waveform generator with the original signal as shown in Fig. 20(a). The input signal was then contaminated with 60 Hz interference with a much larger amplitude than that of the pre-recorded signal as shown in Fig. 20(b) and applied to one of the 64 channels on the chip. Threshold-based spike-detection for these two cases would yield a high false-positives rate. The FIR filter was programmed with the bandpass filter response

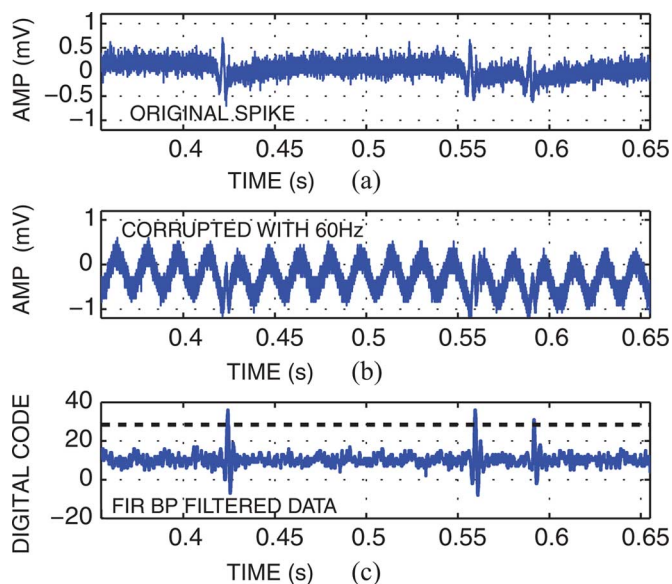


Fig. 20. Example of experimentally measured spike detection using full recording channel (with BP FIR filter).

shown in Fig. 13(d). Fig. 20(c) shows the output after the FIR filtering with the neural activity clearly visible and the 60 Hz interference removed resulting in threshold-based spike detection having fewer false positives (depicted with the dashed line).

E. Power Dissipation and Area Breakdown

The neural recording SoC dissipates 0.8 mW for the analog front-end, ADCs and biasing (includes all LNA, ADC, RF bias currents), 0.53 mW for the digital controller and the adders/registers to implement the FIR filters operating at a sampling rate of 7.1 kS/s. The RF transmitter dissipates 3.7 mW in FSK mode when operating the power amplifier with a -20 dBm output power. The total system power dissipation is 5.03 mW from a 1.2 V supply. When using a 1.0 V supply for the digital and RF transmitter, the total power dissipation is reduced to 4.17 mW at the expense of requiring a second supply voltage. The FIR filters can be used with additional logic to detect channels with little neural activity and the RF transmitter can be shut off to further reduce the power dissipation. In terms of the integration area, the 64-channel analog front-end and ADCs utilize the majority of the die area. The 64 FIR filters add only an additional 20% area overhead to the SoC.

A summary of the experimental results is given in Table V. A comparison with other wireless neural recording SoCs is given in Table VI. This work demonstrates the highest level of integration among recently published state-of-the-art designs by combining 64 recording channels, 64 16-tap FIR filters and a fully integrated closed-loop wireless transmitter without a significant compromise on area or power dissipation.

Future work includes an SOC with these improvements: 64 fully differential chopper-stabilized recording amplifiers with in-channel bandpass filtering, 64 multiplying SAR ADCs and FIR filters for I/Q separation, 64 neural stimulators, a tri-core

TABLE V
SUMMARY OF EXPERIMENTAL RESULTS

System:	
Technology	1P8M 0.13 μ m
Supply Voltage	1.2V
Die Dimensions	4.0mm \times 3.0mm
Area per Channel	300 μ m \times 300 μ m
Number of Recording Channels	64
On-Chip Memory	1kb
Power Dissipation	5.03mW
Recording Channel:	
Number of Recording Channels	64
Gain	54-60dB
Input-Referred Noise (10-5kHz)	6.5 μ V
Input-Referred Noise (1-100kHz)	20 μ V
CMRR	75dB
THD @ 1kHz, 0.7V _{pk-pk}	-51dB
Power Dissipation of LNA	4.5 μ W
NEF of LNA (5kHz)	7.2
NEF of LNA (100kHz)	5.3
ADC SNDR	48.5dB
ADC ENOB	7.8-bits
ADC Sample Rate	57kS/s
Power Dissipation of ADC	1.8 μ W
ADC Figure-of-Merit	140fJ/step
Power Diss. (LNA+ADC)	6.3 μ W/channel
Signal Processing:	
Number of FIR filters	64
FIR filter type	Symmetric 16-tap
Coefficient Resolution	8-bit signed
Output Resolution	12-bits
FIR SNDR	46.5dB
FIR SFDR	56.9dB
LNA+FIR SNDR	40dB
FIR Sample Rate (64-channels)	7.1kS/s
FIR Sample Rate (8-channels)	57kS/s
Power Diss. (LNA+ADC+FIR)	14.5 μ W/Channel
RF Transmitter:	
Carrier Frequency	915MHz
Reference Frequency	14.3MHz
Closed-loop Modulation	FSK and OOK
Data Rate	1.5Mbps
Phase Noise	-123dB/Hz @ 1MHz
Largest Spur	-62dB
Output Power	-20dBm-0dBm
DC Power	3.7mW to 6.6mW

CORDIC processor, 1 kB of memory and a UWB RF transmitter [37]. This SoC implements a neural vector analyzer and computes phase synchrony for seizure detection to trigger a biphasic current stimulator in closed-loop for seizure abortion.

F. In Vivo Neural Recording and FIR Filtering

The SoC was validated in on-line *in vivo* experiments in a population of four freely moving rats. Three depth electrodes were implanted into the hippocampus of each rat with two electrodes connected to the inputs of two channels of the neural recording SoC and one electrode acting as a reference electrode for the SoC. The amplifier was programmed for a bandwidth of 0.1 Hz to 5 kHz. The FIR filter was programmed to implement a bandpass response between 5 Hz and 300 Hz to further remove low frequency drift and high frequency noise. The pharmacological agent gamma-butyrolactone (GBL) was used to invoke a non-convulsive epileptic seizure in a rat. Before injecting the rat with the drug, no seizure activity is recorded as shown in Fig. 21(a). Ten minutes after injecting the rat with GBL, seizure

TABLE VI
 INTEGRATED WIRELESS NEURAL RECORDING SoCs

Spec.	[2]	[3]	[13]	[16]	[9]	[5]	[4]	[15]	THIS WORK
Power Diss. (mW)	13.5	17.2	7.05	6.0	6.5	0.375	0.27	0.5	5.03
CMOS Tech. (μm)	0.5	0.35	0.5	0.35	0.13	0.35	0.18	0.13	0.13
Area (mm^2)	27.3	8.4	16.3	63.4	25	10.9	2.7	2.5	12
Supply (V)	3.3	3.0	3.0	3.3	1.2	3.0	1.8	1.0	1.2
# of Recording Chan.	100	16	32	128	96	4	8	1	64
Power/channel (μW)	38	9	75	11	-	32.8	9	75	6.3 (LNA+ADC) 14.5 (LNA+ADC+FIR)
Gain (dB)	60	60	68-78	57-60	-	51.8-65.7	-	38.3	54-60
Noise (μV_{rms})	5.1	3.1	9.3	4.9	2.2	3.1	-	2.0	6.5 (10Hz-5kHz)
ADC	1xSAR	1xSAR	PWM	1xSAR	96xSAR	1xSAR	1xLog.	1xSAR	64xSAR
ADC Resolution (bits)	9b	8b	N/A	6-9b	10b	10b	8b	8b	8b
Signal Processing	Spike	Spike	None	Spike	None	1xIIR	1x22tap-FIR	None	64x16tap-FIR
Programmable	No	No	No	Yes	No	Yes	Yes	No	Yes
RF Transmitter	Yes	Yes	Yes	Yes	No	Yes	No	Yes	Yes
RF Carrier (GHz)	0.433	0.433	0.915	3.1	-	0.433	-	0.450	0.915
Modulation	FSK	FSK	FSK/OOK	UWB	-	FSK	-	FSK	FSK/OOK
Data rate (Mb/s)	0.330	1.25	0.708	90	-	N/A	-	0.100	1.5
PLL	No	Yes	No	No	-	No	-	Yes	Yes
Fully Int. TX	No	No	No	Yes	-	No	-	No	Yes
RF P_{out} (dBm)	N/A	0	-22	N/A	-	N/A	-	-16	-20 to 0
RF P_{DC} (mW)	4.0	16.6	3.3	1.6	-	0.2	-	0.4	3.7 to 6.6

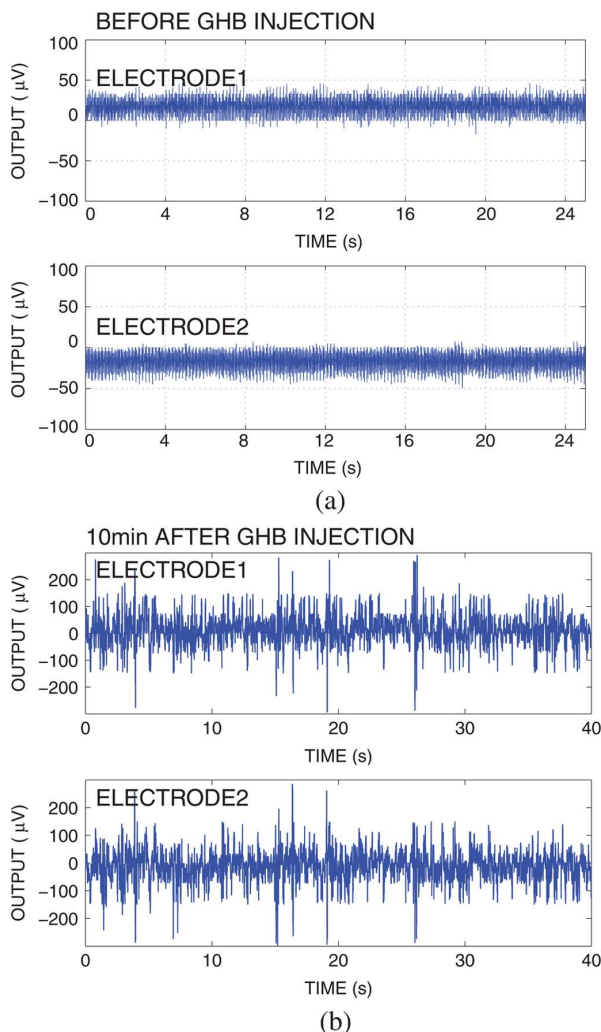


Fig. 21. (a) Online on-chip in vivo recordings before seizure activity triggered by GBL injection, recorded using on-chip BP FIR filter. (b) Online on-chip in vivo recording showing seizure activity after GBL injection recorded using on-chip BP FIR filter.

activity is clearly recorded on two channels in Fig. 21(b) as expected for this epilepsy model.

V. CONCLUSION

A 0.13 μm CMOS wireless neural recording SoC is presented. The die integrates 64 fully differential recording amplifiers with 64 SAR ADCs modified to perform in-channel multiplication. This implements 64 programmable 16-tap mixed-signal FIR filters to perform versatile signal filtering in each channel. A fully integrated PLL-based FSK/OOK transmitter wirelessly sends the digitized neural recorded data at up to 1.5 Mb/s with an output power as high as 0 dBm. The total power dissipation is 5.1 mW from a 1.2 V supply. The system was also characterized in vivo. Compared with previous neural recording SoCs, the presented design integrates a large number of recording channels, signal processing and a closed-loop wireless transmitter without a significant compromise on area or power dissipation. This makes the presented SoC a viable option for an envisioned chronically implantable brain activity monitoring device.

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