64-Channel UWB Wireless Neural Vector Analyzer SOC With a Closed-Loop Phase Synchrony-Triggered Neurostimulator

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***Abstract*—An ultra wideband (UWB) 64-channel responsive neural stimulator system-on-chip (SoC) is presented. It demonstrates the first on-chip neural vector analyzer capable of wirelessly monitoring magnitude, phase and phase synchronization of neural signals. In a closed-loop, abnormal phase synchrony triggers the programmable-waveform biphasic current-mode neural stimulator. To implement these functionalities, the SoC integrates 64 neural recording amplifiers with tunable switched-capacitor (SC) bandpass filters, 64 multiplying 8-bit SAR ADCs, 64 programmable 16-tap FIR filters, a tri-core CORDIC processor, 64 biphasic current stimulation channels, and a 3.1–10.6 GHz UWB wireless transmitter onto a 4 mm × 3 mm 0.13 µm CMOS die. To minimize both the area and power dissipation of the SoC, the SAR ADC is re-used as a multiplier for FIR filtering and as a DAC and duty cycle controller for the biphasic neural stimulator. The SoC has been validated in the early detection and abortion of seizures in freely moving rodents on-line and in early seizure detection in humans off-line.**

***Index Terms*—Closed-loop, closed-loop SoC, early seizure detection, implantable wireless SoC, mixed-signal FIR filters, neural recording, neural stimulation, neural vector analyzer, phase synchronization.**

I. Introduction

NEUROELECTRICAL activity in the brain generates electrophysiological signals in multiple frequency bands such as alpha (8–12 Hz), beta (13–30 Hz) and gamma (40–80 Hz). Through oscillations in these bands, information is communicated among various regions in the brain. These oscillations have been linked to a wide range of cognitive and perceptual processes including sleep states and memory [1]. Simple tasks, such as motor or sensory tasks also often require the coordination or synchronization of many brain areas [1].

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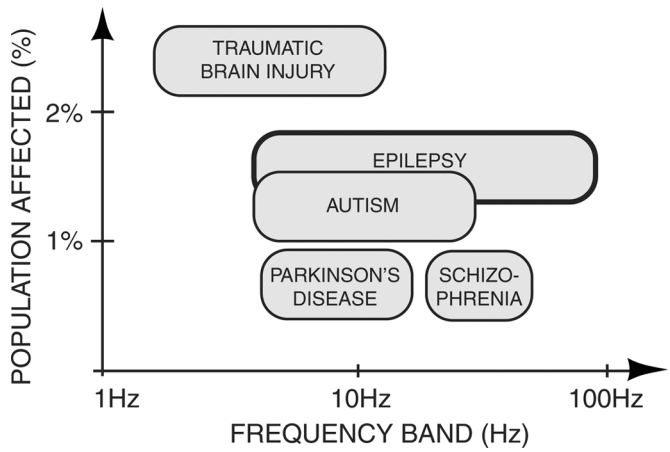

Fig. 1. Various neurological disorders and the frequency bands of the corresponding abnormal phase synchrony.

On the other hand, abnormal coordinated interactions in various regions of the brain are widely recognized as key indicators of pathological brain states in numerous neurological disorders such as epilepsy, schizophrenia, Parkinson's disease, autism and traumatic brain injury [2]. Fig. 1 outlines the frequency bands where abnormal phase synchrony is exhibited by various neurological disorders and the percentage of the population who suffer from each disease [3], [4]. Quantifying phase synchronization among neural oscillations in these frequency bands is a new and promising method for diagnostics, monitoring or treatment of such disorders [5]–[8].

For example, in epilepsy, fluctuations in phase synchrony in narrow frequency bands are among the best features used for early detection of seizures [9]. Detecting the seizure before it develops is critical in a closed-loop implantable device for automated seizure control. Closed-loop operation yields two major advantages. Firstly, the chances of aborting a seizure are much higher if responsive electrical stimulation takes place before one fully develops [9]. Secondly, closed-loop neural stimulators minimize the overall power dissipation of an implantable device. Neural stimulators must provide large biphasic currents to invoke a neural response and exhibit a much higher power dissipation than neural recording and signal processing units. By only triggering the neural stimulator when a seizure is detected, the power dissipation of a closed-loop implantable device can be significantly reduced. This lengthens the battery life and minimizes tissue damage resulting from the heat generated

by the neural stimulator. Thus, to improve the performance of a closed-loop implantable device, a phase synchronization estimation algorithm with high performance (e.g., high true-positive rate and low false-positive rate) is required to be implemented on an integrated circuit within the implant.

Integrated circuits for monitoring electrical activity of the nervous system typically record the brain activity through surface electroencephalography (EEG), electrocorticography (ECoG) or microelectrode arrays (MEA). Systems-on-chip (SoCs) with a large number of neural recording channels have been demonstrated [10]–[13]. As many as 100 or more recording sites in the brain can be monitored simultaneously. Through multiple recording channels coordinated synchronization between various regions of the brain can be monitored. To observe this phenomenon, an instrument known as a vector analyzer is required. It measures not only the magnitude, but also the phase of a signal for all frequencies within its band.

Typically, neural recording SoCs have extracted electrical information from neurons by recording voltages on electrodes over a broad frequency range in the neural spectrum [11], [13]–[20] including our previous work in [21]–[23] and [24]. More recently, researchers have also started performing neural recording and signal processing that extracts spectral information such as the magnitude or energy that exists in specific frequency bands [25] and [26], operating similarly to an AM radio receiver. The real-time processing of spectral energy bands can help establish a closed-loop mechanism. However, these implementations ignore information that exists in the phase of each signal and particularly in the phase difference between signals.

Conventionally, on-chip real-time signal processing is performed on each input independently. This yields no information on the correlation among inputs, ignoring the communication through oscillations that exist among various regions of the brain. Recording neural activity from two or more electrodes, located in various parts of the brain and then performing signal processing among these signals constitutes bivariate or multivariate signal processing, respectively. This offers more advanced algorithms for diagnostics, monitoring and treatment of neurological disorders. Computing the amount of phase synchronization that exists between two or more electrodes located in different regions of the brain is one such bivariate/multivariate technique. A signal processing SoC which computes the amount of phase synchronization between two or more neural inputs, has not yet been demonstrated.

A number of integrated circuits with other advanced signal processing algorithms operating in an open loop have been demonstrated. Our previous work [22] integrates 64 recording channels with 64 programmable finite impulse response (FIR) filters and utilizes multiplication within the ADC to overcome the area and power constraints of integrating 64 16-tap FIR filters. Neural recording SoCs with multiple channels and advanced signal processing to assist in seizure detection have been demonstrated [25], [27], [28]. A 0.18 μm eight-channel EEG acquisition SoC with an on-chip classification processor for seizure detection was reported in [28]. A 90 nm SoC which integrates a RISC processor, a FIR filter and other digital signal processing blocks with 16 neural recording channels was demonstrated in [27]. These previously published designs that utilize advanced signal processing [28], [27], [26], [25] operate in open-loop, have few recording channels and have no wireless communication capabilities.

SoCs with closed-loop operation have also been demonstrated which combine neural recording, neural stimulation and neural signal processing blocks on a single die [16], [14]. For the design in [16], the neural recording functionality has been limited to a few recording channels and the signal processing functionality has been limited to simple FIR filtering. The work presented in [14] demonstrates a bivariate closed-loop stimulator. It has a limited number of recording and stimulation channels (eight recording and eight stimulation channels) and the signal processing implements spike detection and not a high-efficacy seizure detection algorithm. The work demonstrated in [29] and our previous work in [21] and [24] integrate a large number of neural recording and neural stimulation channels. However, these systems lack signal processing required for high-efficacy closed-loop operation, such as neural stimulation triggered as a result of abnormal phase synchrony detection.

We present a 64-channel neural recording and 64-channel neural stimulation SoC that operates in a closed loop based on a high-efficacy signal processing algorithm. This paper extends on our earlier report in [30] and includes extensive treatment of circuit design techniques and additional experimental results. It is the first on-chip neural vector analyzer with the ability to process not only the magnitude, but also the phase of neural signals. It is also the first SoC to demonstrate real-time on-chip computation of the phase synchrony between neural signals.

The rest of the paper is organized as follows. Section II discusses the VLSI architecture of the 64-channel neural recording and stimulation SoC. Section III presents the circuit implementation of the key functional blocks in the SoC. Section IV presents electrical experimental results from the individual blocks and the full system. Section V presents *in vivo* on-line animal and off-line human results validating the SoC in epilepsy treatment.

II. System VLSI Architecture

A. Top-Level VLSI Architecture

The SoC consists of 64 neural recording and 64 neural stimulation channels to connect to a 64-electrode electrocorticography (ECoG) grid or a depth electrode array, both used routinely for presurgical epilepsy monitoring. Each channel is bidirectional and can be dynamically configured for recording or stimulation capabilities. A subset of these 64 channels can be selected for recording electrodes and another subset for lower impedance stimulation electrodes. Another functionality is to share the same electrodes for both recording and stimulation. In this case, low-impedance electrodes are used to both record neural activity from the brain (e.g., deeper areas of the brain) and real-time neural stimulation at the same location can be triggered by seizure detection on the same electrodes.

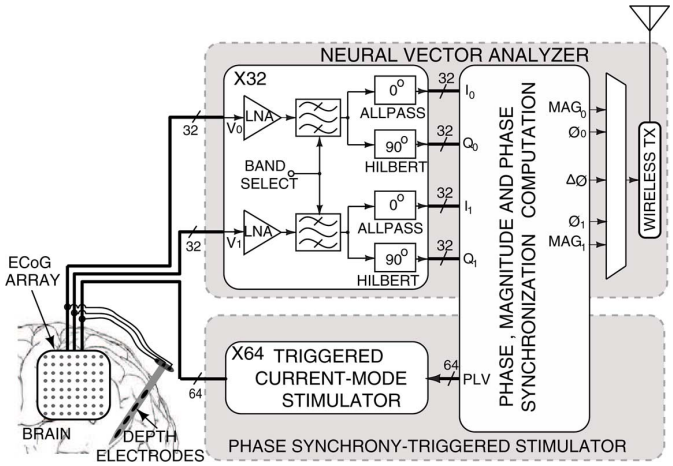

Fig. 2. Functional diagram of the SoC.

Each recording channel has a low-noise amplifier that amplifies signals in the full neural signal band (local field potentials (LFPs) and spikes) consisting of frequencies as low as 0.1 Hz and as high as 10 kHz and with signal amplitudes between 10 μV and a few mV. After amplification, there are two cascaded programmable band-pass filters in each channel. The first filter has a broad band (e.g., 0.1 Hz to approximately 10 kHz) and passes both LFPs and single/multiple unit discharge signals, as needed for raw data monitoring. The second filter is narrow-band (e.g., 3 Hz to 5 Hz) and passes only LFPs which are needed for phase synchrony computation. Higher frequency bands are used to extract spike information or to process magnitude information. For stimulation in order to control seizures in rat intractable epilepsy models, suitable stimulus signal specifications are as follows: frequency of 1 to 200 Hz; current of 0.1 to 1.2 mA; pulse width of 40 to 1000 μs; burst duration <5s; and number of bursts of 1 to 5.

The functional diagram of the SoC is depicted in Fig. 2. The loop consists of the neural vector analyzer in the feed-forward path and the phase synchrony-triggered neural stimulator in the feedback. Pairs of neural signals, V_0 and V_1, are amplified and then filtered within a specific pass-band to monitor the abnormal phase synchrony of interest in that band. The band of interest can be adjusted by programming the center frequency of the bandpass filter.

To monitor the phase synchrony, the in-phase (I) and quadrature-phase (Q) components are then computed by the allpass and Hilbert filters, respectively. The Hilbert filter introduces a 90 degree phase shift and a time delay, while the allpass filter introduces an equal time delay. This results in a 90 degree phase difference between the two components. These components comprise each neural signal, V_0 and V_1, as follows:

$$V_0 = Re(V_0) + jIm(V_0), \quad V_1 = Re(V_1) + jIm(V_1), \quad (1)$$

where $Re(\cdot)$ is the I component and $Im(\cdot)$ is the Q component.

The allpass and Hilbert filtering are conventionally performed over the full band of frequencies in the signal spectrum. In the proposed implementation, a narrow-band bandpass filter is employed before the Hilbert transform to isolate the narrow frequency band of interest where abnormal oscillations are monitored. This enables precise computation of the magnitude and phase at the narrow band center frequency. The algorithm details are given in [31].

These I and Q components are then used to compute the magnitude (MAG) and phase (ϕ) of the signals, and their pairwise phase differences $(\Delta\phi)$. The magnitude and instantaneous phase in the extracted frequency band are then computed as

$$|V_k| = \sqrt{Re(V_k)^2 + Im(V_k)^2}, \phi_k = \arctan\frac{Im(V_k)}{Re(V_k)} \quad (2)$$

where $k = 0, 1$. The vectored outputs are serially wirelessly transmitted. This implements the function of a wireless neural vector analyzer.

Phase locking value (PLV) is a common metric of phase synchrony and is computed in the feedback loop of the SoC. In epilepsy, seizure precursors are abnormally large fluctuations in PLV which can be detected by thresholding. The biphasic current-mode stimulator is triggered when the PLV indicates abnormal phase synchrony levels. In epilepsy this is done to abort an upcoming seizure. The hardware-efficient mean phase coherence algorithm [8] was utilized to compute PLV ranging between 0 and 1 as

$$\text{PLV} = \frac{1}{N}\sqrt{\left(\sum_{i=0}^{N-1} sin(\Delta\phi_i)\right)^2 + \left(\sum_{i=0}^{N-1} cos(\Delta\phi_i)\right)^2}, \quad (3)$$

where N is the length of the sample observation window and $\Delta\phi_i$ is the instantaneous phase difference between the i-th samples of the two signals.

1) Early Seizure Detector Preliminary Validation: Three different seizure detector methods were previously analyzed by us [31]. These are the magnitude, PLV and combined magnitude and PLV detectors. The magnitude detector is activated when the amplitudes of both input channels within a specific frequency band of interest increase above a programmed threshold. The PLV detector is triggered when the phase locking value, integrated over an adjustable period of time, drops below a certain threshold. The PLV detector is known to be an earlier precursor of a seizure compared to the magnitude detector. Typically, epileptic seizure onset in humans is characterized by a decrease in the phase locking value $(\text{PLV} < 0.1)$ and a subsequent increase in brain synchronization $(\text{PLV} > 0.8)$. The combined magnitude and PLV detector output is formed by AND-ing the outputs of the individual detectors. The threshold was adjusted for each patient.

In [31] the efficacy of the magnitude and PLV seizure detector VLSI architecture was verified by us on the intracranial EEG database from the international seizure prediction project from University of Freiburg [32]. A 70% detection rate is obtained when the false positives are set to the rate of 0.6 false positives per hour. The detection rate approaches 100% when the false positives rate is set to 1.2–2 false positives per hour across

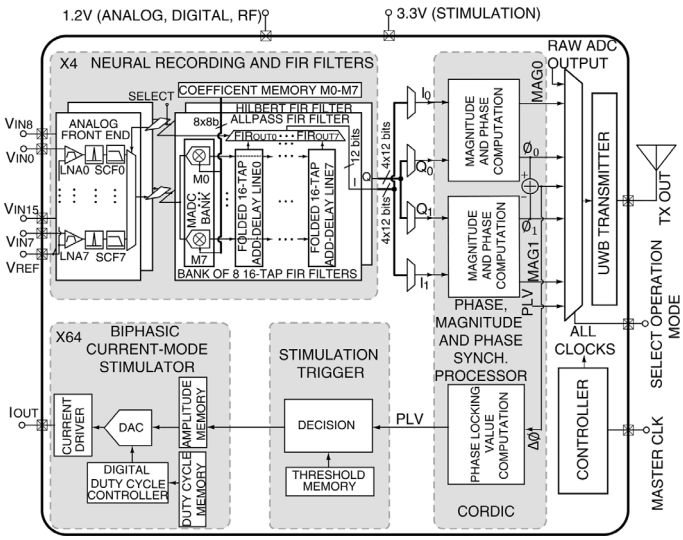

Fig. 3. Detailed system block diagram of the SoC.

multiple patients. This performance is comparable to other algorithms for early seizure detection, with the key advantage that our approach utilizes a low-power SoC that computes on-line and is implantable, as opposed to existing off-line software programs running on bulky computers.

2) Algorithm Accuracy: A resolution of 10-bits was selected for the processor. Fig. 4(a) shows the difference between results using off-line human seizure data obtained from an ideal resolution processor and a finite resolution processor quantified in standard deviations. In terms of seizure detection performance there is little benefit of increasing the processor resolution above 9 bits. As the processor resolution drops below 7 bits, the accuracy of the PLV algorithm degrades significantly. As the seizure in Fig. 4(b) approaches, the lower resolution 7-bit processor is not able to detect the small variations of synchrony which occur 30–40 seconds before the seizure as depicted in Fig. 4(c). For resolutions above 9 bits the performance is nearly identical.

B. Detailed VLSI Architecture

A detailed block diagram of the SoC is shown in Fig. 3. There are 64 ADCs organized in a scalable manner, one per neural input, for raw neural data monitoring (not shown). In the neural vector analysis and phase synchrony computation mode, the ADCs are re-configured as multiplying ADCs (MADCs). These MADCs perform the multiplications which are the most computationally intensive operations in allpass and Hilbert FIR filters. A bank of eight MADCs combined with a 16-tap folded add-and-delay line yields a 16-tap transposed symmetric mixed-signal FIR filter. MADCs are time-multiplexed among eight neural inputs and eight add-and-delay lines to comprise eight FIR filters [22]. In this design, two sets of eight FIR filters, eight allpass and eight Hilbert filters are implemented to compute I and Q components for eight inputs, respectively. The phase, magnitude and phase synchronization processor utilizes three digital CORDIC cores. By performing all FIR multiplications within the ADC, and utilizing vector processing in the

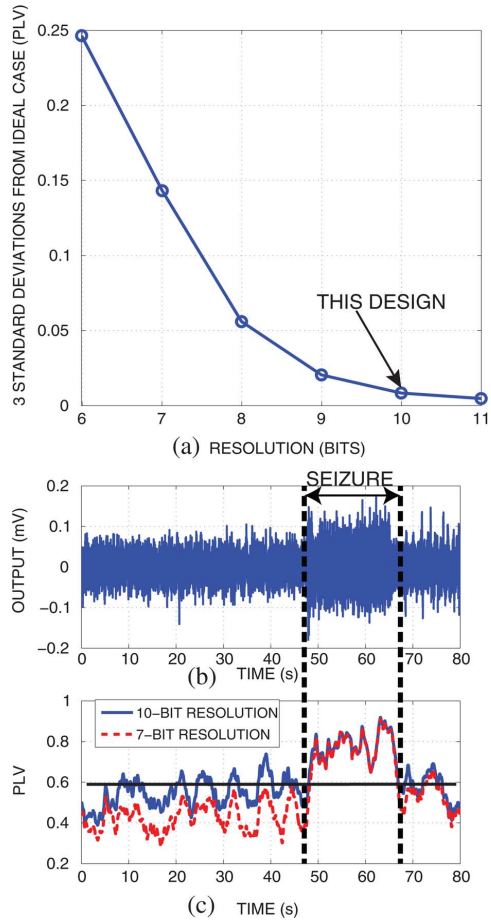

Fig. 4. (a) Simulated error of the PLV for different processor resolutions when compared with an ideal processor resolution. (b) Off-line human seizure data input for a University of Toronto epilepsy patient. (c) Simulated PLV between two inputs in the 25 Hz to 35 Hz frequency band computed for a processor resolution of 7-bits and 10-bits.

CORDIC-based processor, the computationally intensive digital multiplication operation is avoided entirely. The computed PLV value is compared with the programmed neural stimulation criteria. When triggered, the 64-channel neural stimulator generates individually programmable biphasic currents. The duty cycle and amplitude can be programmed and stored in the on-chip memory. An UWB wireless transmitter sends raw ADC data, neural vector parameters and PLV data off-chip. The SoC also contains 1 kb of on-chip registers that store the FIR coefficients, stimulation current amplitude and stimulation current duty cycle. The 0.13 μm CMOS SoC utilizes 1 million transistors and operates from a 1.2 V supply for the neural recording, signal processing and wireless transmission and a 3.3 V supply for the neural stimulation. An on-chip controller generates all clocks used by various blocks within the SoC.

III. VLSI Circuit Implementation

A. Neural Recording

1) Low-Noise Amplifier (LNA): Over the two stages the low-noise amplifier provides a tunable gain between 54 dB and 60 dB. The first stage of the amplifier has a small output voltage swing and thus utilizes two diode-connected MOSFETs

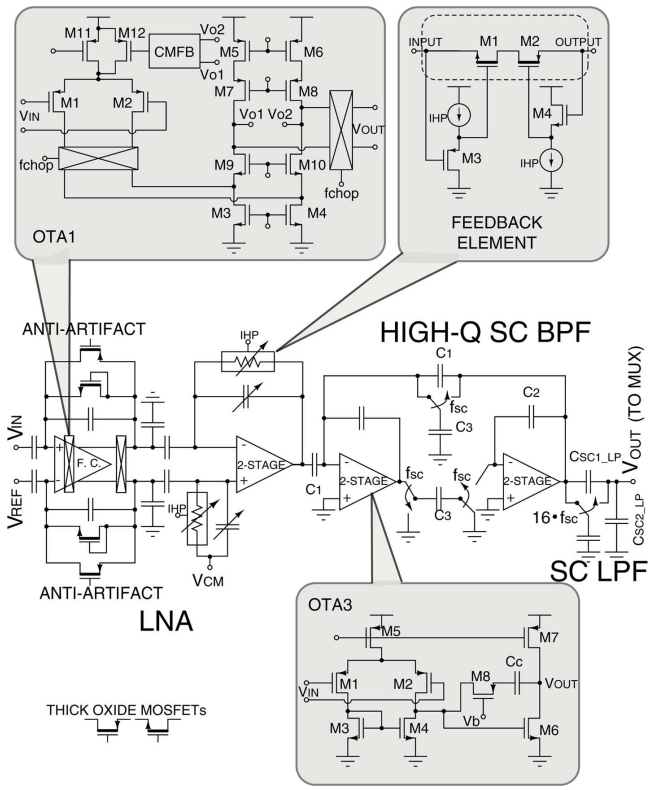

Fig. 5. Neural recording channel including LNA, SC BPF and SC LPF.

which implement two MOS-bipolar pseudo-resistive devices in its feedback [13]. For a larger output swing such as that of the second stage, $|V_{\rm GS}|$ of the feedback element would change resulting in a time-varying resistance and thus time-varying HPF pole frequency, leading to nonlinearities at low frequencies. The linearity of the front-end would degrade when the signal frequency is near the high-pass pole (below 1 Hz).

In the second stage, to ensure a more constant $|V_{\rm GS}|$ for the higher output swing and to allow for HP pole frequency tunability, two source followers act as floating DC voltage sources to track the dynamic output as shown in Fig. 5 [22], [33] and to ensure a fixed DC bias. This feedback element yields up to 14 dB improvement (experimentally validated) in linearity compared with the conventional approach [33]. The NMOS and PMOS feedback devices are implemented using thick oxide and the source followers are implemented using low-threshold thin-oxide devices. Transistor sizes of the feedback element are listed in Table I.

The first stage utilizes a fully differential folded-cascode OTA (OTA1 in Fig. 5) with a 60 dB open-loop gain. To minimize flicker noise of devices M3/M4 and M5/M6 the first chopping circuit is placed at the folded node. Placing chopping in front of the input pair, as is done conventionally [34], would have resulted in noise multiplication due to a switched capacitor resistor created by the parasitic capacitance of the input pair [25] and [34]. Conventionally, this is overcome by utilizing very large capacitors at the input of the amplifier [34] at the expense of large silicon area.

TABLE I
TRANSISTOR SIZES OF THE TWO OTAS AND THE FEEDBACK ELEMENT (F.E.) FOR THE NEURAL RECORDING AMPLIFIER AND THE NEURAL STIMULATOR

Transistor (OTA1)	W/L (μm)	Transistor (OTA3)	W/L (μm)
$M_{1,2}$	$25 \times 2/1.5$	$M_{1,2}$	$4 \times 0.5/5$
$M_{3,4}$	$4 \times 0.5/15$	$M_{3,4}$	$2 \times 0.5/10$
$M_{5,6}$	$4 \times 1/10$	M_5	$2 \times 0.8/3$
$M_{7,8}$	$4 \times 0.6/1$	M_6	$2 \times 1.0/3.8$
$M_{9,10}$	$4 \times 0.6/1$	M_7	$5 \times 0.8/3$
M_{11}	$4 \times 1/2$	M_8	$2 \times 2.5/1$
M_{12}	$1 \times 1/2$	C_c	1pF
Transistor (F.E.)	**W/L (μm)**	**Transistor (Stimulator)**	**W/L (μm)**
M_1	$1 \times 0.5/15$	M1	$5 \times 1/1$
M_2	$1 \times 0.5/15$	M2	$4 \times 2.5/1$
M_3	$2 \times 2.5/0.5$	M3	$4 \times 2.5/1$
M_4	$3 \times 1.0/0.5$	M4	$40 \times 2.5/1$
–	–	M5	$2 \times 2.5/1$
–	–	M6	$20 \times 2.5/1$
–	–	M7	$32 \times 2.5/0.4$
–	–	M8	$16 \times 2.5/0.4$
–	–	R	5.5kΩ
–	–	C_c	670fF

The low impedance at the folded-cascode node allows for high-frequency chopping at that node. We choose to chop at that node. The chopping harmonics are filtered out by the bandpass filter of the second stage of the low-noise amplifier. To minimize flicker noise of the input pair M1/M2, large PMOS devices are selected. To minimize thermal noise, transistors M1 and M2 are biased in the sub-threshold regime as needed to maximize their g_m. Transistors M3/M4 and M5/M6 are biased in saturation to minimize their g_m. The OTA requires a total of 2.6 μA of current which includes 1.6 μA into the input pair, 0.8 μA into the cascode transistors and 0.2 μA for the CMFB amplifier. The chopping frequency is set to 50 kHz. Comparing this approach to the same amplifier with chopper disabled, the experimentally measured input-referred noise improved from 6.5 μV to 4.7 μV integrated between 10 Hz and 5 kHz and the NEF improved from 7.2 to 4.4 for the same power dissipation. In this design, the bandwidth of the first stage was set higher as a result of minimizing the thermal noise (maximizing g_m) and reducing the area of the channel (minimizing $C_{\rm load}$). The overall bandwidth of the front-end is determined by the second-stage amplifier and the subsequent switched-capacitor filters, described in the next section. The second stage utilizes a two-stage OTA topology. This OTA has PMOS input devices, has an open-loop gain of 60 dB (sufficient for 8-bit resolution) and a phase margin of 70 degrees. It draws 350 nA of current from a 1.2 V supply. Transistor sizes for both OTAs are listed in Table I. All transistors utilize standard thin oxide devices.

The chopping amplifier was simulated using Spectre with PSS and Pnoise. When chopping is disabled, 30% of the total input-referred integrated noise in the frequency band from 10 Hz to 5 kHz is contributed by the flicker noise of M3 and M4 as shown in Fig. 6(a). When chopping is enabled, the majority of the total input-referred integrated noise is due to thermal noise as depicted in Fig. 6(b). Flicker noise is contributed mainly by the input differential pair. This design allocates 25% of the total noise contribution to the flicker noise of the input differential pair which can be further reduced by increasing the size of the input devices at the expense of silicon area.

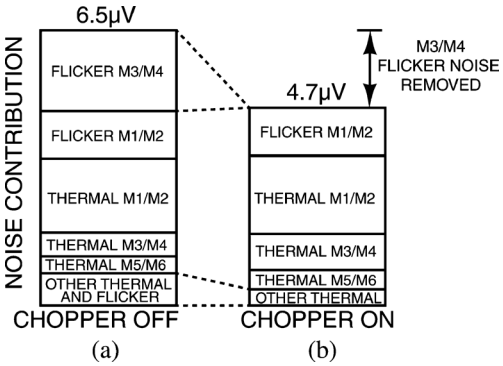

Fig. 6. Summary of simulated noise contributions with the chopper enabled and disabled.

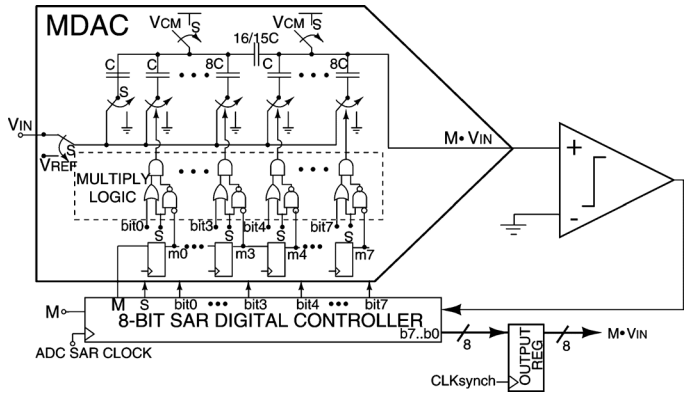

Fig. 7. Schematic of the SAR multiplying ADC (MADC).

2) Switched-Capacitor Bandpass Filter: The second-order bi-quad switched-capacitor (SC) bandpass filter (BPF) selects the neural band of interest. The circuit architecture as shown in Fig. 5 was selected as it minimizes the capacitance ratios resulting in a smaller area. The quality factor (Q) and center frequency, respectively, are

$$Q = \frac{C_2}{C_1}, \quad f_{\rm BP} = \frac{1}{2\pi}\frac{C_3}{C_2} f_{SC} \tag{4}$$

with $C_1 = 770$ fF, $C_2 = 2.5$ pF and $C_3 = 200$ fF. This yields a Q of 3.2 and a center frequency 78.5 times lower than the switched-capacitor clock frequency, $f_{\rm SC}$. A 2 kHz clock yields a center frequency of approximately 25 Hz.

The two OTAs are implemented using the two-stage topology, each requiring 350 nA of current with capacitors implemented as dense dual-MIM capacitors. Adjusting the SC clock frequency, $f_{\rm SC}$, enables linear tuning of the center frequency of the bandpass filter. This allows for filtering in different neural frequency bands.

3) Switched-Capacitor Lowpass Filters: The SC BPF discussed above introduces harmonics below the Nyquist rate of the ADC. To remove these harmonics a switched-capacitor lowpass filter (LPF) is utilized as shown in Fig. 5 in order to reduce the area of the on-chip passives required for the low-frequency filtering. The LPF is a SC LPF which utilizes a clock frequency that is 16 times higher than that of the switched-capacitor BPF filter, and attenuates the BPF harmonics. The lowpass pole frequency is

$$f_{\rm LP} = f_{\rm SC}/(2\pi * 10) \tag{5}$$

and yields

$$\frac{f_{\rm BP}}{f_{\rm LP}} = 0.8. \tag{6}$$

This sets the LP SC filter cutoff frequency to 1.25 times the center frequency of the SC BP filter.

B. FIR Filtering Circuits

1) Multiplying SAR ADC: A successive approximation register (SAR) ADC is often used to digitize the amplified neural signals since it provides high energy efficiency for medium resolutions and sample rates. The implemented ADC is an 8-bit charge redistribution SAR multiplying ADC (MADC) as shown in Fig. 7 and detailed in [22]. It multiplies two digital values at the cost of a small overhead of three two-input logic gates per bit as shown in Fig. 8. The ADC dissipates 1.8 μW at 56 kS/s from a 1.2 V supply. Each channel contains a 22-bit register to store the 8-bit multiplication coefficient, two 1-bit sign coefficients for the FIR filter, and 12-bits for neural stimulation mode.

2) Neural Signal Filtering Modes: The SoC is divided into eight modules each consisting of eight channels. A module in different configuration modes is shown in Fig. 8(a)–(c). In the raw-ADC mode, the analog output is digitized directly by the ADC as shown in Fig. 8(a). In the FIR filtering mode, an OTA buffer drives the eight parallel MADCs of the mixed-signal FIR filter. Each MADC is a SAR ADC with a multiplying DAC (MDAC). In this mode, 64 recording channels use the 64 FIR filters as depicted for eight channels in Fig. 8(b). In I/Q vector mode, the OTA buffer drives two sets of eight parallel MADCs. One set of MADCs implements an FIR filter programmed as an allpass filter (I-extraction). The other set implements an FIR filter programmed for the Hilbert transform (Q-extraction). In this mode, 32 recording channels utilize 64 FIR filters (32 allpass and 32 Hilbert FIR filters) as shown for eight channels in Fig. 8(c). Both the I and Q signals are sent to the on-chip CORDIC processor to compute the magnitude, phase and phase synchronization.

Eight or 16 recording channels share the tuneable RC LPF as shown in Fig. 8(b) and (c), respectively. The RC LPF removes the higher frequency harmonics of the in-channel SC LPF described in Section III.A.3 and switching harmonics of the multiplexer. The two-stage OTA buffer draws a current of 25 μA. The value of R is tuneable between 365 kΩ to 1.5 MΩ and the value of C is 25 pF yielding a lowpass pole between 4.2 kHz and 17.4 kHz. For example, for a SC BPF center frequency of 65 Hz, this requires a SC BPF clock frequency of 5 kHz and a SC LPF clock frequency of 80 kHz $(16 \times f_{\rm SC})$. The 80 kHz harmonics are then removed by this RC lowpass filter.

C. Phase, Magnitude, and Phase Synchronization Processor

The block diagram of the digital signal processor that computes phase, magnitude and phase synchronization is shown

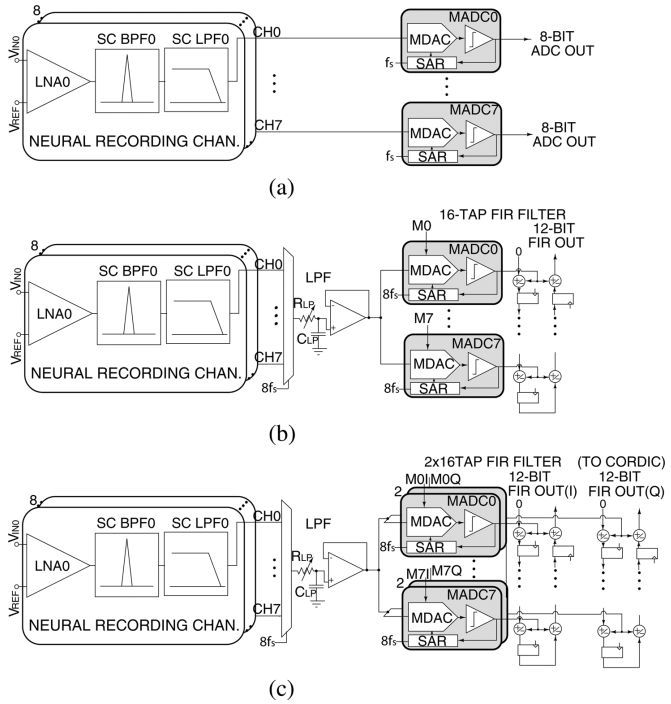

Fig. 8. Integrated circuit implementation of eight channels of neural signal filtering for different modes of operation. (a) Raw data ADC mode, (b) general purpose filtering FIR mode and (c) I/Q extraction mode.

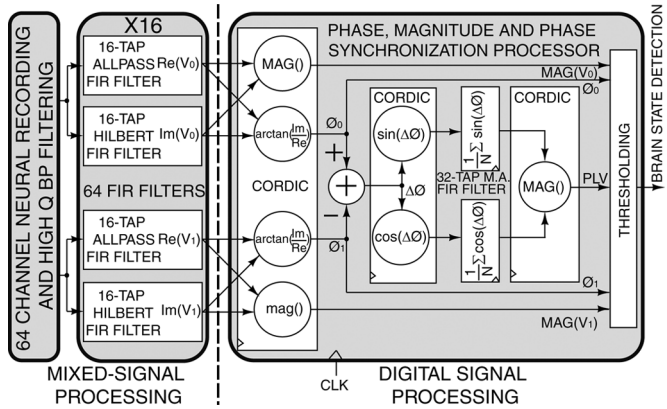

Fig. 9. Block diagram of the phase, magnitude and phase synchronization processor.

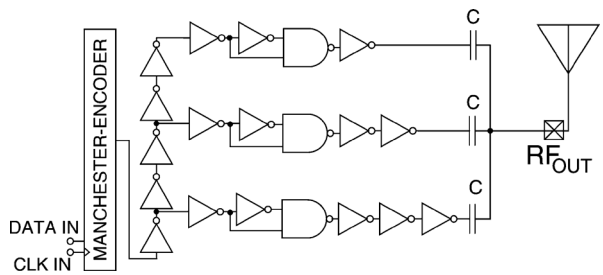

Fig. 10. Schematic of the UWB transmitter.

on the right hand side of Fig. 9 and detailed in [31]. The processor receives vectored inputs, I and Q, for each of the two channels. The 10-bit processor is fully synthesized utilizing three CORDIC cores to simultaneously compute the magnitude, phase, phase difference and the phase-locking value per sample. An iterative CORDIC-based architecture was selected as it does not require any digital multiplication, but only adders, bit shifters and memory retrieval operations [35]. This minimizes the area and power dissipation while trading-off speed and latency. It utilizes 41 k gates, requires 18 clock cycles per operation, occupies an area of 0.178 mm^2 and has a total latency of 54 clock cycles. It dissipates 200 μW from a 1.2 V supply at 2 MHz at 1.7 kS/channel and scales linearly with the sampling rate. A digital threshold can be programmed to trigger a stimulation pulse if the magnitude, phase, phase-difference or PLV goes above or below a chosen threshold.

D. UWB Transmitter

The block diagram of the all-digital pulsed ultra wideband (UWB) transmitter is shown in Fig. 10. The input data are modulated using on-off keying (OOK) modulation at up to 10 Mb/s. UWB pulses are generated on the rising edge of the input data. The proposed digital UWB transmitter achieves both power efficiency and spectral compliance in a minimal chip area by combining a delay line architecture with a capacitively coupled output combiner [36]–[38]. The input data are passed through a delay line and a delayed version of the input data are passed through three pulse generators. The width of the output pulse depends on the delay in the delay lines. The pulse generators form a first-order Gaussian pulse at the rising edge of the input data. The delay cells in all the paths are implemented as current-starved inverters to allow for tuning of the UWB pulse width for two different bands (0–1 GHz or 3.1–10.6 GHz).

E. Neural Stimulator

1) DAC-Sharing Architecture: Any of the 64-channels can be individually configured as a neural recorder or a neural stimulator. Incorporating neural recording and neural stimulation capabilities into each channel requires both an ADC for the recording phase and a DAC and digital controller for the stimulation phase.

The SAR ADC described in Section III.B.1 requires a capacitor-array DAC and digital SAR logic which take up a significant amount of area. The DAC as well as the digital logic SAR controller can be reused for neural stimulation since the neural recording and stimulation circuits do not operate at the same time on one input. Here the SAR MADC is reconfigured such that the MDAC and the digital logic of the SAR MADC are reused to set the stimulation current amplitude and its duty cycle, respectively, as shown in Fig. 11. By sharing the MDAC and digital logic between the recording and stimulation phases, a more compact implementation is realized.

In the neural stimulation mode, the MDAC of the SAR MADC operates as a voltage DAC and the SAR logic of the MADC is reconfigured to implement duty cycle modulation. Both are combined with a V-I converter and an output current driver to implement the current-mode neural stimulator as shown in Fig. 11. The neural stimulator is a biphasic current stimulator with an 8-bit in-channel DAC, a 4-bit duty

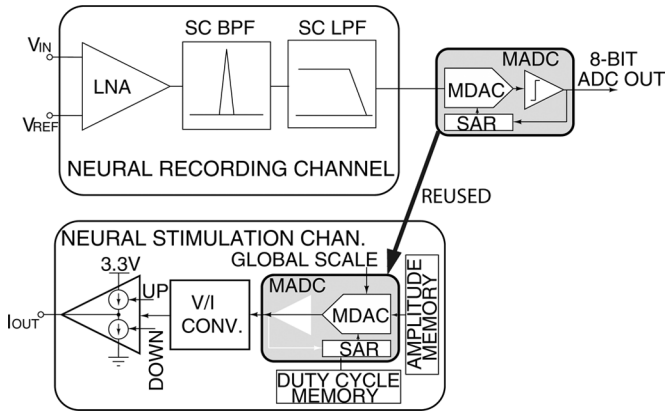

Fig. 11. MADC reuse in the neural stimulation mode.

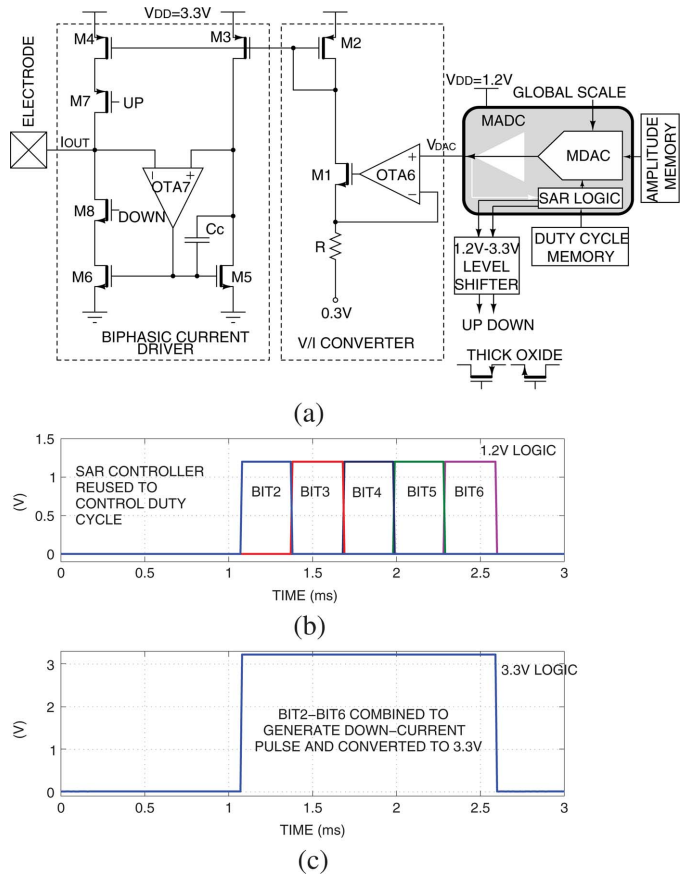

Fig. 12. (a) Schematic of neural stimulator. (b)–(c) Example simulation results showing output bits from the SAR ADC logic being used to generate a stimulator current pulse.

cycle controller and the corresponding 12-bit shift register memory. Biphasic current-mode stimulation is preferred over voltage-mode stimulation as it offers direct control over the charge delivered to the tissue and ensures charge balancing when sinking and sourcing current to and from the neural tissue. Currents in the range of 10 μA–1 mA can be generated and are sufficient to invoke a neural response [39].

The detailed schematic is shown in Fig. 12(a) with transistor sizes listed in Table I. The main components of the stimulator are an 8-bit MDAC capacitor array, low-power SAR digital logic, the voltage-to-current converter and the high-impedance biphasic current driver.

2) DAC and Duty Cycle Controller: The DAC and duty cycle controller are reconfigured from the SAR ADC architecture. Each bit is toggled beginning with the most significant bit. There are eight pulses in a shift register which toggle each bit of the DAC. To adjust the duty cycle, these pulses are combined together to form a wider or narrower current pulse. Two conversion cycles are required for a biphasic current pulse generation. During one conversion cycle up to eight different pulses can be combined to form the positive phase pulse and similarly up to eight different pulses can be combined to form the negative phase pulse. This requires 4-bit storage for adjusting the duty cycle. The approach to combine pulses to modulate the duty cycle, is illustrated in an example in Fig. 12(b) an (c), where five bits are combined to generate the positive biphasic current pulse. To minimize both area and power, all digital logic utilizes 1.2 V thin-oxide devices with minimum length (0.12 μm). The signal is boosted to 3.3 V to drive the rest of the stimulator circuitry.

3) Voltage-to-Current Converter: The capacitive DAC output voltage ranges from 0.3 V to 0.9 V (which matches the input range of the ADC). The DAC voltage is forced across an on-chip resistor R of 5.5 kΩ by OTA6 as shown Fig. 12. The current gets multiplied by 10 by setting the current mirror width ratios of M2:M4 and M5:M6 to 1:10. The common reference voltage of the DAC is 0.3 V, and thus the generated current is

$$I_{\mathrm{DAC}} = 10\,(V_{\mathrm{DAC}} - 0.3V)/R \tag{7}$$

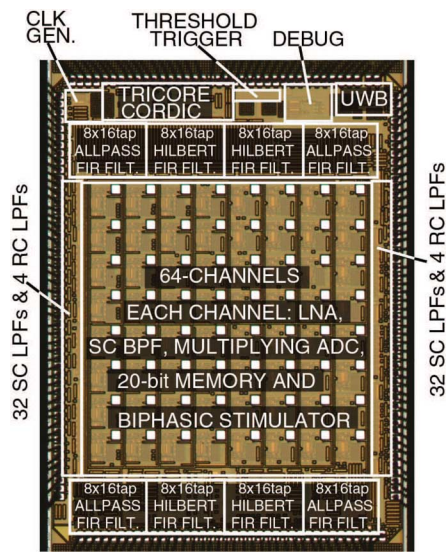

Fig. 13. Micrograph of the 4 mm × 3 mm 0.13 μm CMOS SoC.

which ranges between 5 μA and 1.09 mA. This selection of R can be adjusted for the intended application or electrode impedance. The on-chip resistor value can vary by 10% over process corners. With a large channel count, to adjust for this, the currents for each channel can be read off and each channel

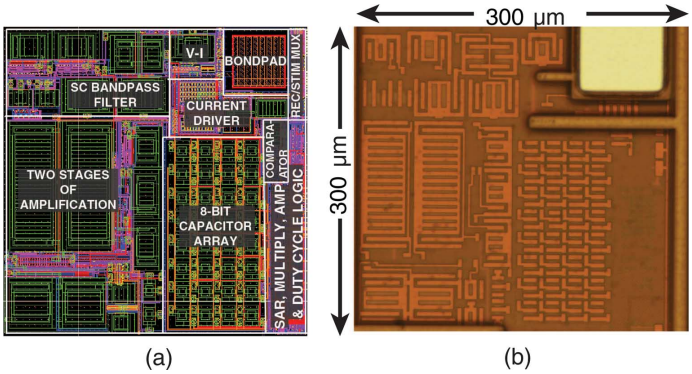

Fig. 14. (a) Layout and (b) micrograph of the recording and stimulation channel.

can be digitally calibrated. The OTA6 in the voltage-to-current converter uses thick oxide 3.3 V devices and a standard two-stage architecture.

4) Current Driver: For the current driver it is important to ensure that the positive and negative current pulses are matched closely to minimize excess charge at the electrode-tissue interface. It is also important to have a high impedance at the electrode node to ensure the current is less sensitive to the load variations. As shown in Fig. 12(a), during the UP pulse, the current from the voltage-to-current converter is mirrored to the output transistor M4. This current is inversely proportional to the electrode voltage at the drain of M4. To match currents between the UP and DOWN pulses, OTA7 ensures the current during the DOWN pulse is also inversely proportional to the electrode voltage at the drain of M7. OTA7 was implemented using a five-transistor differential amplifier with thick-oxide devices.

A ratio of 1:10 was selected to implement the current mirrors to reduce area and power dissipation. Capacitor C_c was added to stabilize the feedback loop with OTA7 across all operating conditions of the current driver. For this feedback loop, capacitor C_c sets the dominant pole and thus lowers the unity-gain frequency from 33 MHz to 1.7 MHz while increasing the phase margin to 74 degrees. An additional inversion due to the common-source transistor M5 implements Miller compensation. For lower stimulation currents, the second pole frequency is lowered and stability degrades. The worst-case operating condition (10 μA) has a phase margin of 54 degrees. OTA7 can also be configured to remove any excess charge from the tissue after the stimulation by applying the reference voltage to the electrode [40].

IV. Electrical Experimental Results

The micrograph of the SoC implemented in a standard 1P8M IBM 0.13 μm CMOS technology is shown in Fig. 13. The SoC occupies an area of 4 mm $\times$ 3 mm. There is a total of 1 kb of on-chip memory and approximately 1 million transistors. The SoC operates from a 1.2 V supply for the neural recording, digital signal processing and RF transmitter and a 3.3 V supply for the neural stimulator. The micrograph and layout of the full channel including the neural recording amplifier, SC bandpass filter, biphasic current driver, multiplying SAR ADC/DAC and a 22-bit memory are depicted in Fig. 14(a) and (b). The full

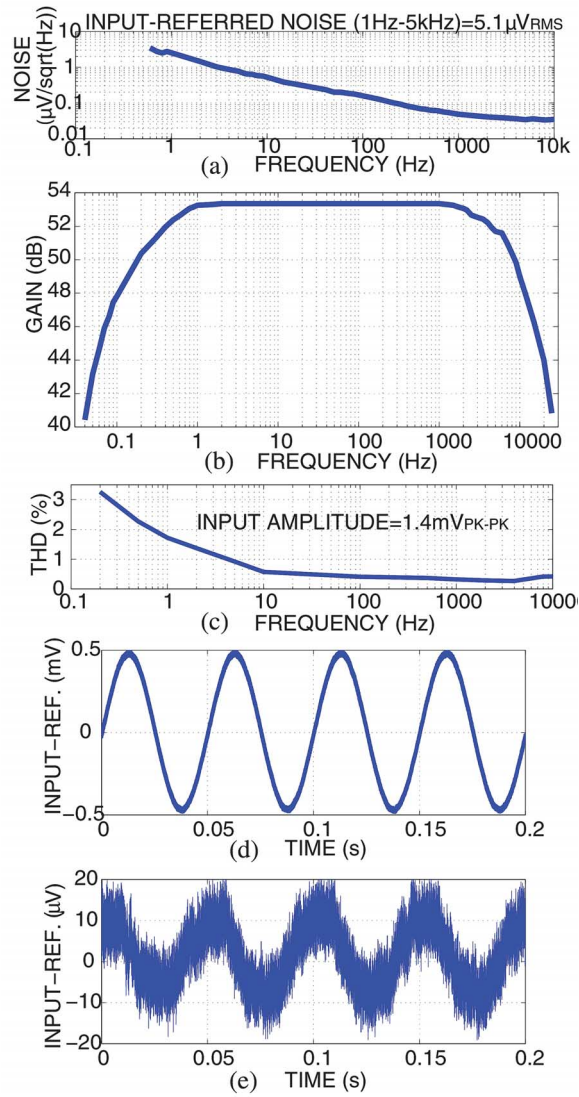

Fig. 15. Experimentally measured (a) input-referred noise, (b) frequency response of neural recording amplifier and (c) total harmonic distortion (THD). (d) Experimentally measured output waveforms for a 20 Hz 1 mV_{pk-pk} input and (e) a 20 Hz 20μV_{pk-pk} input.

channel occupies 300 μm $\times$ 300 μm of area. Each channel has a bondpad to be flip-chip bonded directly to a microelectrode array.

A. Analog Front-End and Switched-Capacitor BPF

The experimentally measured input-referred noise, amplitude frequency response and total harmonic distortion (THD) of the neural recording channel are shown in Fig. 15(a)–(c). The amplifier has an integrated input-referred noise of 4.7 μV and 3.7 μV for the frequency bands of 10 Hz to 5 kHz and 1 Hz to 100 Hz, respectively. The NEF of the fully differential neural recording amplifier is 4.4 for the 5 kHz bandwidth. The experimentally measured CMRR at 10 Hz and 1 kHz is 75.4 dB and 71.5 dB, respectively. The frequency response is consistent across multiple channels on the chip. Both the highpass and lowpass poles can be adjusted, with the maximum bandwidth of 0.01 Hz to 10 kHz. The experimentally measured THD is

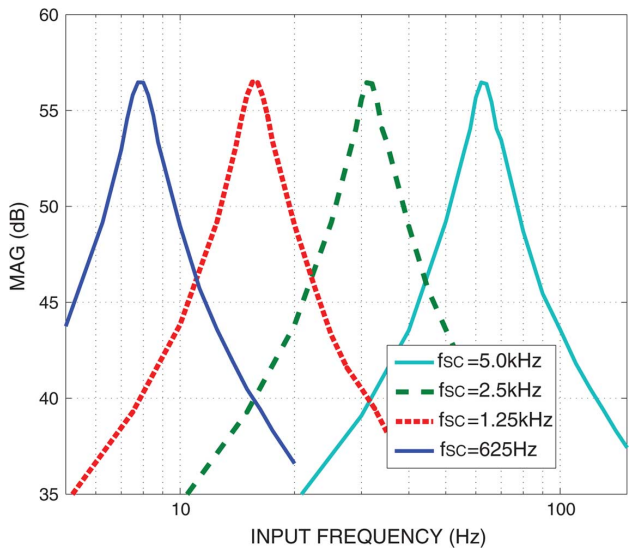

Fig. 16. Experimentally measured frequency response of the neural recording amplifier and the switched-capacitor bandpass filter.

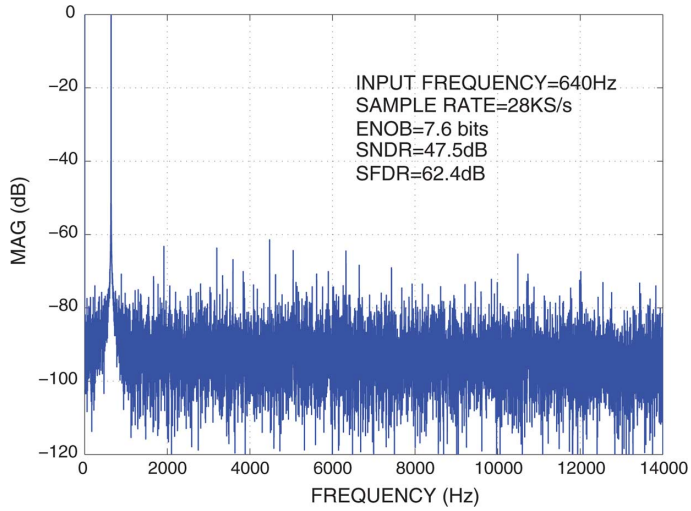

Fig. 17. Experimentally measured FFT of an in-channel ADC output with a 640 Hz input and sampled at 28 kS/s.

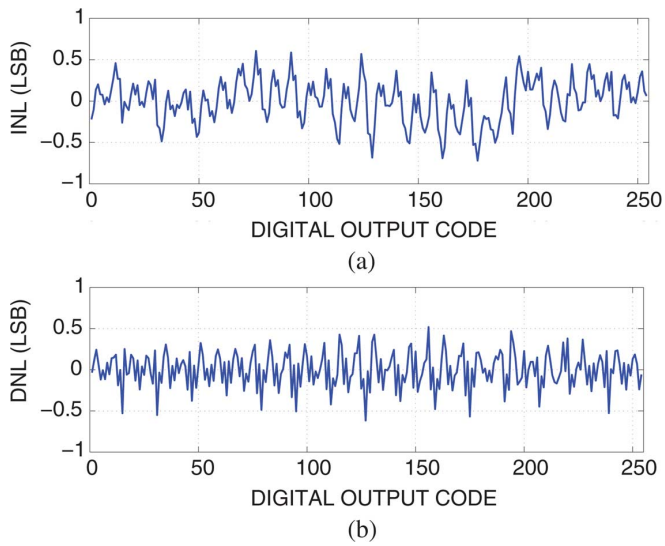

Fig. 18. Experimentally measured (a) INL and (b) DNL of an in-channel ADC, sampled at 28 kS/s.

-50 dB when the output is 700 mV between 100 Hz and 5 kHz and drops to -35 dB at 1 Hz due to the non-linearity introduced by the feedback device of the second stage. The output waveforms for a 1 mV_{pk-pk} 20 Hz sinusoid and a 20 μV_{pk-pk} 20 Hz sinusoid inputs are shown in Fig. 15(d) and (e), respectively. For the 1 mV_{pk-pk} input (0.5 V_{pk-pk} output), the distortion is not visible, with a THD below -50 dB. Fig. 15(e) depicts the output for a low-SNR signal of 20 μ V_{pk-pk}. The amplifier noise and high frequency ripple due to the chopper switching can be observed.

The experimentally measured frequency response of the neural recording amplifier and SC BPF is shown in Fig. 16. Four different bands are shown when tuning the SC clock between 625 Hz and 5 kHz that yield the bandpass filter center frequency of 8 Hz, 16 Hz, 32 Hz and 64 Hz, respectively. The SC filter provides an additional 2 dB of gain to the analog front-end.

B. ADC and Full Recording Path

The experimentally measured FFT of an in-channel ADC is shown in Fig. 17. The ENOB and SFDR are 7.6 bits and 62.4 dB, respectively. The ADC achieves close to 7 bits over the full Nyquist bandwidth with consistent performance across multiple channels on the chip. The experimentally measured INL and DNL are 0.6 and 0.7, respectively, as shown in Fig. 18. The FFT of the full recording path output including the analog front-end, SC bandpass filter and the ADC is displayed in Fig. 19(a). The 5 kHz harmonic clock of the SC BPF (CLK_{SC}) is visible in the spectrum and limits the SFDR to 38 dB. As shown in Fig. 19(b), when enabling the SC and RC lowpass filters and programming the FIR filter as a lowpass filter, the SFDR improves to 51 dB. A larger second harmonic is introduced due to mismatch of utilizing eight different ADCs in the FIR filtering mode.

C. Neural Vector Analysis and Phase Synchronization

The SoC was characterized to demonstrate the computation of magnitude, phase and phase synchronization. Fig. 20 depicts experimental results for the full signal path from the LNA to the SC filter (set to 30 Hz center frequency) then processed by two 16-tap FIR filters to generate the real and imaginary components. Fig. 20(a) and (b) shows the I/Q extraction for a low-amplitude (30 μV) sinusoid signal. Fig. 20(c) and (d) shows the case for a larger amplitude input (500 μV) sinusoid signal. Both cases yield an accurate 90 degree phase shift. The frequency response of the I/Q extraction measured starting from the input of the LNA is depicted in Fig. 20(e) when the SC filter is centered at 30 Hz. Due to the approximate response of the 16-tap FIR filters, exact gain matching between I and Q is not achieved with a difference of approximately 2 dB, as expected in Matlab simulations. A higher

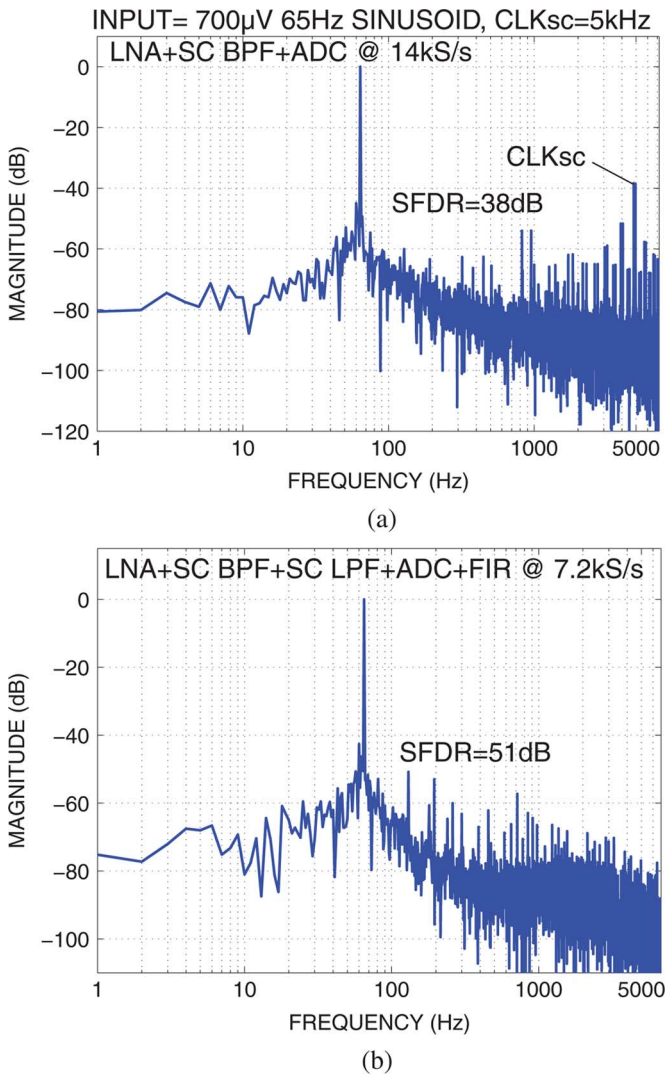

Fig. 19. (a) Experimentally measured output FFT of an in-channel analog front-end, SC BPF and ADC with a 65 Hz 700 μV input sampled at 14 kS/s. (b) Experimentally measured output FFT of an in-channel analog front-end, SC BPF, SC LPF, RC LPF and FIR LPF with a 65 Hz 700 μV input sampled at 7.2 kS/s.

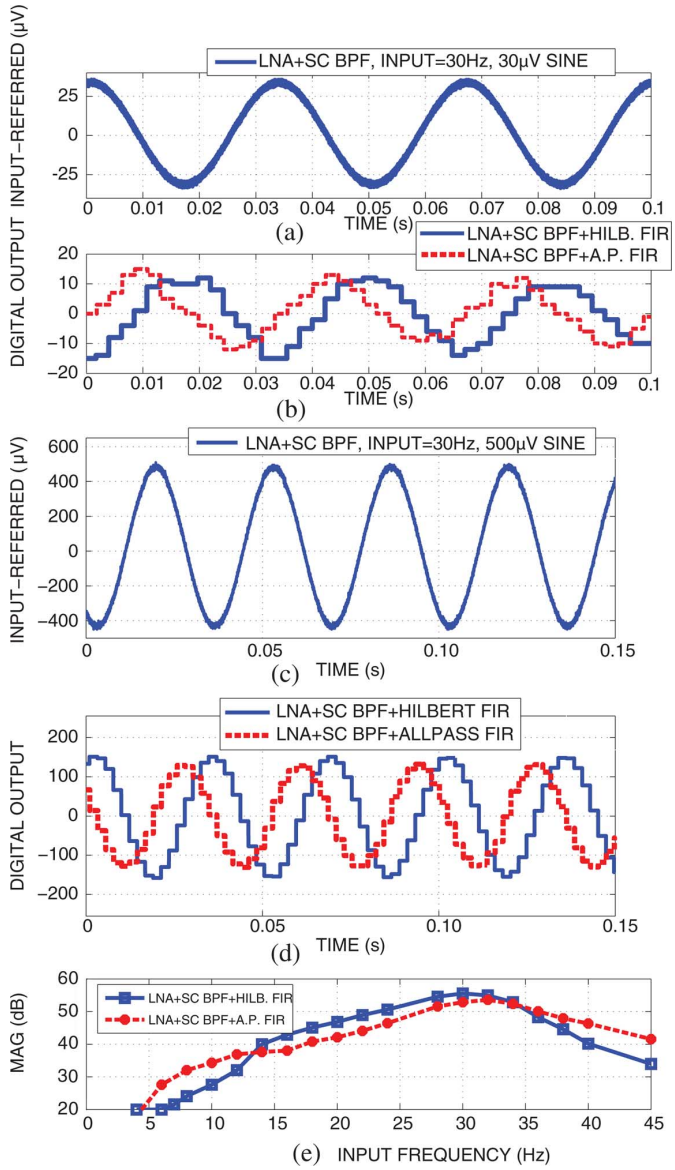

Fig. 20. (a) A low-amplitude sinusoidal input into the neural recording amplifier. (b) Experimentally measured I/Q separation of signal in (a) including full signal path of input (a). (c) A high-amplitude sinusoid input into the neural recording amplifier. (d) Experimentally measured I/Q separation including full signal path of input (c). (e) Experimentally measured frequency response of full signal path for I and Q.

order FIR filter achieves more accurate gain matching at the expense of area and power dissipation.

Experimental results for the phase difference computation between two neural recording channels are shown in Fig. 21(a). The two input sinusoid signals have an amplitude of 100 μV and a frequency of 30 Hz. The phase difference was varied using a Tektronix arbitrary waveform generator and the computed phase was plotted against the phase displayed on the source. In Fig. 21(b), the two signals were placed at a 180 degree phase shift and the amplitudes of both signals were swept. At low SNR (10 μV-inputs), the phase varied by 60 degrees over three standard deviations from the mean. At higher SNR (500 μV-inputs), the phase varied by five degrees over three standard deviations from the mean.

The magnitude was computed for a single channel as shown in Fig. 21(c) and (d). Fig. 21(c) displays the extracted magnitude for different signal amplitudes from 12.5 μV to 400 μV and compares with the ideal magnitude. Fig. 21(d) depicts the computed magnitude in response to a slow step-wise amplitude increase of only 25 μV into the amplifier. The minimum noise floor for magnitude extraction is 8 μVrms.

The phase-locking value (PLV) was computed on-chip between two different inputs for three different frequency bands. The experimental results are shown in Fig. 22(a). In this case, a 100 μV sinusoid input was held constant at 8 Hz, 30 Hz and 120 Hz with the SC BPF center frequency set to these frequencies. The other 100 μV sinusoid signal frequency was swept and the PLV was computed. The PLV output is 1 as expected when both frequencies are locked. Any deviation away from the center frequency yields a lower phase synchronization as expected. In

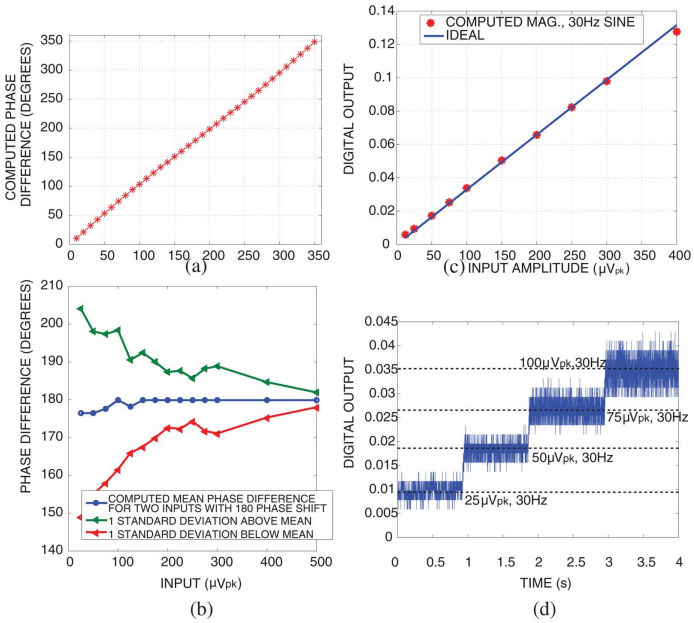

Fig. 21. (a) Experimentally measured phase difference computation results including full signal path (100 μ V inputs). (b) Experimentally measured phase difference error for different input amplitudes between two neural recording amplifiers. (c) Experimentally measured magnitude computation including full signal path and compared with the ideal case. (d) Experimentally measured magnitude computation of a low-frequency step introduced at the input of the neural recording amplifier.

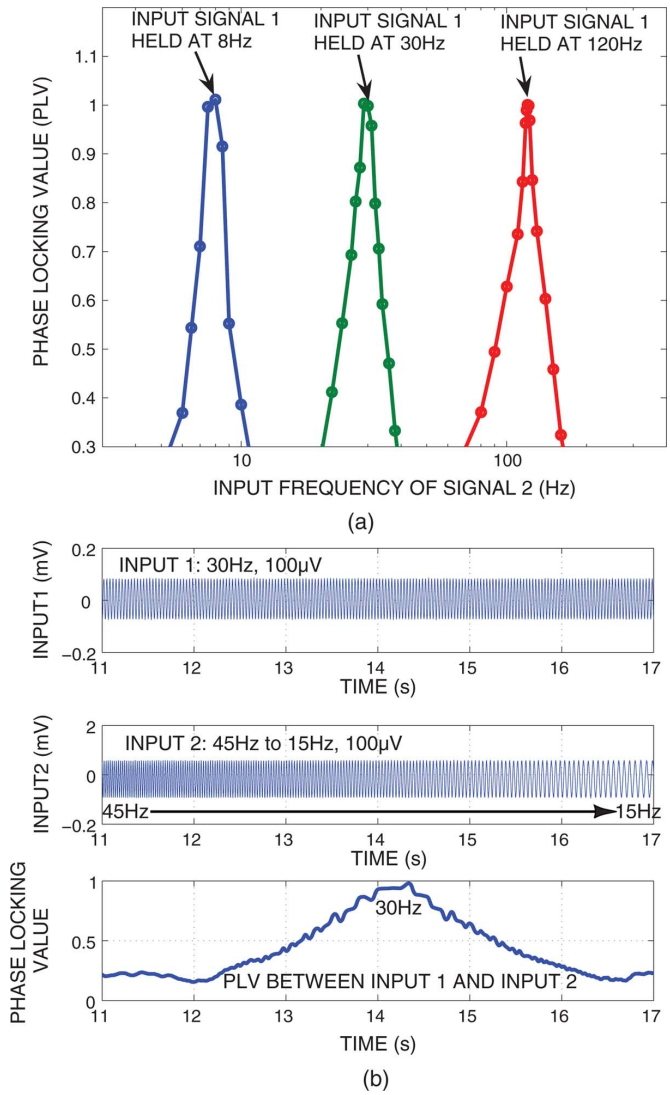

Fig. 22. (a) Experimentally measured PLV computation between two different channels for three different frequency bands. (b) Experimentally measured PLV computed between two channels, where one frequency is constant for one channel and the other frequency is increasing for the other channel.

Fig. 22(b), one 100 μV sinusoid was set to 30 Hz and the other 100 μV input had its frequency linearly swept from 45 Hz down to 15 Hz. The PLV tracks the change in the frequency and outputs a 1 when both frequencies are 30 Hz.

D. UWB Transmitter

Fig. 23(a) shows transmitted 10 MB/s Manchester encoded-data. Fig. 23(b) depicts the wirelessly received UWB modulated data utilizing the 3.1–10.6 GHz UWB frequency band across a 5 cm distance with a bit-error-rate (BER) of 5×10^{-3}.

E. Neural Stimulator

The neural stimulator reuses the same MDAC as the SAR MADC and exhibits an INL and DNL below 1 LSB as depicted in Fig. 18. The neural stimulator was characterized experimentally using both a resistive load and a saline solution. In Fig. 24(a) the DAC was set to output 225 μA and the electrode voltage was swept from 0.3 to 2.7 V. The results show a close match between the positive and negative current pulses. The UP and DOWN currents are accurately matched (close to 1%) when the electrode voltage swings as high as 2.0 V.

If a lower current is used ($<$100 μ A), the currents are matched when the electrode voltage swings as high as 2.5 V. When the output voltage is high the UP current source transistor M1 in Fig. 12(a) enters the triode region and no longer sustains the proper current. Similarly, when the output voltage is low the DOWN current sink transistor M6 enters the triode region and can no longer sustain the proper current. When the output voltage is high (above 2.5 V), OTA7 can no longer maintain the proper loop gain. By disabling OTA7 at high output voltage, the swing can be extended at the expense of lower current matching.

The output current for different DAC configurations is depicted in Fig. 24(b). The UP and DOWN currents up to 1 mA are closely matched. Fig. 24(c) and (d) shows various amplitude and duty cycle configurations for the neural stimulator while generating a biphasic current pulse into a saline solution. Lastly, the voltage across a 1 kΩ resistor is shown on the oscilloscope plot in Fig. 24(e) when the biphasic neural stimulator is programmed for a 450 μA current.

V. Experimental Validation in Epilepsy Control

The SoC was demonstrated experimentally in both detection and control of epileptic seizures. An on-line animal epilepsy model (*in vivo* freely-moving rodents) and off-line human ECoG data from epilepsy patients were used to validate the SoC.

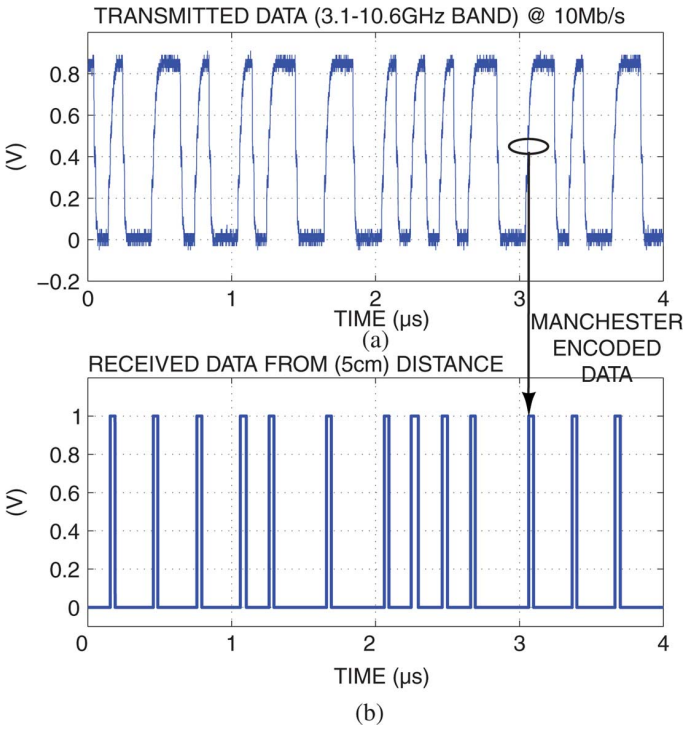

Fig. 23. (a) Wireless transmitter digital Manchester-encoded data. (b) Experimental wirelessly received data from a 5 cm distance @ 10 Mb/s in the 3.1–10.6 GHz band.

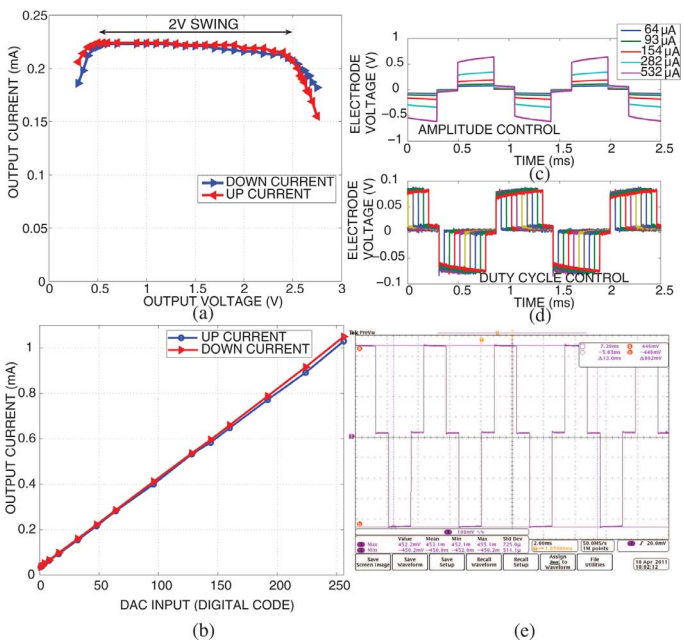

Fig. 24. (a) Experimentally measured output current for different output voltages. (b) Output current vs. DAC input for positive and negative current cases. (c), (d) Experimentally measured neural stimulating current into a saline solution for different duty cycle and amplitude control settings. (e) Biphasic stimulator set to 450 μA output current and connected to a 1 kΩ load.

A. On-Line Early Seizure Detection and Control in Rodents In Vivo

A model was used in-vivo, which trigger convulsive seizures in Long Evans rats, aged between 55 and 90 days. The convulsive model induces spontaneous seizures after an injection

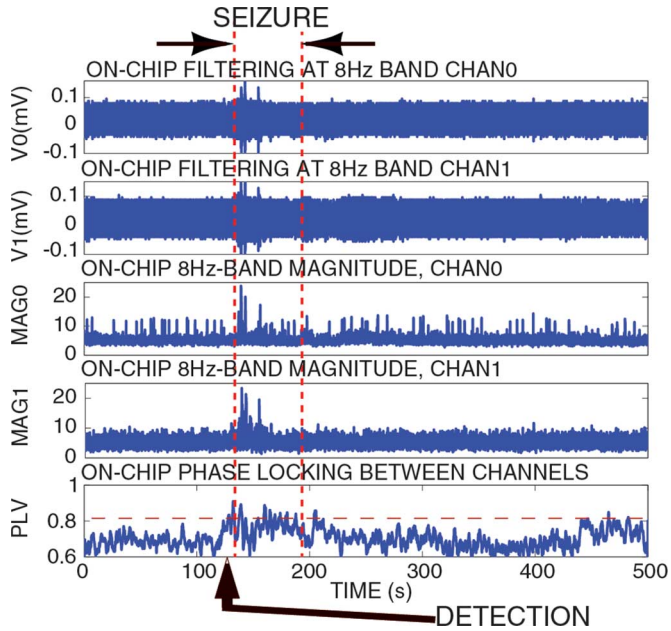

Fig. 25. In-vivo testing in a freely moving rat showing detection of a convulsive seizure triggered by a kainic acid injection at $t = -5$ min.

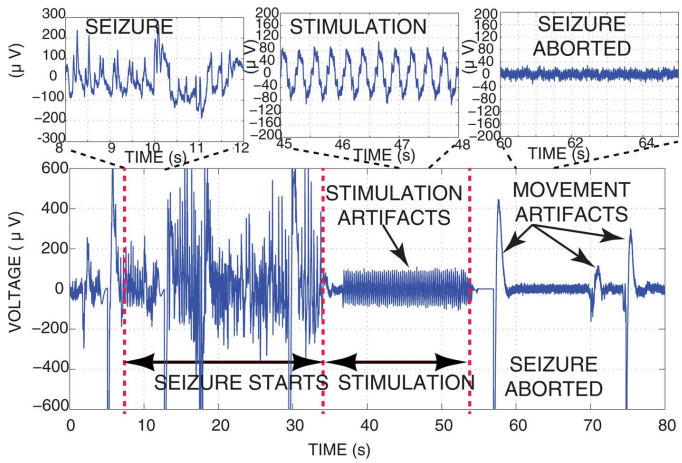

Fig. 26. Successful abortion of a seizure in a rat using the on-chip neural stimulator.

of kainic acid. Five electrodes were implanted into the hippocampus of freely moving rats. The electrodes are bipolar electrodes (Plastics One) and were implanted chronically into the hippocampi, cortex and thalamus brain regions of the Long Evans rats (55 to 90 days old) using a stereotaxic apparatus. Two different pairs of electrode inputs were processed by the SoC, and another electrode provided a reference. Seizures were labeled by examining the rodents's LFPs in realtime recorded by a benchtop amplifier in parallel, and by observing the rat's seizure-like symptoms, both by trained epileptologists.

Rats were injected with kainic acid to induce convulsive seizure-like events. The administered dose was a 15–20 mg/kg intraperitoneal injection. Similarly, the magnitude and phase synchronization were observed to increase before and during the seizure-onset and disappear after the seizure. In Fig. 25, a convulsive seizure (at 8 Hz) in a rat is induced by a kainic acid

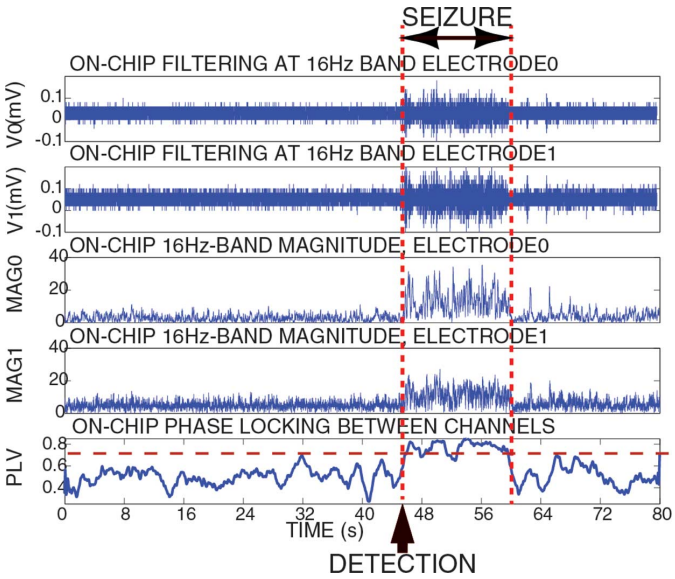

Fig. 27. Off-line human seizure detection for a University of Toronto seizure patient.

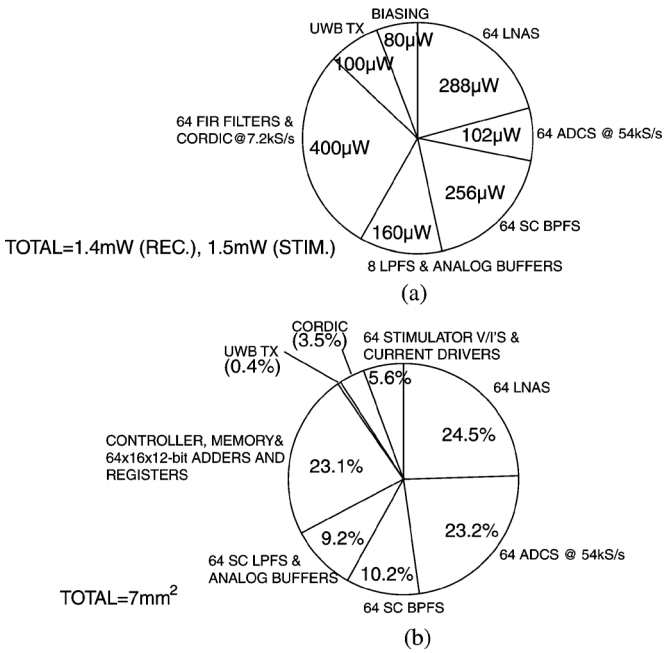

Fig. 28. (a) Power dissipation breakdown of the SoC (neural stimulator excluded). (b) Area breakdown of the SoC. The remaining 5 mm^2 are utilized for I/O, ESD, test blocks, routing, decoupling capacitors and biasing.

injection at time $t = -5$ min. The phase synchrony in the 8 Hz band increases approximately 20 s before the seizure starts and the magnitude in the 8 Hz band increases during the seizure. In Fig. 26, after a seizure was observed, a 5 Hz, 100 μA biphasic current stimulation was invoked and the seizure was aborted. Overall, on-chip responsive electrical stimulation aborted 80% of all rat seizures. The stimulation current pulse was invoked after the seizure onset, delayed on purpose so that the seizure onset and seizure abortion can be easily observed electrically and visually. This approach would not yield the best result, as it is better to stimulate before the seizure onset [41], [42]. In a future study, we plan to trigger the neurostimulator before the seizure onset and compare the seizure reduction rate between closed-loop neurostimulation and open-loop neurostimulation in a large population animal study (over 100).

In early seizure detection in rodents, the real-time processing of phase synchrony between two inputs in the 4 Hz and 8 Hz bands was used to provide early seizure detection of between 4 and 20 seconds before the seizure onset. This was better than the case of observing only magnitude, which increased above a detection threshold only after a seizure onset.

TABLE II
SUMMARY OF THE EXPERIMENTAL RESULTS

System:	
Technology	IBM 0.13μm
Supply Voltage (Rec.)	1.2V
Supply Voltage (Stim.)	3.3V
Die Dimensions	4.0mm×3.0mm
Area per Channel	$300\mu m \times 300\mu m$
Number of Recording Channels	64
Number of Stimulation Channels	64
On-Chip Memory	1kb
Number of Transistors	1 Million
Power Dissipation (Rec.)	1.4mW
Power Dissipation (Stim.)	1.5mW
Recording Channel:	
Gain	54-60dB
Input-Ref. Noise (1Hz-5kHz)	$5.1\mu V$
Input-Ref. Noise (1Hz-100Hz)	$3.5\mu V$
LNA NEF	4.4
CMRR	75dB
THD @ 1kHz	0.3%, 0.9V output
ADC SNDR	47.5
ADC SFDR	62.5
ADC ENOB	7.6-bits
ADC INL	0.7LSB
ADC DNL	0.6LSB
ADC Sample Rate	up to 100kS/s
Power Diss. (LNA+SCF+ADC)	10μW
Signal Processing:	
Analog Filters	64x high-Q SC BPF
Number of FIR filters	64
FIR filter type	Symmetric 16-tap
Coefficient Resolution	8-bit signed
Processor	3xCORDIC
Univariate Operations	64xMag,Phase
Bivariate Operations	32xPhase diff,PLV
Power Dissipation	0.26mW (64-chan. 30Hz band)
Neural Stimulation:	
Type	Biphasic current
Voltage Compliance	2V
Current Matching	1 %
Current Range	10μA-1.0mA
DAC res.	8-bits
Duty Cycle res.	4-bits
Wireless TX:	
Modulation	UWB
Freq. Band	0-1GHz/3.1-10.6GHz
Data Rate	10Mb/s
Power diss.	100μW

B. *Off-Line Early Seizure Detection in Humans*

Results of off-line early seizure detection in human ECoG data from a University of Toronto patient are shown in Fig. 27. For spontaneous seizures in humans the SC BPF center frequency was set to 16 Hz to capture abnormal synchrony at that frequency. The two 16 Hz magnitude outputs both increase early in and during the seizure. The synchrony in the 16 Hz frequency band between the two inputs also increases early in and during the seizure. This trend was observed in multiple patients.

TABLE III
STATE-OF-THE-ART NEURAL RECORDING AND/OR STIMULATION SOCS

Spec.	[28]	[27]	[19]	[18]	[26]	[14]	[25]	[16]	[11]	[22]	THIS WORK
Pwr. Diss.(mW)	-	0.253	7.05	6.0	0.005	0.375	0.077	0.27	6.5	5.03	1.4/1.5
Tech.(μm)	0.18	0.090	0.5	0.35	0.8	0.35	0.18	0.18	0.13	0.13	0.13
Area(mm)^2	25	14.8	16.4	65	18	10.9	6.25	2.7	25	12	12
Supply(V)	1.8	1.0	3.0	3.3	1.8	1.5	1.0	1.8	1.2	1.2	1.2/3.3
# Record Chan.	8	16	32	128	4	4	1	8	96	64	64
Pwr/chan.(μW)	2.5	10.3	75	11	4.5	32.8	4	9	68	6.3	10
Gain(dB)	52	40	67.8	57-60	-	52-66	72	-	56	54-60	54-60
Noise(μV_{rms})	0.91	-	4.4	4.9	1	3.1	1.3	-	2.2	6.5	5.1
f_{L3dB}(Hz)	0.1	0.1	1	1	0.1	0.1	0.5	-	280	10	1
f_{H3dB}(Hz)	100	-	10k	5k	100	12k	100	-	10k	5k	5k
CMRR(dB)	90	-	134	90	80	58	60	-	-	75	78
ADC res./SNDR (dB)	10bit	9bit	PWM	9bit	-	54.7	65	44	60.3	48.5	47.5
SC Filter	LPF	LPF	-	-	-	-	BPF	BPF	BPF	-	BPF
Signal Proc.	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes
FIR Filters	64x	2x	-	1x	-	-	7x48T	1x22T	-	64x16T	64x16T
IIR Filters	-	-	-	-	-	1x1T	-	-	-	-	-
DSP	Classification Proc.	GP RISC	-	Feature Extract	Analog	-	Feature Extract	- Spectral	-	-	Tri-CORDIC
Univariate Operations	SVM	16xMag, 16xSpike	-	1xSpike	4x Mag	4x Spike	1x Mag	-	-	64x Spike	64xMag 64xϕ
Bivariate Operations	-	8xcross corr.	-	-	-	4x Spike	-	-	-	-	32x$\Delta\phi$ 32xPLV
Mag. Floor	-	-	-	-	2μV	-	-	-	-	-	8μV
Closed-loop Stimulation	No	No	No	No	No	Yes	No	Yes	No	No	Yes
# Stim. Chan.	0	0	0	0	0	4	0	64	0	0	64
DAC Res.(bits)	-	-	-	-	-	6	-	7	-	-	8
Compliance(V)	-	-	-	-	-	3.2	-	1.8	-	-	2
Current(mA)	-	-	-	-	-	0-0.1	-	0-0.14	-	-	0.01-1.2
Duty Cycle Res.	-	-	-	-	-	No	-	6-bit	-	-	4-bit
Wireless TX	No	No	Yes	Yes	No	Yes	No	No	No	Yes	Yes
Modulation	-	-	FSK	UWB	-	FSK	-	-	-	FSK	UWB
Date-rate(Mb/s)	-	-	-	90	-	-	-	-	-	1.5	10
TX Pwr.(mW)	-	-	3.3	1.6	-	0.2	-	-	-	3.7	0.1

VI. DISCUSSION

A. Resource Utilization

A summary of experimental results is given in Table II. The power dissipation and area breakdown of the entire SoC are shown in Fig. 28(a) and (b), respectively. The SoC operating in the neural vector analysis mode with the UWB TX on dissipates 1.4 mW for 64-channels or 21.6 μW per channel when running the FIR filters at 7.2 kS/s from a 1.2 V supply. The analog feed-forward path (including biasing) from the LNA to the output of the ADCs dissipates 886 μW or 13.8 μW per channel. The digital adders and registers for the FIR filters, digital controller and the CORDIC processor dissipate 400 μW or 6.25 μW per channel.

The neural stimulator (not inlcuded in Fig. 28(a)) dissipates 1.5 mW from a 3.3 V supply for all 64-channels or 23 μW per channel. This includes the DAC, control logic, V-I converter and output current driver operating with a 1 kHz 50 μ A biphasic current at minimum duty cycle. The neural stimulator is not expected to be active during routine operation of the SoC and thus its power dissipation is not as critical when compared with the recording and signal processing functionalities.

In terms of integration area (excluding routing, IO pads, decoupling capacitors, etc.), the 64 neural recording amplifiers, 64 ADCs and 64 16-tap 12-bit digital adders and registers for the FIR filters each utilize approximately 1/4 of the total active area as shown in Fig. 28(b). The area allocation is well balanced. The large area required by the conventional digital multipliers for implementing 64 16-tap FIR filters is saved as the multiplication is performed within the ADC conversion cycle. Adding 64 channels of neural stimulation only requires additional 6% of area, as the DAC and duty-cycle controller are reused from the ADC. The SC BPF, SC LPF and RC LPF and buffer stage utilize a combined 20% of the area. The phase-synchrony processor requires only 3.5% of the total area due to using a CORDIC-based processor.

B. Comparison to the State of the Art

A comparison with other neural recording and/or stimulation SoCs is given in Table III. This work demonstrates the highest degree of integration among recently published state-of-the-art SoCs by combining 64 recording channels with SC bandpass filtering, 64 stimulation channels, 64 multiplying SAR ADCs, 64 16-tap FIR filters, a tri-core CORDIC processor and a UWB transmitter. It is the first published SoC to compute and monitor neural signals phase and phase synchronization.

It also computes the magnitude or energy in a frequency band of up to 5 kHz across 64-channels. The work in [27], [28], [25] and [26] demonstrate 16, 8, 18 and 4 channels, respectively. These designs also lack a neural stimulator and a wireless transmitter. Even with the high degree of integration the presented design demonstrates comparable power dissipation and area.

The SoC also demonstrates seizure detection and seizure abortion *in vivo* in freely moving rats.

VII. Conclusion

A 0.13 μm CMOS wireless closed-loop neural recording and stimulation SoC is presented. The 12 mm^2 die integrates 64 fully differential recording amplifiers with in-channel bandpass filtering with 64 multiplying SAR ADCs, 64 FIR filters, 64 neural stimulators, a tri-core CORDIC processor, 1 kB of memory and a UWB RF transmitter. It demonstrates the first neural vector analyzer and computes phase synchrony between inputs to trigger a closed-loop biphasic current stimulation. The total power dissipation is 1.4 mW from a 1.2 V supply in the recording mode and 1.5 mW from a 3.3 V supply in the stimulation mode. The system was also characterized *in vivo* and demonstrates seizure detection and abortion in freely moving rodents and off-line seizure detection in humans.

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