Rail-to-Rail-Input Dual-Radio 64-Channel Closed-Loop Neurostimulator

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***Abstract*— A 64-channel 0.13-μm CMOS system on a chip (SoC) for neuroelectrical monitoring and responsive neurostimulation is presented. The $\Delta\Sigma$-based neural channel records signals with rail-to-rail dc offset at the input without any area-intensive dc-removing passive components, which leads to a compact 0.013-mm^2 integration area of recording and stimulation circuits. The channel consumes 630 nW, yields a signal to noise and distortion ratio of 72.2 dB, a 1.13-μVrms integrated input-referred noise over 0.1–500 Hz frequency range, and a noise efficiency factor of 2.86. Analog multipliers are implemented in each channel with minimum additional area cost by reusing the multi-bit current-digital to analog converter that is originally placed for current-mode stimulation. The multipliers are used for compact implementation of bandpass finite impulse response filters, as well as voltage gain scaling. A tri-core low-power DSP conducts phase-synchrony-based neurophysiological event detection and triggers a subset of 64 programmable arbitrary-waveform current-mode stimulators for subsequent neuromodulation. Two ultra-wideband (UWB) wireless transmitters communicate to receivers located at 10 cm to 2 m distance from the implanted SoC with data rates of 10–46 Mb/s, respectively. An inductive link that operates at 1.5 MHz provides power to the SoC and is also used to communicate commands to an on-chip ASK receiver. The chip occupies 6 mm^2 while consuming 1.07 and 5.44 mW with delay-based and voltage controlled oscillator-based UWB transmitters, respectively. The SoC is validated in *vivo* using epilepsy monitoring (seizure detection) and treatment (seizure suppression) experiments.**

***Index Terms*— Analog multiplication, battery-less implant, brain monitoring, closed-loop system on a chip (SoC), dc offset removal, diagnostics, discrete-time front end, epileptic seizure detection, implantable wireless SoC, inductive powering, intractable, *in vivo* experiments, multi-band radio, multiplying analog to digital converter (ADC), neural recording, neural stimulation, phase synchronization, SoC.**

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I. Introduction

CLOSED-LOOP neurostimulation, triggered by the detection of a neurological event, has been demonstrated effective in diagnosis and treatment of various neurological disorders [1]–[5]. We have recently demonstrated that current-mode stimulation upon an accurate time-advanced phase-synchrony-based seizure detection performed on a computer-in-the-loop, renders approximately 83% of subjects seizure-free in a six-month animal study [2].

A general block diagram of a wireless and battery-less closed-loop neurostimulator brain implant is shown in Fig. 1(a). Fig. 1(b) shows an envisioned implantation configuration of the implantable system on a chip (SoC) in the proximity of the brain where it is connected to an array of electrocorticography (ECoG) or surface electrodes. The system communicates recorded physiological data to an external module through a wireless link and receives power and configuration commands through a link enabled by inductive coupling. Accurate capture and efficient control of neurological disorders, such as epileptic seizures that often originate in multiple regions of the brain, requires neural interface microsystems with an ever-increasing need for higher channel count. To realize a small form factor and to avoid damaging brain cells due to over-heating, area and power consumption of each channel must be minimized.

Fig. 2(a) shows a conventional ac-coupled closed-loop neural front end used in recording channels. Different variations of such topology have been reported in many works, such as [6]–[9]. In this topology, the voltage gain is set by C_1/C_2 ratio, where C_1 and C_2 are the input decoupling and feedback capacitors, respectively. The lower 3-dB corner frequency of the amplifier is set by $[1/(C_2 \times R_2)]$, and the decoupling capacitor is placed at the input to block the dc offset voltage. To prevent any significant signal loss in lower frequencies where the majority of disease-related brain activities occur [δ(<4 Hz), θ(4–7 Hz), α(8–15 Hz), and β(16–31 Hz) bands], the lower 3-dB corner frequency of the amplifier should be set to a maximum of 1 Hz. To meet this condition while maintaining a reasonably high voltage gain, and also to keep C_1 in a reasonable range for on-chip implementation, C_2 is

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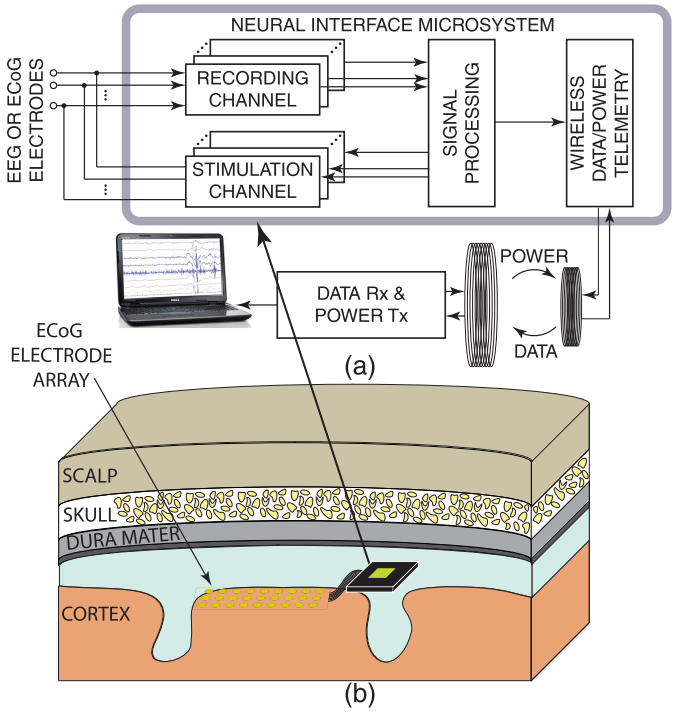

Fig. 1. (a) Block diagram of a wireless closed-loop neurostimulator. (b) Envisioned placement of the wireless neurostimulator in the proximity of the brain and connected to ECoG electrode array.

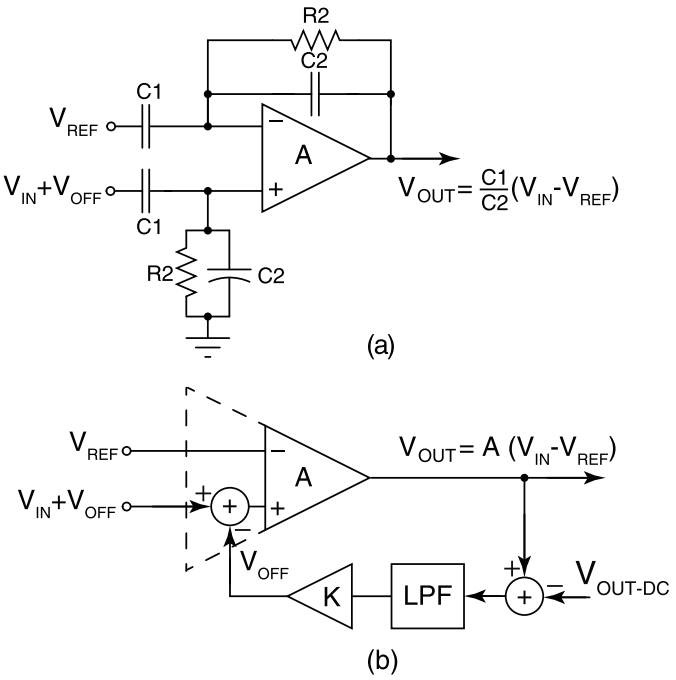

Fig. 2. (a) Conventional ac-coupled and (b) digitally assisted dc-coupled neural amplifiers.

typically chosen to be in the order of 100 fF, which forces R_f to have a very large value (>100 GΩ) [9].

Even with the above-mentioned considerations, C_1 is typically >10 pF and is repeated twice in every channel, which makes it the most significant silicon area consumer in a many-channel neural interface microchip. Additionally, on-chip realization of $a\ >100$ GΩ resistor is another design challenge for recording channels with the ac-coupled closed-loop topology. Area constraints disallow a passive implementation of such large resistors, and reported that active pseudo-resistor implementations (reviewed in [9]) suffer from nonlinear performance when a high-swing signal is applied across them. In addition to the area problem, it has been discussed that ac-coupled neural front ends have major issues with flicker noise, as the conventional noise reduction methods such as chopper stabilization cannot simply be applied to them without degrading input impedance or causing noise multiplication [10].

Mentioned issues that are rooted from the existence of an input decoupling capacitor have motivated the introduction of dc-coupled front ends, in which the decoupling capacitors are removed and the input offset is compensated using a feedback path with low-pass signal transfer function (STF), as shown in Fig. 2(b). The idea is to compare the amplifier's output dc value with a reference and feed the average of the difference (i.e., the error) to the input. The low-pass transfer characteristics realized by averaging in the feedback path will translate into a high-pass one in the main (or feed-forward) signal path. Various implementations of this idea are reported in the literature, however, only dc offset of up to ± 50 mV is removed [10]–[13], and additional area intensive circuits are required to compensate for larger offsets. Moreover, a significant channel-to-channel gain mismatch caused due to the open-loop architecture of the circuits using dc-coupled topology must be eliminated, which requires additional calibration circuits [10].

The rather fundamental shortcomings of the conventional ac and dc-coupled front ends call for a new channel architecture. The architecture must solve the aforementioned issues while meeting the specific design requirements of a neural recording circuit. This paper presents a 6-mm^2 neurostimulator SoC developed in a 0.13-μm CMOS technology. The chip has 64 neural recording/stimulation channels, designed based on a compact power-efficient technology-scalable $\Delta^2\Sigma$-based architecture that allows for recording neural activity in the presence of a rail-to-tail input dc offset. Oversampling and input device sizing techniques are used to minimize the input-referred thermal noise, while correlated double-sampling is employed in each channel to suppress the flicker noise.

A mixed-mode analog–digital compact multiplier is implemented in each channel to perform voltage gain scaling as well as finite impulse response (FIR) filtering. A multi-core digital processor, shared between all the channels, is used to carry out signal feature extraction and epileptic seizure detection. The chip also has 64 programmable arbitrary-waveform bi-phasic current-mode stimulators that are triggered by the on-chip digital processor upon detection of a neurological event to modulate the brain activity. Two ultra-wideband (UWB) wireless transmitters are included in the design that enable communication of diagnostic data to a wide range of distances. The chip is powered wirelessly using a magnetic inductive link, with energy signals that are amplitude shift-keyed to

communicate configuration commands to the chip. The SoC is validated in an *in vivo* epilepsy monitoring (seizure detection) and treatment (seizure suppression) experiment. This paper extends on an earlier report of the principle and demonstration in [14], and offers a more detailed analysis of the design and additional experimental results characterizing the circuit implementation and *in vivo* validation.

The rest of this paper is organized as follows. Section II discusses the feasibility and possible design tradeoffs of a discrete-time front end for neural recording. Section III describes the presented channel architecture, and discusses the circuit implementation of the key functional blocks in the SoC. Section IV discusses the VLSI architecture of the neurostimulator SoC, and the implementation of system-level resource sharing schemes. Section V presents electrical experimental testing results from individual blocks as well as the full system. Section VI presents *in vivo* online animal epilepsy seizure detection and treatment results and offline human epilepsy seizure detection results. Section VII discusses resource utilization, power and area scalability, and comparison with the state of the art.

II. Discrete-Time Neural Front-End: Feasibility and Tradeoffs

Looking at the conventional front-end architectures summarized in Section I, it can be concluded that the bottleneck in shrinking the size of neural recording channels is mainly rooted from techniques used to remove the input dc offset. The offset removal in ac-coupled front ends [6], [7], [15]–[19] is done by the area-intensive decoupling capacitors, and in dc-coupled ones [10]–[12], is done by a digital low-pass filter that can require a significant silicon area if large offsets are to be removed. This suggests that a new architecture capable of removing the dc offset without a substantial area increase has the potential to be used in many-channel SoCs without introducing scalability constraints.

In this section, we will discuss the feasibility of a discrete-time front end for neural recording from various aspects, including input-referred noise, input impedance, signal-to-noise ratio, bandwidth, and power consumption. We will also consider various tradeoffs that must be taken into account among different system performance specifications. The main idea of a discrete-time front end is to merge the amplification and quantization stages into a single stage: 1) to leverage from the low-cost low-complexity switched-capacitor (SC) techniques for input dc offset removal and 2) to realize an active-component-dominated architecture yielding a technology-scalable area for the channel.

A. Input-Referred Noise

There are three major noise sources at the input of a neural recording circuit: 1) noise that is generated by the recording circuit; 2) the electrode noise; and 3) the background noise. The latter is the term used for the noise that is typically generated from neuronal activity in the proximity of the recording site, and is estimated to be $\simeq 10\mu V_{rms}$. The noise generated by the electrode impedance can be simply expressed as

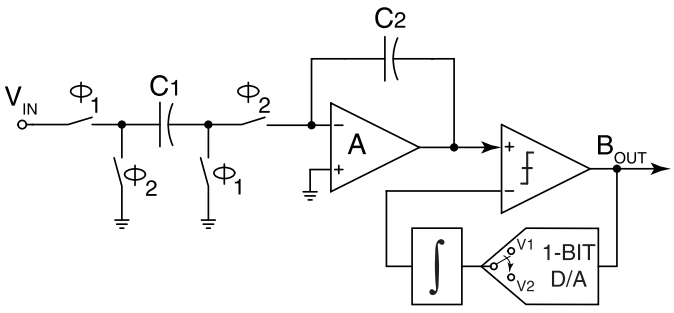

Fig. 3. First-order single-ended input $\Delta\Sigma$ modulator.

$$V_{\mathrm{RMS}} = \sqrt{4kTR\Delta f}. \tag{1}$$

A good neural front-end design must add minimally (e.g., <10%) to the total noise at the input. As a result, its noise power must be less than 1% of the total noise generated by the electrode and the background neural activity. For a discrete-time circuit with a sampling input stage, the input-referred noise can be written as

$$\overline{N_{i1}^2} = \frac{kT}{C_s} \tag{2}$$

where C_s is the equivalent sampling capacitor, k is Boltzmann's constant, and T is the temperature. Therefore

$$0.01(4kTR_{\mathrm{elec}} \cdot \Delta f + N_{i-\mathrm{BG}}^2) > \frac{kT}{C_s} \tag{3}$$

where $N_{i-\mathrm{BG}}^2$ is the background noise power. Based on this equation, a practical value for C_s (e.g., 1 pF) will result in an input-referred noise that is orders of magnitude larger than what can be tolerated. Such a high level of noise appears at the input, because the aliased noise is added to the signal bandwidth during sampling. In other words, wideband thermal noise is folded back to the signal bandwidth and results in higher noise level in this frequency range without changing the total noise. It is shown in [20] that sampling at the input increases the in-band thermal noise level by

$$\pi f_{3\,\mathrm{dB}}/f_s \tag{4}$$

where f_s is the sampling frequency and $f_{3\,\mathrm{dB}}$ is the thermal noise bandwidth. This equation implies that the oversampling could be a possible solution to the input-referred noise problem as it increases f_s by oversampling ratio (OSR). To analyze this quantitatively, let us consider a first-order $\Delta\Sigma$ analog to digital converter (ADC) as shown in Fig. 3. The input-referred thermal noise of this circuit can be written as [20]

$$\begin{aligned}\overline{N_{i1}^2} &= \frac{\overline{V_{ni1}^2}}{f_s/2}\int_0^{f_s/(2\cdot\mathrm{OSR})} |\mathrm{NTF}_{i1}(f)|^2 df \\ &= \frac{\overline{V_{ni1}^2}}{f_s/2}\left[\frac{5f_s}{2\cdot\mathrm{OSR}} - \frac{2f_s}{\pi}\sin\left(\frac{\pi}{\mathrm{OSR}}\right)\right]\end{aligned} \tag{5}$$

where $\overline{V_{ni1}^2}$ is the thermal noise power contribution of the input switches and the amplifier in the input integrator.

Assuming that switches will be implemented with a bigger-than-minimum size to decrease their on resistance, and consequently, make their noise contribution insignificant compared with the amplifier, the noise power of the input integrator can be expressed as

$$\overline{V_{ni1}^2} \simeq 4kT \cdot \eta_f/(3C_s) \tag{6}$$

where η_f is the amplifier topology-dependent noise coefficient. By sizing active load PMOS transistors of the amplifier to have a transconductance considerably smaller than the input NMOS devices, η_f can be minimized (e.g., 1.5 for a telescopic architecture). Equations (5) and (6) suggest that a compact discrete-time neural front-end design is feasible if instead of sampling an area-intensive capacitor (e.g., 1 nF) at the Nyquist rate, we sample an orders of magnitude smaller capacitor (e.g., 1 pF) at much higher rate (e.g., OSR = 1000). However, it must be investigated that other design requirements, such as input impedance, speed, effective number of bits, and power consumption, can still be met with such a high OSR value.

B. Noise-Speed Tradeoff

Generally, a significant increase in sampling frequency of an SC circuit (e.g., an amplifier or integrator) leads to stringent speed requirements. With the increase in the sampling frequency, the operational amplifier used in the body of the SC circuit must settle in a substantially shorter time. If $1/2f_s$ is the period of the sampling clock, τ=$1/(2\pi f_{3\,\mathrm{dB}})$ is the settling time of the system, and N is the target data acquisition accuracy

$$\begin{aligned} e^{\frac{-1}{2f_s\tau}} &< 2^{-(N+1)} \\ \Rightarrow \pi \frac{f_{3\,\mathrm{dB}}}{f_s} &> (N+1)\cdot Ln(2) \end{aligned} \tag{7}$$

where $f_{3\,\mathrm{dB}}$ is equal to

$$f_{3\,\mathrm{dB}} = \frac{\beta g_m}{2\pi C_0} \tag{8}$$

in which

$$\beta = \frac{C_f}{C_s + C_f} \quad \text{and } C_0 = C_L + \frac{C_s C_f}{C_s + C_f} \tag{9}$$

where β is the feedback ratio, and C_L is the load capacitance. By sizing C_s to be much larger (10×) than both C_f and C_L, (7) and (8) are simplified to

$$g_{m,\min} = \frac{2f_s Ln(2)(N+1)}{C_s}. \tag{10}$$

Replacing C_s by its equivalent from (5) and (6) and with the assumption of a very high OSR

$$\begin{aligned} g_{m,\min} &= \frac{2f_s Ln(2)(N+1)\cdot 5kT}{\overline{N_{i1}^2}\cdot \mathrm{OSR}} \\ &= \frac{20(N+1)Ln(2)\cdot kT\cdot f_B}{\overline{N_{i1}^2}} \end{aligned} \tag{11}$$

where f_B is the target frequency bandwidth of the neural signal. Equation (11) shows the tradeoff between total integrated noise ($\overline{N_{i1}^2}$), OSR, resolution (N), and power consumption (g_m). This equation is used as a reference point for $\Delta\Sigma$-based neural front end to relate the targeted noise budget, resolution (number of bits), power budget, and input signal frequency bandwidth.

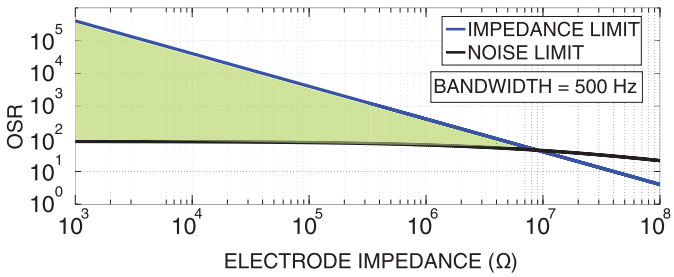

Fig. 4. OSR versus the electrode impedance for ECoG bandwidth. The green area shows the OSR and R_{ELEC} values that satisfy both noise and input impedance requirements.

C. Noise-Input Impedance Tradeoff

High input impedance is one of the main requirements of a neural front end. A commonly accepted value for the Z_{IN} is ten times larger than the electrode impedance, to avoid loss of signal [21]. For a discrete-time front end, (5) and (6) encourage increasing of C_s and OSR to suppress the input-referred noise. However, increasing the two cannot be done indefinitely due to a twofold reason. First, maximum C_s size is set by the area allocated for each channel and should be kept smaller than a certain value, and second, the input impedance of an SC is set by $1/(f_s \cdot C_s)$, with f_s being the sampling frequency, and larger C_s or OSR results in smaller input impedance for the front end.

For the circuit shown in Fig. 3, the input impedance is the equivalent impedance of the SC

$$Z_{\mathrm{IN}} = \frac{1}{f_s \cdot C_s} = \frac{1}{2\cdot \mathrm{OSR}\cdot f_B \cdot C_s} \tag{12}$$

where f_s is the sampling frequency, f_B is the input signal bandwidth, and OSR is the oversampling ratio. Based on this equation, to achieve higher input impedance, OSR must be decreased. However, as was shown in (5), decreasing OSR directly increases the front-end input-referred noise, which is undesired. As a result, OSR must be selected in a way that it satisfies both noise and input impedance requirements. Combining (3), (5), and (6), we have

$$0.01(4kT R_{\mathrm{elec}}\cdot \Delta f + N_{i-\mathrm{BG}}^2) > \frac{4kT\cdot \eta_f}{3C_s\cdot \mathrm{OSR}} \tag{13}$$

also, to satisfy input impedance requirement

$$Z_{\mathrm{IN}} = \frac{1}{2\cdot \mathrm{OSR}\cdot f_B \cdot C_s} > 10R_{\mathrm{elec}}. \tag{14}$$

Using (13) and (14), a lower and a higher limit for OSR is found based on the electrode impedance. Fig. 4 shows the OSR versus the electrode impedance for ECoG signal bandwidth. The area highlighted in green is the range of OSR values that can satisfy both noise and input impedance requirements as defined by (13) and (14). As shown, for ECoG signals, with the bandwidth of 500 Hz, the circuit

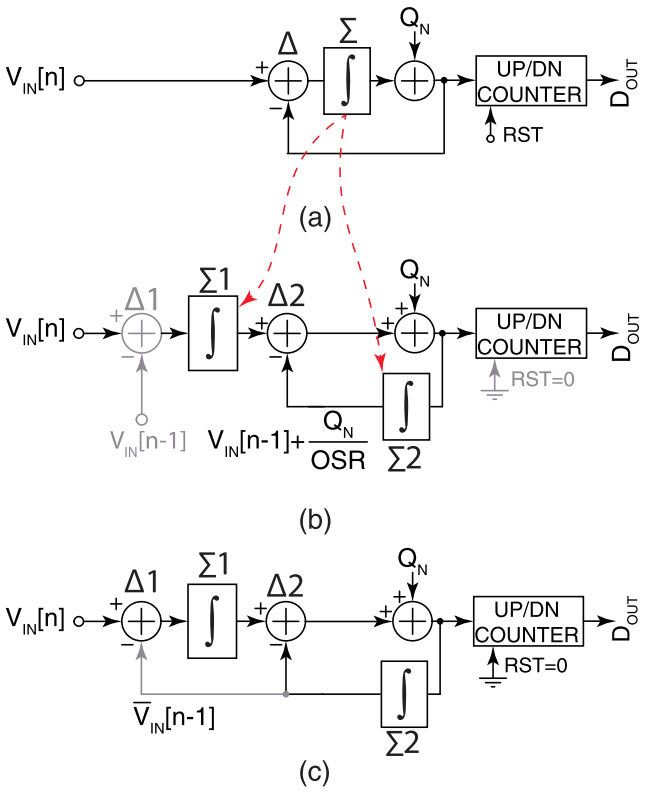

Fig. 5. Incremental evolution of the block diagram of $\Delta^2\Sigma$-based neural recording channel. (a) First-order $\Delta\Sigma$-based ADC. (b) First-order $\Delta\Sigma$-based with an additional differentiating stage at the input. (c) Self-contained $\Delta^2\Sigma$-based ADC.

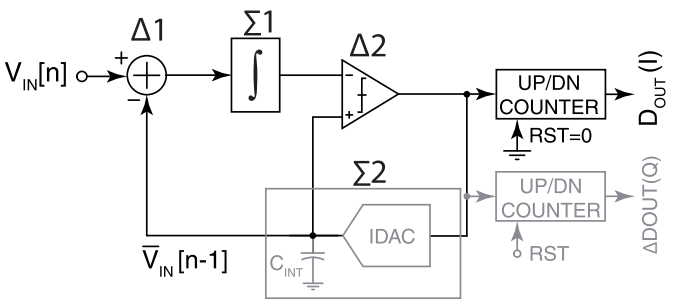

Fig. 6. Single-ended $\Delta^2\Sigma$-based neural recording channel with quadrature outputs.

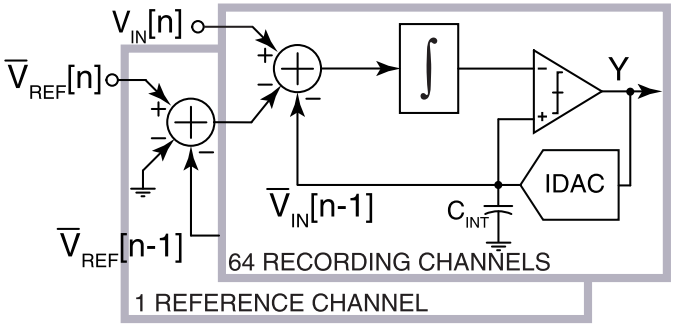

Fig. 7. 64 differential $\Delta^2\Sigma$-based neural recording channels.

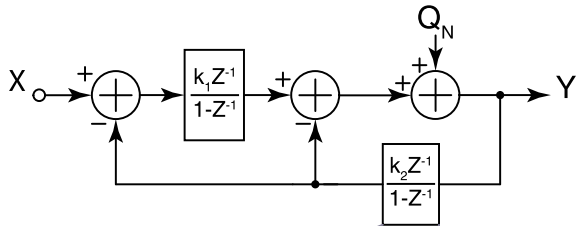

Fig. 8. First-order $\Delta^2\Sigma$ modulator with z-domain transfer functions of the blocks.

satisfies both noise and impedance requirements up to an electrode impedance of 10 MΩ. The electrode impedance for the recording electrodes depends on both the material used to build the electrode and the size of recording sites.

III. Discrete-Time Neural Recording/Stimulation

A. Rail-to-Rail Front-End Architecture

Fig. 5(a) shows a conventional first-order $\Delta\Sigma$ modulated ADC. As discussed in Section II-C, with a careful design that is governed by (11), (13), and (14), this circuit can satisfy noise, input impedance, bandwidth, and power requirements of a neural recording front end. However, it still cannot be used as a neural front end as it gets saturated with any dc offset at the input. In Fig. 5(b), the input integrator (Σ) is split into two integrators ($\Sigma 1$ and $\Sigma 2$) that are placed earlier in the signals paths. Also, to avoid saturation, a Δ stage is added in front of the $\Delta\Sigma$ modulator to subtract two consecutive samples, $V_{\rm IN}[n]$ and $V_{\rm IN}[n-1]$. The quantized difference is later integrated by a non-resettable up/down counter. Fig. 5(b) also shows that since the input of $\Sigma 2$ is equivalent to the signal derivative, the previous sample plus the ADC quantization noise, $V_{\rm IN}[n-1]+Q_N/{\rm OSR}$, is reconstructed at the output of the feedback integrator, $\Sigma 2$. As a result, connecting this node (output of $\Sigma 2$) to the subtracting input of $\Delta 1$ will form a single-input single-output $\Delta^2\Sigma$ ($\Delta+\Delta\Sigma$) modulator as shown in Fig. 5(c).

Due to the additional Δ stage at the input, the output bit-stream of the $\Delta^2\Sigma$ ADC represents the signal derivative; therefore, a non-reset counter (shown in Fig. 5) is used to integrate the bit-stream while decimating it. Fig. 6 shows that by adding a reset counter to the $\Delta^2\Sigma$ modulator, the signal is only decimated without being integrated, and the output bit-stream represents the signal derivative that has a natural 90° phase difference with reference to the signal. As a result, by adding a single counter (instead of multi-tap all-pass and Hilbert filters [8], [10]), two quadrature outputs, I and Q, can be obtained and later used in signal's phase calculation.

Fig. 7 shows the differential implementation of the 64 differential recording channels. To eliminate the effect of common mode (CM) noise, the input signal derivative is subtracted by the respective reference signal derivative, calculated by the reference channel, which is the only channel on the chip with a single-ended input. The presented in-channel neural ADC records intracranial EEG signal with an arbitrary rail-to-rail dc level, different for each of the 64 channels.

B. In-Channel Multiplication

Fig. 8 shows the $\Delta^2\Sigma$ ADC block diagram, where the Σ blocks are replaced with a generic delaying integrator's

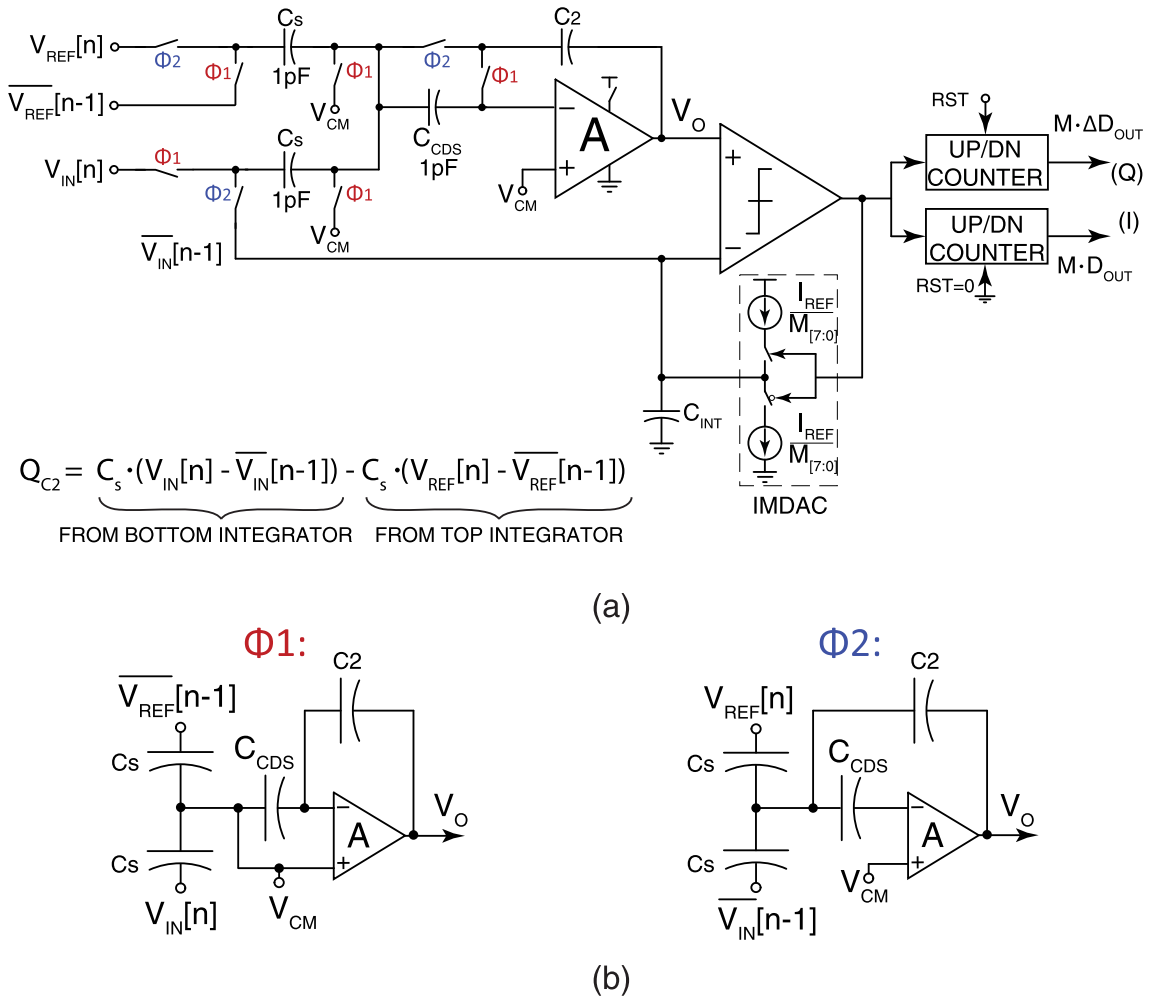

Fig. 9. (a) Simplified circuit diagram of the $\Delta^2\Sigma$-based neural recording front end with correlated double-sampling, quadrature output, and in-channel mixed-mode multiplication. (b) Simplified circuit schematic showing the differential subtracting input integrator configuration during two main phases of operation.

z-domain transfer function. In the figure, k_1 and k_2 represent the gain of each integrator. STF of this system can be written as

$$\left|\frac{Y(z)}{X(z)}\right| = \left|\frac{k_1(z-1)}{(z-1)^2 + k_2(z-1) + k_1 \cdot k_2}\right| \tag{15}$$

where z is equal to

$$z = e^{j\omega T_s}. \tag{16}$$

Considering that $\omega = 2\pi f$, with f being the input signal frequency, and defining f_b as the Nyquist bandwidth, we will have

$$\begin{aligned} &\omega = 2\pi f_b/n, \quad 1 < n < \infty \\ &\Rightarrow j\omega T_s = \frac{j\pi}{n \cdot \text{OSR}} \\ &\Rightarrow z = e^{j\omega T_s} = \cos\left(\frac{\pi}{n \cdot \text{OSR}}\right) + \text{jsin}\left(\frac{\pi}{n \cdot \text{OSR}}\right). \end{aligned} \tag{17}$$

For a very large OSR, which is necessary as discussed in Section II-A, we can simplify (17) to

$$z = e^{j\omega T_s} = 1 + \frac{j\pi}{n \cdot \text{OSR}}. \tag{18}$$

Replacing z in (15) with the expression in (18)

$$\left|\frac{Y(z)}{X(z)}\right| = \left|\frac{k_1\left(\frac{\pi}{\text{OSR}}\right)}{\left(\frac{\pi}{\text{OSR}}\right)^2 + k_2\left(\frac{\pi}{\text{OSR}}\right) + k_1 \cdot k_2}\right| \cong \frac{\pi}{n \cdot k_2 \cdot \text{OSR}}. \tag{19}$$

Equation (19) shows that for large OSR values, the feedback integrator's coefficient has an inverse linear relationship with the magnitude of the digital output of the data converter. On the other hand, as shown in Fig. 6, the feedback integrator is basically a current digital to analog converter (DAC) that pumps charges into an integrating capacitor. Therefore, by using a multi-bit DAC, we can set an arbitrary amount of charge to be pumped into the capacitor, hence, control the gain of the integrator, and consequently, multiply an arbitrary number to the input signal. This means that analog multiplication with N-bit resolution can be done by adding an N-bit current-mode DAC to each channel. We will discuss in Section IV that the analog multi-bit multiplier is used to construct area- and power-efficient digital filters in the DSP backend.

The presented analog multiplier leads to significant saving in the area compared with a digital alternative, but what makes

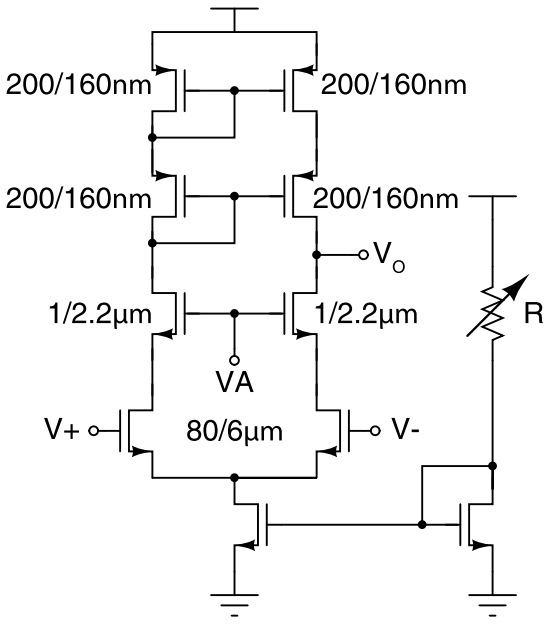

Fig. 10. Simplified schematic of the amplifier used for the input integrator.

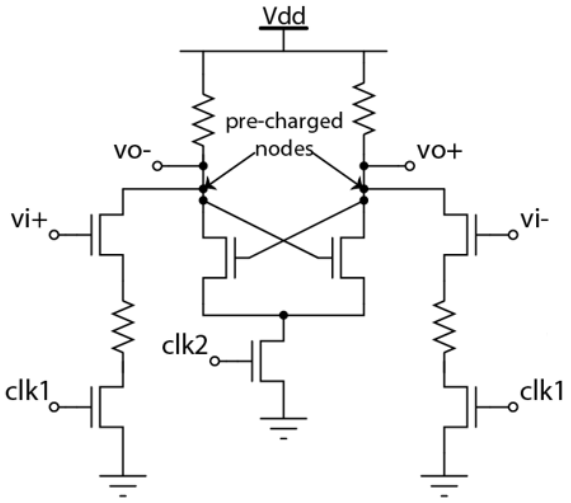

Fig. 11. Simplified schematic of the dynamic comparator used in the neural front end.

it especially advantageous for closed-loop neurostimulators is the fact that every channel already houses a multi-bit current-mode DAC for electrical charge stimulation [10], [14], [22], [23]. Without the proposed analog in-channel multiplier, during recording and signal processing, this DAC remains unused. Therefore, by using a multiplexer, the DAC can be programmed to either be used as a current-mode pulse generator during stimulation, or as a part of a multiplying ADC during recording. This way, the N-bit multiplication comes at almost no extra cost in terms of silicon area.

C. Neural Front-End VLSI Implementation

The transistor-level implementation of the recording channel circuit is shown in Fig. 9. Positive-gain and negative-gain parasitic insensitive integration are used to implement the Σ stage of the $\Delta\Sigma$ modulator for the input and reference signals, respectively. In each clock cycle, one integrator pulls and the other pushes charge to the shared accumulating capacitor (C2), resulting in differential integration. During $\Phi 1$, the two sampling capacitors (C_s) are charged to $V_{\rm IN}[n]-V_{\rm CM}$ and $V_{\rm REF}[n-1]-V_{\rm CM}$, respectively. During $\Phi 2$, the common terminal of the two C_s remains at the same voltage ($V_{\rm CM}$), but the other terminals change to $V_{\rm IN}[n-1]$ and $V_{\rm REF}[n]$, respectively. As a result, the lower branch pulls a charge equal to $C_s \times (V_{\rm IN}[n]-V_{\rm IN}[n-1])$ and the upper branch pushes a charge equal to $C_s \times (V_{\rm REF}[n-1]-V_{\rm REF}[n])$. The charges are added and integrated on C_2 thus implementing subtraction of the two derivatives and integration $\Sigma 1$. A simplified schematic of the amplifier and the low-power dynamic comparator are shown in Figs. 10 and 11, respectively.

Correlated double sampling is implemented using $C_{\rm CDS}$ and one extra switch to remove the flicker noise and offset of the two-stage 10T amplifier A. $C_{\rm CDS}$ samples the amplifier input offset and $1/f$ noise during $\Phi 1$, and keeps the common terminal of the two C_s at $V_{\rm CM}$ during $\Phi 2$. To prevent the CDS technique from hampering the noise performance of the front end, the amplifier input devices are sized to have minimum parasitic capacitance while their transconductance as high as possible. This ensures that a $C_{\rm CDS}$ of 1 pF is significantly larger that the input parasitic capacitance of the amplifier, which results in effective flicker noise suppression [24].

D. Current-Mode Stimulators

Each channel is equipped with a neural stimulator that generates arbitrary-waveform current-mode pulse-train. The stimulator circuit, shown in Fig. 12, is comprised of two segments of 4-bit binary-weighted programmable push/pull current sources. The segments are biased using two current references different by a factor of 16 for a total of 8 bits of resolution. Thick-oxide transistors are used to be able to increase the stimulator voltage compliance up to 3.3 V. Also the minimum current ($I_{\rm LSB}$) is programmable, which allows for changing the minimum/maximum stimulation current for different applications.

IV. System VLSI Architecture

Fig. 13 shows the system VLSI architecture of the fabricated responsive neurostimulator SoC. It includes 64 closed-loop neurostimulator channels, a low-power DSP with compact 64-tap mixed-signal FIR filters, UWB transmitters, and an inductive command and power receiver. The on-chip DSP calculates the phase synchrony among channels to detect an upcoming epileptic seizure. In short, the algorithm computes a phase locking index as a quantitative representation of phase synchronization among neural signals acquired from pairs of recording channels. To do this, first, an in-phase and a quadrature-phase version of the signal must be obtained. This is conventionally done using Hilbert and all-pass filters both implemented digitally using multi-tap FIR filters. In this paper, since our presented channel already generates such quadrature-phase outputs, these area- and power-hungry multi-tap filters are not required. Then, the signals are filtered to the band

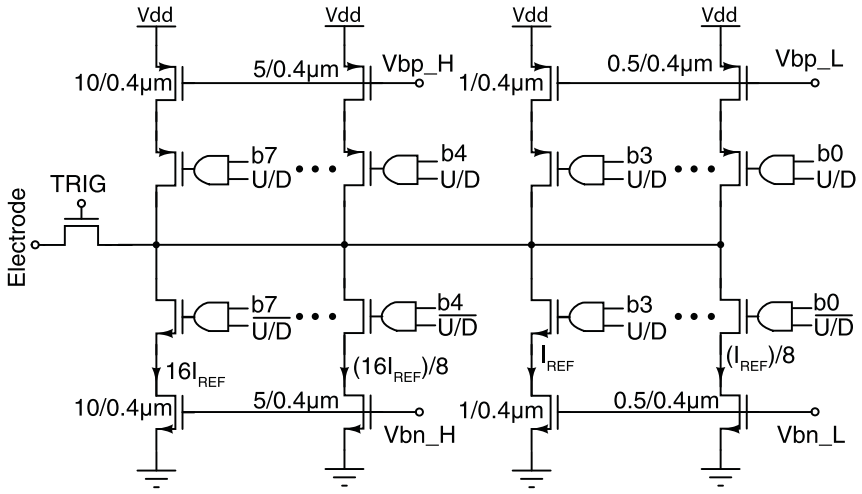

Fig. 12. Simplified circuit schematic of the 8-bit current-DAC used for current-mode stimulation as well as in-channel multiplication.

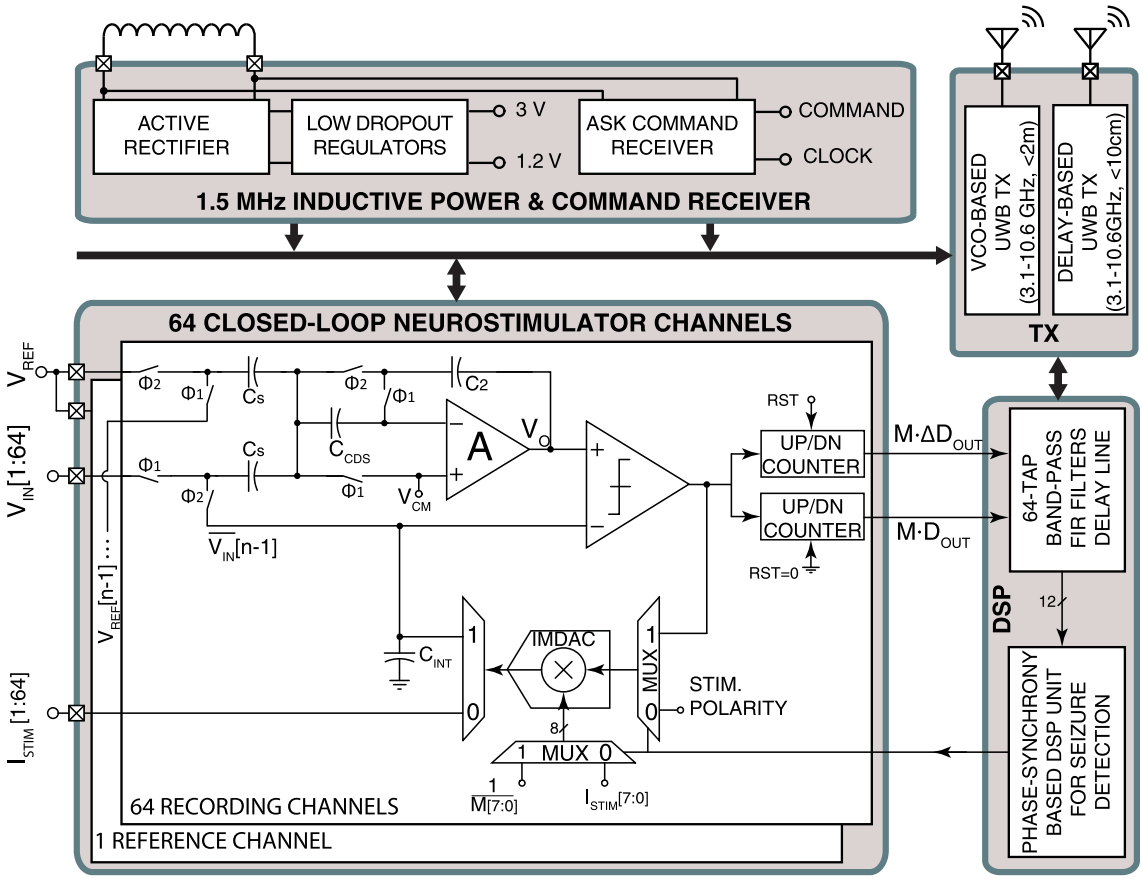

Fig. 13. Simplified functional diagram of the presented neurostimulator SoC and peripheral blocks.

of interest (using the area-efficient mixed-mode analog-digital band-pass filters (BPFs) implemented using analog in-channel multipliers as discussed in Section III-B) and their magnitude, instantaneous phase, and phase difference are computed. Finally, the mean phase coherence that is introduced in [29] is evaluated between two arbitrarily selected channels.

Once a detection is made, an arbitrary-waveform current-mode stimulation is applied to a subset of the stimulation electrodes with a spatio-temporal profile specifically chosen for a given subject. In each neurostimulator channel, the I-mode multiplying DAC utilized in the neural recording $\Delta^2\Sigma$ ADC is reused for current-mode stimulation (at a different programmable bias point) in a time-multiplexed fashion. Thus, arbitrary-waveform stimulation enabled by analog–digital multiplication is performed at almost no extra area cost, and 64×64-tap power-hungry and

TABLE I
COMPARISON OF DIFFERENT IMPLEMENTATIONS FOR 64 64-TAP FIR FILTERS

Spec.	64x32 Digital Multipliers	*64x1 Digital Multipliers	This Work
Power Diss. of Mult.	$2048\times P_{Mult}$	$64\times32\times P_{Mult}$	0
Power Diss. of ADC	$64\times P_{ADC}$	$64\times P_{ADC}$	$64\times32\times P_{ADC}$
Power Diss. of Add./Reg.	$64\times P_{Add,reg}$	$64\times P_{Add,reg}$	$64\times P_{Add,reg}$
Area of Mult.	$2048\times A_{Mult.}$	$64\times A_{Mult.}$	0
Area of Add./Reg.	$64\times A_{Add,reg}$	$64\times A_{Add,reg}$	$64\times A_{Add,reg}$
Power Diss.	$2048\times P_{Mult.}$+$64\times P_{ADC}$ +$64\times P_{Add,reg}$	$64\times32\times P_{Mult}$+$64\times P_{ADC}$ +$64\times P_{Add,reg}$	$64\times32\times P_{ADC}$ +$64\times P_{Add,reg}$
Est. Power Diss. (mW)	2.79	2.79	1.45
Total Area	$2048\times A_{Mult.}$+$64\times A_{Add,reg}$	$64\times A_{Mult.}$+$64\times A_{Add,reg}$	$64\times A_{Add,reg}$
Est. Area (mm^2)	78.53	7.1	4.8
Power$\times$Area	219.1	19.8	6.96

Note: $A_{Mult.}$=0.036mm^2, $A_{Add,reg}$=0.075mm^2, $32\times P_{ADC}$=4.16μW, $P_{add,reg}$=18.5μW, $P_{Mult.}$=0.78μW
*Additional area and power dissipation required for memory.

area-inefficient digital multipliers are avoided. The recorded intracranial ECoG data and status signals are also transmitted out transcutaneously. One low-power delay-based short-range transmitter [25] and one voltage controlled oscillator (VCO)-based long-range UWB transmitter [26] are used to communicate data to on-skin wearable receivers ($d < 10$ cm) and indoor stationary receiver ($d < 2$ m), respectively. Energy is received by a single coil through a multi-coil cellular inductive link at 1.5-MHz frequency [10], [27]. An ASK demodulating command receiver reuses the same inductive link to recover transmitted commands and the clock.

In the seizure detection mode, a high-Q bandpass filter is required. FIR architecture is preferred over IIR due to its linear phase response (hence, maintaining signal's phase) as well as its lower sensitivity to process variations. Based on our MATLAB simulations, for an FIR filter, 64 taps are enough for excellent band-selecting performance. A conventional implementation of this filter requires 64 multi-bit digital multipliers for each recording channel. This number can be reduced by half when there is symmetry in the filter coefficients ($|M_i| = |M_{63-i}|$ for i=0,1,...,63) so only 32 filter coefficient absolute values are utilized in the multiplication. By taking advantage of in-channel mixed-mode multipliers, a bank of 32 adjacent channels is used to implement this computation in parallel. We have previously shown the idea of compact FIR implementation using in-channel multipliers of SAR ADCs [8]. A similar sharing scheme is utilized here, where at each sample, all the 32 channels are connected to one of the electrodes using a 32-to-1 multiplexer. Each ADC output is fed to two slices of the 64-tap add-and-delay line; 32 add-and-delay lines corresponding to the 32 input channels are clocked cyclicly by the on-chip digital controller. A counter output is synchronized with the ADC sampling clock and cycles the output of the neural recording front end and its corresponding FIR filter clock.

It should be noted that if all the 32 channels sample at the same time from a single electrode, the overall input impedance will be degraded significantly. However, in this design, to avoid input impedance degradation, we leveraged the fact that the sampling clock in each channel ($\phi1$) could be programmed to have a duty cycle as low as $<1\%$. Therefore, when the chip was switched to the FIR mode where the in-channel mixed-mode multipliers are used, a time-multiplexed sampling fashion is employed in a way that at any time, although 32 of the channels were connected to a single electrode, only one of them is sampling from the electrode. In this way, the sampling frequency remains the same, which means that the input impedance of each channel stays the same.

The time-multiplexed sampling does not lead to any significant phase error in the signal due to the high OSR used in this architecture, as well as low input signal frequency bandwidth (i.e., <500 Hz). In other words, when we consider the slowly varying neural signal together with a sampler with OSR $>$ 100, the 32 consecutive samples of the same electrode could be assumed the same. This is confirmed by our experimental measurements showing practically no signal loss due to impedance degradation when the chip is switched from simple monitoring mode to monitoring + detection mode.

Table I compares three methods for implementing 10-bit 64-tap FIR filters in terms of area $\times$ power efficiency. The first method, uses 32 10-bit digital multipliers per filter, which results in 2048 (32 $\times$ 64) 10-bit multipliers for 64 channels. The second method shares one 10-bit digital multiplier for all the taps in a filter and clocks it 64 times faster, which results in a more compact design, but has significantly

higher dynamic power consumption and requires additional memory cells for the filter coefficients. The third method, which uses the presented mixed-mode multiplication idea, is to take advantage of in-channel analog multipliers by using a bank of 32 adjacent channels. To maintain the same output data-rate, channels are clocked 32 times faster, hence having higher-than-normal power consumption. As presented, the mixed-mode multiplication results in 31.5× lower power-area product compared with the filter with 64 multipliers, and 2.84× compared with the case with one over-clocked multiplier.

V. Experimental Results

Fig. 14(a) shows the micrograph of the neurostimulator SoC. The chip is designed and fabricated in a 0.13-μm CMOS technology and is sized 2.6 × 2.3 mm^2. It has two power supplies of 1.2 V for neural recording and 3.3 V (2.5 V, when powered wirelessly) for current-mode stimulation. The floor-plan of each channel is shown in Fig. 14(b). Thanks to removing large input passive components and the compact architecture of $\Delta^2\Sigma$ ADC, the channel only occupies 0.013 mm^2. As illustrated, each channel houses a recording neural multiplying ADC, a current-mode stimulator, two up/down counters for quadrature decimation, and a memory that stores multiplication coefficients and stimulation signal properties.

A. Mixed-Signal Front End

Fig. 15 shows the experimentally measured data for the neurostimulation channel. Fig. 15(a) shows the FFT of the ADC output with 130-Hz input sampled with an OSR of 1000, which yields a signal to noise and distortion ratio of 72.2 dB. Fig. 15(b) shows the input-referred noise without and with correlated double sampling, measured to be 8.19 and 1.13 μVrms, respectively, when integrated over 0.1–500 Hz ECoG frequency band. This results in a noise efficiency factor of 2.86 for the whole front end (amplifier + ADC). Fig. 16 shows the discrete-time front-end common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) versus rail-to-rail input dc offset variations. As shown, unlike [10], the channel presented here has a steady performance that is almost independent of the dc offset. We believe that this is mainly because, in [10] (and generally other digitally assisted dc-coupled front ends), the digital feedback path compensates the dc offset by forcing an imbalance to the input differential gain stage biasing. As such, the larger offset results in a need for larger imbalance, which could have less precision than a small imbalance. On the other hand, for the channel presented here, the input dc offset is rejected due to the Δ stage at the input, which acquires the derivative of the signal rather than its magnitude.

We also measured the channel-to-channel crosstalk by grounding the inputs of all channels except one. The single non-grounded channel was connected to a large (150 mV_{p-p}) input at 130 Hz. We performed the experiment on eight random channels and the results showed a maximum of −78 dB crosstalk for the neighboring channels.

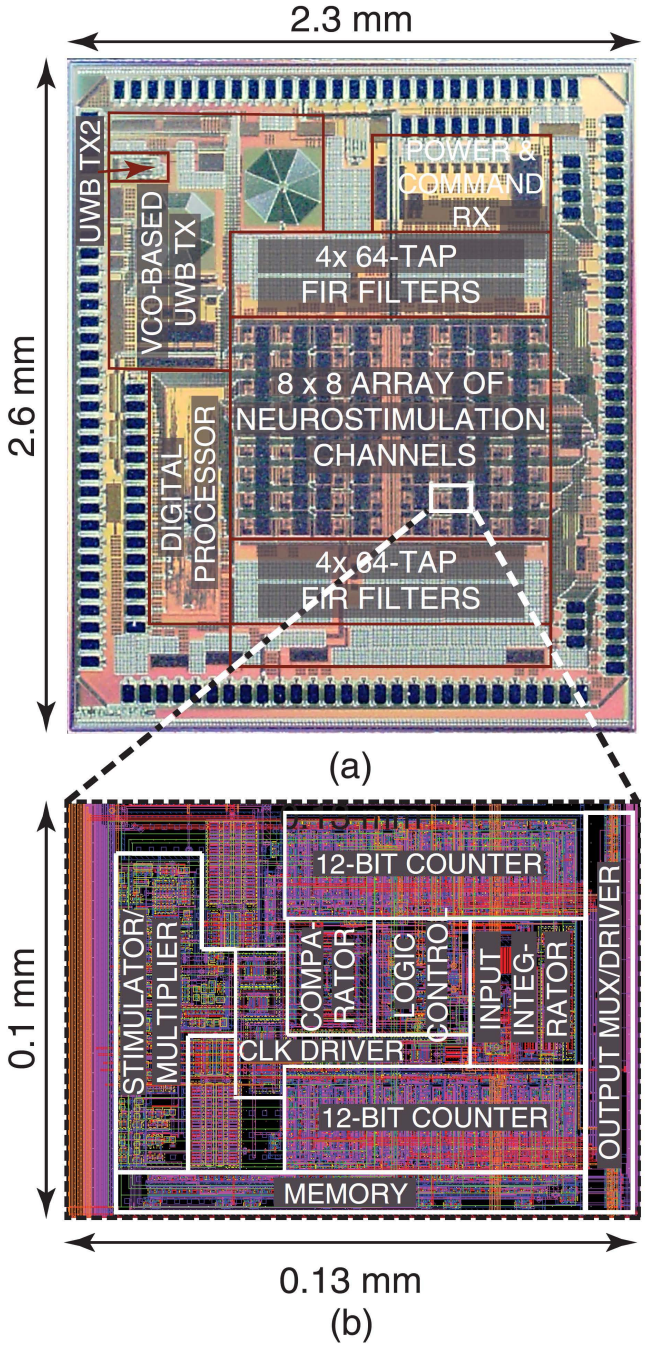

Fig. 14. (a) Micrograph of the SoC with major blocks labeled. (b) Floor plan of the neural recording/stimulation channel.

Fig. 15(c) shows three examples of waveforms generated by the arbitrary-waveform current-mode stimulator with a 1-kΩ load. The neurostimulator is capable of generating current-mode pulse trains with an arbitrary waveform (8-bit accuracy). The stimulator is designed to generate both monophasic and biphasic current pulses with a maximum voltage compliance of 3.1 V. The current amplitude ranges from 10 μA to 1.35 mA.

Charge balancing of the stimulator is also another important concern to avoid tissue or cell damage due to charge accumulation in long-term stimulation. Since large dc-blocking capac-

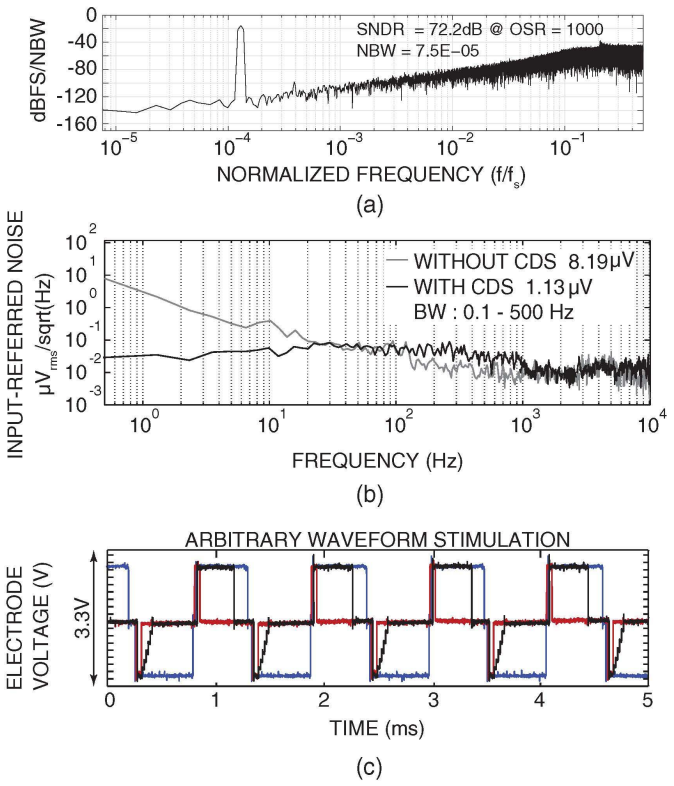

Fig. 15. Experimentally measured results for the neurostimulator channel. (a) Power spectral density of the neural ADC with 130-Hz input. (b) Input-referred noise with and without correlated double sampling. (c) Neural stimulating current into a 1-kΩ load for different pulse shapes and duty cycles.

itors are avoided in this paper, we used an electrode shorting method to ensure residual charges are exhausted completely. It is known that the degree to which shorting is effective depends greatly on the initial charge imbalance. In both design and layout of the current-mode stimulator, matching considerations were taken into account, which yielded an experimentally measured matching of $<1\%$. Such small initial mismatch, along with the small time constant of the path, results in a short discharge period.

At the end of each stimulation episode, residual charges that are accumulated at the stimulation site due to mismatches between sourcing and sinking stimulus currents ($<1\%$) are exhausted by connecting the channel output to a line with VDD/2 voltage. To measure the responsiveness and effectiveness of this method, we programmed the stimulator to generate an unbalanced biphasic pulse with 50-μA amplitude for both the anodic and cathodic phases, and with 80- and 120-μs durations, respectively. Through multiple repetitions, we observed that the residual charge for the imbalance is canceled in less than 4 μs.

B. Mixed-Signal FIR Filter and Digital Backend

Fig. 17(a) shows the frequency response of the 64-tap FIR filter when it is programmed to perform bandpass filtering with three different center frequencies. As shown, with a sampling rate of 80 S/s, the 64-tap filter yields a high selectivity for center frequencies of 10, 20, and 30 Hz. Fig. 17(b) shows a

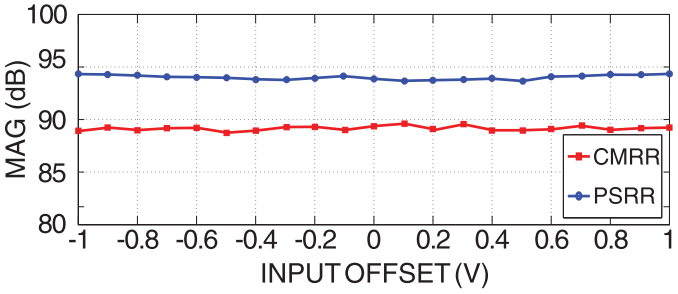

Fig. 16. Experimentally measured front-end CMRR and PSRR versus rail-to-rail input dc offset variations.

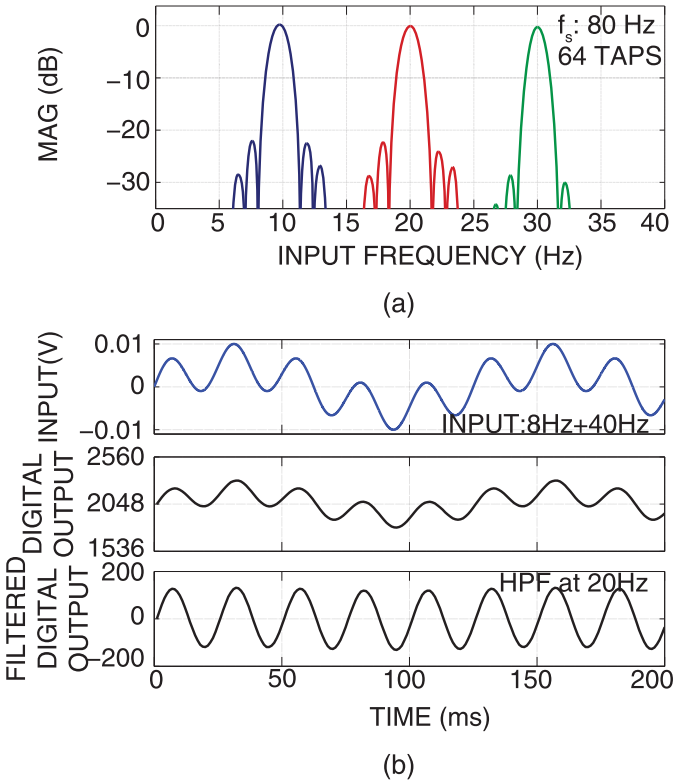

Fig. 17. (a) Experimentally measured frequency responses of the programmable FIR filter for different center frequencies. (b) Example of the FIR filter performance for a two-tone input (8 and 40 Hz) and the FIR being programmed as a high-pass filter with a pole at 20 Hz.

two-tone input comprised of 40- and 8-Hz signals. The digital output shows that the neural ADC captures both the signal and the low frequency drift. To remove the low-frequency component, the FIR filter is programmed as a high-pass filter with a corner frequency of 20 Hz. The digital output after filtering is shown in the bottom of Fig. 17(b). Fig. 18(b) shows the quadrature outputs of the channel for a multi-tone input shown in Fig. 18(a). The phase error compared with the ideal 90° phase difference and the calculated phase using the on-chip processor is also shown in Fig. 18(c) and (d), respectively.

C. Wireless Radio, and Inductive Powering

Two wireless transmitters were tested experimentally with receivers located in different distances from the SoC. For both

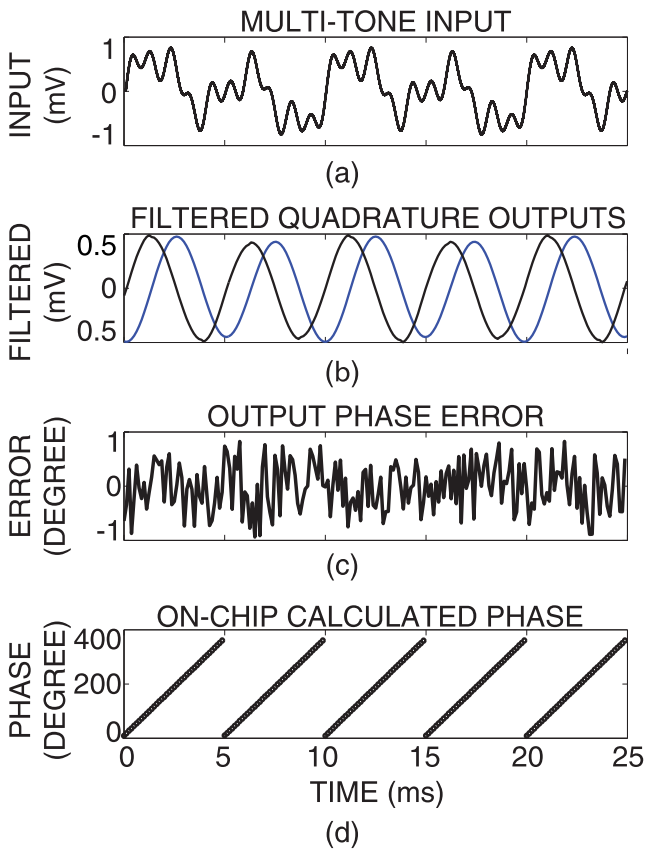

Fig. 18. (a) Experimentally measured input multi-tone sinusoidal signals. (b) Reconstructed output of the FIR bandpass filter programmed at 200 Hz for both in-phase and quadrature signals. (c) Quadrature output phase error with reference to ideal 90°. (d) 8-bit phase output of the on-chip processor.

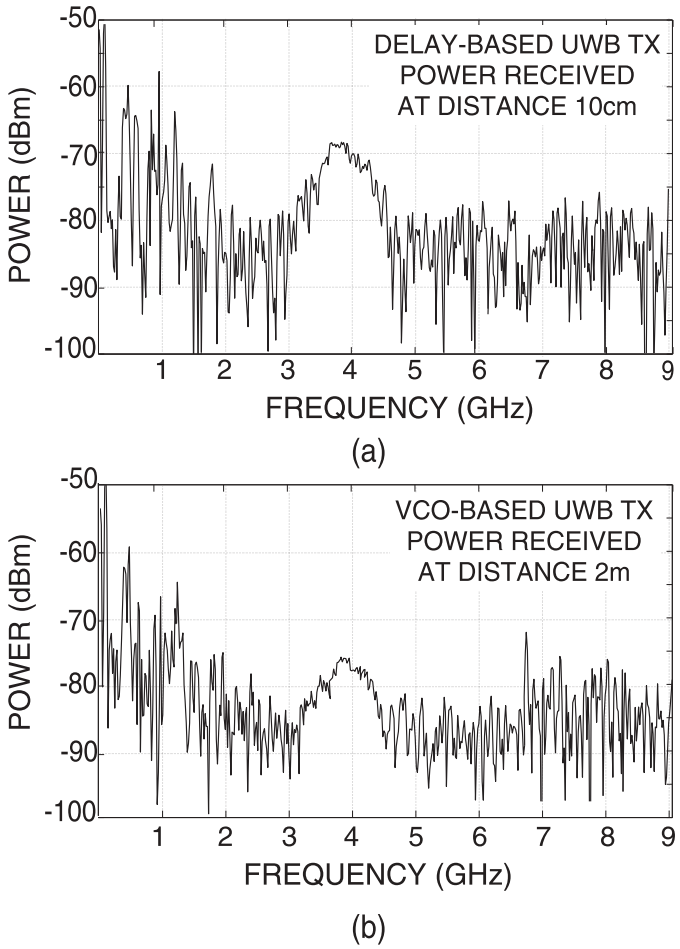

Fig. 19. Experimentally measured received pulse spectrum for (a) delay-based and (b) VCO-based UWB transmitters [26].

transmitters, a custom receiver board was used and placed in 10-cm and 2-m distances. Fig. 19(a) and (b) shows the power spectral density of the short- and long-range UWB transmitters, respectively.

For the short-range transmitter, the experimental measurements show a maximum of 10 Mb/s data rate at 10 cm that promises a high-throughput link for short-distance communications to a wearable on-skin receiver. Higher data-rate and longer transmission range are achieved using the VCO-based UWB transmitter, in cost of higher power consumption. The experimental results show a maximum of 46 Mb/s measured at a maximum distance of 2 m from the SoC. The bit error rate (BER) of the delay-based transmitter is tested by feeding 1-Mb pseudo-random binary sequence data stream to the on-chip transmitter and capturing the received data on the Agilent DSO-X 92004A oscilloscope with a deep memory. No error was observed for the mentioned data length for antenna separation of up to 10 cm, which yields a maximum BER of 10^{-6}.

The inductive power/command receiver is designed to work with an inductive powering system, previously reported by our group [27]. For the inductive transmitter, the load current is optimized for the highest power transfer efficiency. At this point, the input impedance of the on-chip active rectifier is matched to the output impedance of the receiver coil. The RX coil receives a signal with an amplitude limited to 3 V [27], which is converted to a noisy dc signal at 2.9 V with 70-mV ripple at the output of active on-chip rectifier. The output of rectifier is fed to on-chip low drop-out regulator with steady 2.5- and 1.2-V dc outputs, both with less than 5-mV ripple at all time, which only limits the system from recording signals with lower than 0.1-μV amplitude, considering the front-end high PSRR. These voltages are used as reference inputs to the eight-output 8-bit voltage DAC, to generate biasing voltage on the chip.

The inductive powering link was validated experimentally using the coil with electrical and physical specifications reported in Table II, and could deliver up to 10 mW to the implantable chip with a maximum coil separation of 15 cm, while the link was operating at 1.5 MHz and using air as medium. These numbers are expected to be smaller when the coil is implanted. We did not perform the *in vivo* wireless power delivery test.

VI. *In Vivo* Experiments

An on-chip-calculated coordinate rotation digital computer-based phase-synchrony indicator is used for the early detection of epilepsy seizures [29]. The absolute phase and phase synchrony are calculated between pairs of channels and

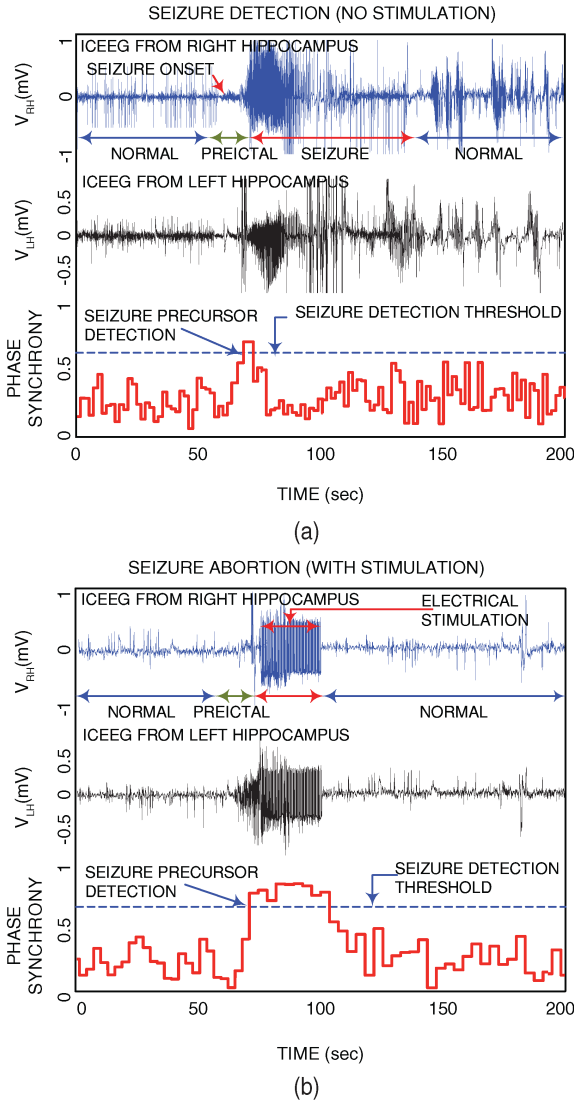

Fig. 20. Experimentally measured seizure detection and control results. (a) Example of seizure detection for the first experiment (no stimulation). (b) Example of a seizure abortion for the second experiment (detection+ SoC-triggered stimulation).

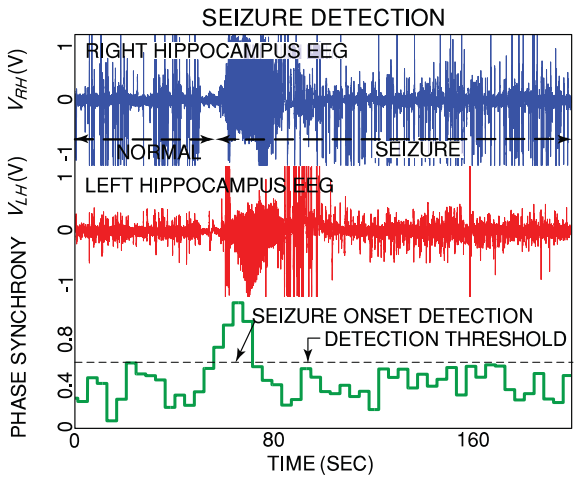

Fig. 21. Example of offline early seizure detection in a human patient.

seizure is detected by applying thresholding on the phase synchrony indicators. Upon detection, a programmable arbitrary-waveform pulse-train is triggered to a subset of 64 current-mode stimulation channels for seizure abortion.

A. In Vivo Early Seizure Detection and Control

The SoC was validated *in vivo* for both detection (experiment 1) and control (experiment 2) of temporal lobe epilepsy (rat model). For this purpose, 4AP was injected intraperitoneally into a Wistar rat to induce recurrent spontaneous temporal-lobe seizures. The animal underwent craniotomy with general anesthesia for electrode implantation. Following the recovery period, the animal was connected to the presented SoC for recording and detection of spontaneous recurrent electrographic seizures. A commercial recording system was connected and used as a reference point. The experiment was also video-monitored to cross-check seizure detections with clinically associated behaviors such as convulsions. This also helped to classify seizures based on the electrographic and behavioral features. For every subject, EEG was collected for 1 h and seizures were labeled by a professional epileptologist. The labeled data are used to set the threshold for the specific subject and the chip is programmed with the offline-calculated threshold. This threshold is then used for long-term online seizure detection and abortion.

Rats were anesthetized with isoflurane and oxygen, and placed in a stereotaxic frame. Two burr holes were drilled in the skull overlying the right and left temporal lobes. For the *in vivo* recording/stimulation experiments, the flex polyamide electrodes were bilaterally implanted into CA1 regions of both hippocampi using the stereotaxic micromanipulator. Also a micro-cannula (C333-001, Plastics One) was implanted similarly into the right CA1 region for drug infusion. The coordinates of electrode implantation were: bregma 4.3, midline ± 3.0, depth 3.1. Histologic examination (cryostat sections of paraformaldehyde-fixed brains) of the rat brains at the end of the experiments confirmed the location of the electrode.

The ECoG electrode was fabricated on a polyimide sheet of thickness 125 μm that was cleaned in acetone and isopropanol alcohol baths, and then dehydrated on a hotplate. Polyimide material was chosen for its flexibility, chemical stability, and biocompatibility properties. For the electrode material, gold pads with the diameter of 250 μm were designed. Chrome was used to improve adhesion between gold and polyimide. Metal films are deposited using e-beam evaporation and dc sputtering for chrome (30 nm) and gold (500 nm), respectively.

In order to reduce the surface impedance of the resulting microelectrode pads, modification technique was developed using low-current pulsed electroplating process to increase the pad surface roughness. Electroplating is performed using pure gold plating process (Technic Mini Plating Plant 3), in which a 30-mA current was applied in bursts of 20 s for 2 min. The resulting nanotextured electrodes exhibit rough surface and an improved average impedance of approximately 7 kΩ at 100 Hz, and 28 kΩ at 10 Hz.

Fig. 20(a) shows an example of *in vivo* online on-chip real-time seizure detection without stimulation. In the

TABLE II
SUMMARY OF THE EXPERIMENTAL RESULTS

SYSTEM:		
Technology	0.13μm	
Supply Voltage (Rec.)	1.2V	
Supply Voltage (Stim.)	2.5/3.3V	
Die Dimensions	2.6mm$\times$2.3mm	
Area Per Channel	$130\mu m \times 100\mu m$	
No. of Recording Channels	64	
No. of Stimulation Channels	64	
Power Dissipation (Rec.)	1.07/5.44mW	
RECORDING CHANNEL:		
Bandwidth	0.01-500 Hz	
Power/Ch	0.63μW	
Noise Bandwidth	0.1-500 Hz	
Input-Ref. Noise	1.13 μV_{rms}	
NEF	2.86*	
Area	0.013 mm^2 **	
Z_{IN} at OSR=100	0.99-1.02 MΩ	
ADC SNDR	72.2 dB	
STIMULATION CHANNEL:		
Type	Arbitrary current	
Voltage Compliance	3.1V	
Current Matching	1 %	
Current Range	10μA-1.35mA	
DAC Resolution	8 bits	
WIRELESS TX:		
Modulation	UWB	
Freq. Band	3.1-10.6 GHz	
Architecture	Delay-based	VCO-based
Data Rate	10Mbps	46Mbps
Range	10cm	2m
Power Diss.	100μW	3.7mW
WIRELESS POWER:		
Receiver Coil:		
Type	8-layer flexible	
Size	2cm x 2cm	
No. of turns	104	
Inductance	176 μH	
Coil Separation	15cm	
Frequency	1.5 MHz	
No. of Voltage Levels	10	

*: Amplifier + ADC
**: Does not include FIR filters used for seizure detection.

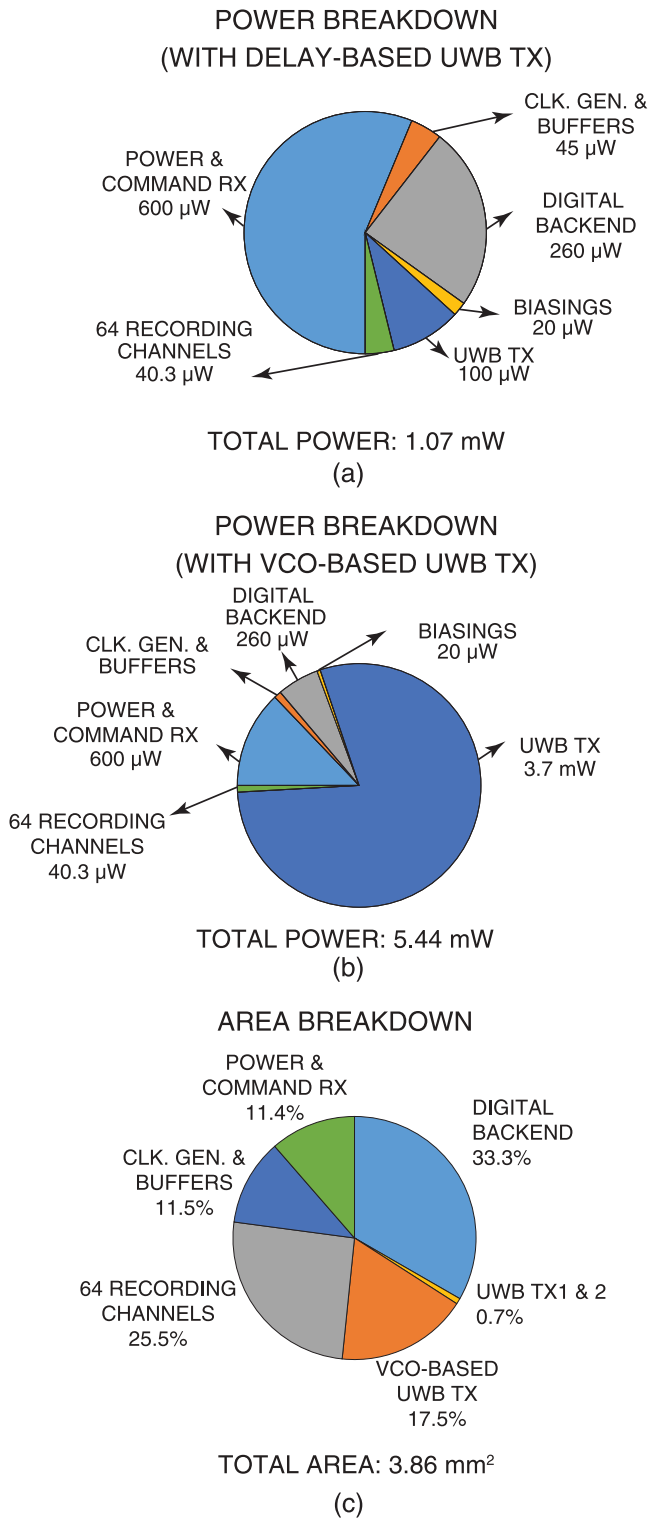

Fig. 22. Power breakdown of the integrated circuit operating in two modes. (a) With the delay-based UWB transmitter. (b) With the VCO-based UWB transmitter. (c) Area breakdown of the IC.

second experiment, the SoC was configured to automatically trigger the closed-loop electrical stimulation for the purpose of suppressing upcoming seizures. Fig. 20(b) shows the SoC-triggered stimulation upon a seizure onset detection. The feedback electrical stimulation consists of a burst of square-wave bipolar biphasic current pulses of 150 μA, pulsewidth 100 μs, frequency 5 Hz, and duration 5 s, triggered by the real-time synchrony analysis in response to the seizure precursor detection. The stimulation was delivered to the right or left hippocampus (depending on seizure initiation). The stimulation current was chosen according to safety considerations [36], which was three times lower than the maximum deliverable charge per phase [37].

B. Offline Early Seizure Detection in Humans

Fig. 21 shows an example of early seizure detection in offline human ECoG data from an epilepsy patient at the University of Toronto. The ECoG data set included 8 h of data from three patients and contained 12 labeled seizure periods. It was fed to the SoC to evaluate its efficacy in detection of seizures

TABLE III
STATE-OF-THE-ART NEURAL RECORDING AND/OR STIMULATION SOCS

Spec.	[8] JSSC'13 Genov	[7] JSSC'14 Wu	[31] JSSC'15 Rabaey	[32] JSSC'15 Yoo	[10] JSSC'16 Genov	[34] TBCAS'16 Spiegel	[33] TBCAS'16 Thakor	[35] TBCAS'16 Sodini	THIS WORK
Targeted Application	Epileptic Seizure Detection and Control	Epileptic Seizure Detection and Control	Rat EEG Recording	Epileptic Seizure Detection and Control	Epileptic Seizure Detection and Control	Monkey Neural Recording	Vagus Nerve Stimulation	Epileptic Siezure Detection	Epileptic Seizure Detection and Control
Tech. (μm)	0.13	0.18	0.065	0.18	0.13	0.18	0.18	0.18	0.13
Area (mm)	12	13.47	5.76	25	16	1.26	2.25	12	5.98
Supply (V)	1.2	1.8	0.5	1.8	1.2/2.5	N/R	1.5/5	0.9	1.2/2.5
Power Diss. (mW)	1.4	2.8	0.22	0.25	2.17	0.25	N/R	N/R	1.07*
NEURAL RECORDING									
Area/ch (mm^2)	0.09	0.5	0.025	0.7	0.09	0.3	0.56	0.26	0.013**
Power/ch (μW)	10	57.67	2.3	1.62	9.1	3.2	5.5	2.75	0.63
Bandwidth (Hz)	1-5k	0.1-7k	1-250	0.5-100	1-5k	0.5-7k	0.25-250	1-10k	0.01-500
Noise (μVrms)	4.7	5.23	1.43	0.90	7.5/4.2	2.8	1	1.13	1.13
Noise BW (Hz)	10-5k	0.5-7k	1-500	0.5-100	1-1k	0.5-7k	0.25-250	0.5-500	0.1-500
# of Rec. Channels	64	8	64	16	64	16	4	8	64
ADC Architecture	SAR	DMSAR	VCO	SAR	SAR	SAR	$\Delta\Sigma$	SAR	$\Delta^2\Sigma$
Max Offset (mV)	AC-coupled	AC-coupled	$\pm$50	AC-coupled	$\pm$50	AC-coupled	$\pm$30	AC-coupled	Rail-to-Rail
SIGNAL PROCESSING	YES	YES	NO	YES	YES	NO	NO	YES	YES
Closed-loop	YES	YES	-	YES	YES	-	-	NO	YES
Detection Method	Ampl/Phase Synchrony	Entropy /Spectrum	-	LSVM	Phase Derivative	-	-	Energy Threshold	Phase Synchrony
NEURAL STIMULATION	YES	YES	NO	YES	YES	NO	YES	NO	YES
# of Stim. Channels	64	1	-	1	64	-	4	-	64
Current Range (μA)	10-1200	30	-	PVTES	10-1000	-	250	-	10-1350
WIRELESS POWER	NO	YES	YES	NO	YES	YES	NO	NO	YES
Receiver Coil									
Type	-	Wire-wound	1-layer flex	-	8-layer flex	Wire-wound	-	-	8-layer flex
Size/Area(cm^2)	-	5.72	0.42	-	4	N/R	-	-	4
# of turns	-	4	1	-	104	N/R	-	-	104
Inductance (μH)	-	N/R	N/R	-	176	N/R	-	-	176
Coil Separation (cm)	-	N/R	1.6	-	$<$15	N/R	-	-	$<$15
Frequency (MHz)	-	13.56	300	-	1.5	13.56	-	-	1.5
# of Voltage Levels	-	3	2	-	10	3	-	-	10
WIRELESS COMM.	YES	YES	YES	NO	Tri-Band	YES	NO	NO	YES
Modulation	UWB	OOK	OOK	-	UWB/FSK	OOK	-	-	UWB
Frequency (Hz)	3.1-10.6G	401M	300M	-	$<$1G, 3.1-10.6G	13.56M	-	-	3.1-10.6G
IN-VIVO RESULTS	YES	YES	YES	NO	YES	YES	YES	NO	YES

-: Not Applicable
N/R: Not Reported
*: Without the VCO-based UWB Transmitter
**: Does not include FIR filters used for seizure detection.

prior to their clinical onset using the on-chip synchrony-based processor. The seizure detection algorithm yields an average sensitivity of 75% for the three patients when maximum false positive rate is set at 0.5 FP/h. When acceptable false positive rate is increased to 1 FP/h, the sensitivity reaches 100%.

VII. DISCUSSION

A. Resource Utilization

A summary of experimental measurement results is shown in Table II. Also, Fig. 22(a) and (b) shows the power breakdown of the chip when operating with the delay-based and VCO-based UWB transmitters, respectively. The SoC dissipates 1.07 mW when operating with the delay-based UWB transmitter and 5.44 mW with the VCO-based transmitter. For the ECoG ($<$500 Hz) bandwidth, the 64 neural ADCs consume 40.3 μW for 64 channels resulting in 630 nW per channel.

Fig. 22(c) shows the area breakdown of the chip (excluding routings, IO pads, and decoupling capacitors for supplies). The total area occupied by 64 recording and stimulation channels together with the digital back end, wireless transmitters, and power management circuits is 3.86 mm^2. The 64-tap FIR filters and the synchrony processor have the biggest quota with 33 % followed by the 64 recording front ends with 25.5%. The 64 stimulators are added to the chip with less than 0.1% area overhead, since they share some blocks such as DAC and the memory (for duty-cycle control) with the recording circuitry.

B. Area and Power Scalability

Fig. 23(a) shows how the power consumption of all the blocks scales linearly with the input signal bandwidth. As shown, the channel dissipates a total of 630 nW for recording signals in the ECoG frequency band. This gives the advantage of working with proportionally lower power, when recording signals with smaller frequency bandwidth.

Fig. 23(b) shows how the active-component-dominated channel area scales with the CMOS technology node compared with a conventional ac-coupled channel [8]. In this figure, the black line shows how the minimum gate width scales with the technology, and the red circles show the estimated

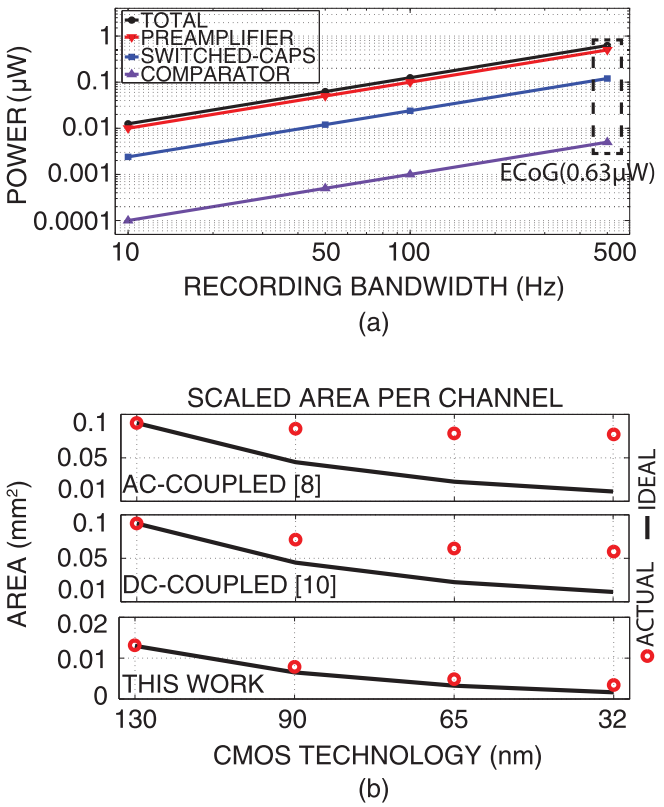

Fig. 23. (a) Channel power scalability with the input signal frequency bandwidth. (b) Comparison between conventional ac-coupled [8], dc-coupled [10], and presented $\Delta^2\Sigma$-based channel area scalability with CMOS technology node.

scaled channel area based on [30]. Since the presented channel is dominated by active components, its area scales almost linearly with technology, which allows for the integration of 1000+ channels for high-definition brain recording when the design is taken to a more advanced technology node.

C. Comparison With the State of the Art

The SoC is compared with the state of the art in terms of both system-level and channel-level performance, which is presented in Table III.

In terms of applications, the functionality of the presented design is validated *in vivo* for monitoring, detection, and control of epileptic seizures. However, due to the ability to record signals with rail-to-rail ac amplitude and dc offset variations, the chip is capable of recording other physiological signals with amplitudes much larger than the nominal maximum 1 mV for EEG signals.

In terms of system integration, this paper demonstrates one of the highest levels of integration among recently published state-of-the-art SoCs by combining 64 rail-to-rail signal recording channels, 64 current-mode arbitrary-waveform stimulation channels, 64 multiplying $\Delta^2\Sigma$ ADCs, a multi-core DSP unit, short- and long-range wireless transmitters, and wireless power and command receivers.

In terms of the channel design, this paper has the smallest channel area, while amplifier and ADC and part of the BPF are included in the channel. It also features one of the lowest integrated input-referred noise and power consumption for the ECoG band, which results in a superior noise efficiency factor. The power consumption is scalable with the input signal frequency bandwidth, and the channel area is scalable with CMOS technology node.

VIII. Conclusion

A CMOS wireless closed-loop neurostimulation SoC is presented. The 6-mm^2 die integrates 64 rail-to-rail differential $\Delta^2\Sigma$ neural recording channels with in-channel correlated double-sampling, mixed-mode multiplication, multi-core digital signal processing unit, dual-range UWB wireless transmitters, active rectifiers, regulators and DACs for inductive power receiving, ASK demodulator for command receiving, and 64 in-channel synchrony-triggered current-mode arbitrary-waveform stimulators.

The SoC is implemented in IBM 0.13-μm technology and dissipates 1.07 and 5.44 mW with the delay-based and VCO-based UWB transmitters, respectively. The power consumption of neurostimulation channels scales with input signal frequency bandwidth. Thanks to the presented architecture, the channel area is around 7$\times$ smaller than our previously reported ac-coupled design, and is dominated by active components, which make it technology-scalable. The SoC is validated *in vivo* using epilepsy monitoring (seizure detection) and treatment (seizure suppression) experiments.

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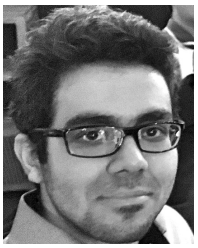

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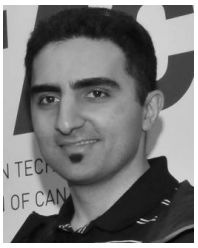

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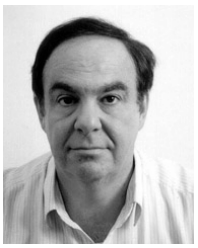

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