Multi-Channel Integrated Neural Interfaces for Distributed Electro-Chemical Sensing

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***Abstract*— Distributed monitoring of electro-chemical activity facilitates understanding various neurophysiological phenomena. Single-chip neural interfaces offer a small-size, low-power, low-noise and cost-effective alternative to commercial bench-top instruments. They present an opportunity to enhance implantable microsystems functionality with multi-site simultaneous distributed recording capability. We present two integrated neural interfaces, for chemical and electrical sensing. The first integrated neural interface performs simultaneous current-mode acquisition of 16 independent channels of redox currents ranging five orders of magnitude in dynamic range over four scales down to hundreds of picoamperes. The second neural interface acquires neural field potentials in microvolts to millivolts range on a 16x16-electrode microarray in voltage mode. Each microsystem features programmable gain amplifiers, tunable band filters, configurable sample-and-hold circuits, and is ready for external analog-to-digital conversion. Side-by-side quantitative comparison of the two neural interface technologies is given.**

I. Introduction

The electro-physiology of populations of biological elements has been greatly aided by the development of microfabricated array of electrodes [1]. Electro-chemical activity, such as that of neurons, typically exhibits considerable heterogeneity across biological ensembles. Sensory systems capable of recording on very many channels allow to capture, study and utilize this heterogeneity. The spectrum of electro-chemical activity often remains significant at higher frequencies (e.g., 0.5-10kHz). This calls for multi-channel sensory systems performing true simultaneous signal acquisition without multiplexing. Conventional bench-top signal acquisition instruments are bulky, expensive, and prone to interference noise due to wiring. They typically are stationary and provide only one or few recording channels. Single-chip neural interfaces offer a small-size, low-power, low-noise and cost-effective alternative to commercial bench-top instruments. When optimized for power (e.g., by trading for sampling rate), they enable implantable microsystems to perform multi-site truly simultaneous distributed spatial recordings.

A number of integrated neural interfaces with more than two channels have been recently developed. Both time-multiplexed and simultaneous signal acquisition systems have been reported. Electrical and chemical sensing is implemented through voltage and current acquisition respectively.

Integrated neural interfaces with time-multiplexed signal acquisition perform recordings on multiple sites with the number of signal recording channels being smaller than the number of recording sites [2], [3]. The number of channels typically ranges from eight [2] to 32 [3]. Time-multiplexed signal acquisition does not allow to accurately capture heterogeneity across biological ensembles as recording on different channels takes place at different times.

Integrated neural interfaces for simultaneous signal acquisition record on all channels at the same time. They require dedicated channels for each recording electrode. Current-acquisition neural interface microsystems, or potentiostats, record chemical concentrations by measuring reduction-oxidation currents. Recently reported integrated potentiostats [4], [5] employ oversampling data conversion techniques and achieve very high dynamic range, down to 8 pA currents, at the cost of reduced sampling rate of less than 30 samples per second.

Voltage-acquisition microsystems record neural action potentials by measuring extracellular potential field. Existing designs trade between acquisition channel circuit area and intrinsic circuit noise. The 4×4 sensor array design reported in [6] achieves 9 μV RMS noise at the expense of 400 μm cell pitch. The 128×128 biosensor array design presented in [7] has 7.8 μm cell pitch at the cost of increased circuit noise.

We present two integrated neural interface architectures for simultaneous signal acquisition of currents and voltages on very many channels, for chemical and electrical sensing respectively. The current-acquisition microsystem, described in Section II, is implemented in current mode and can simultaneously sample 16 redox currents down to 46 pA with the sampling rate of up to 200 $ksps$. The voltage-acquisition voltage-mode neural interface, presented in Section III, simultaneously samples 256 action potentials on a 170 μm electrode grid with 15 μV RMS noise. The two neural interface technologies are quantitatively compared in Section IV to offer integrated neural interface design trade-off insights.

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II. Current-Acquisition Current-Mode Integrated Neural Interface

For multi-site simultaneous chemical sensing, a current-acquisition current-mode integrated neural interface was designed, prototyped and experimentally characterized.

A. Architecture

The current-acquisition neural interface is a track-and-hold potentiostat [8] comprising 16 current-mode inputs, 4 voltage references setting the voltage levels of the virtual-ground current inputs in groups of 4, and a single full-range differential voltage output, all on a single chip. The block diagram of the single-chip potentiostat is given in Figure 1. Each of the 16 channels is independently configured for a gain of attenuation covering four orders of magnitude allowing to acquire bidirectional currents in the range from 46 pA to 50 μA, at a reference voltage ranging from 0 to 5V. Programmable cut-off frequencies ranging from 50Hz to 400kHz prevent aliasing of high frequency components and allow to decrease the level of noise generated prior to sampling. The maximum fully sustained sampling rate ranges from DC to 200kHz. The outputs of the chip are pipelined and continuously valid, interfacing asynchronously to an external ADC on the PC host acquisition board for data post-processing.

B. VLSI Implementation

The input current to each data channel in Figure 1 is summed with a reference current I_{ref}, to convert the signal from bipolar to unipolar form. A transconductance amplifier drives a PMOS load transistor to provide a low impedance input stage. The acquired input current is then fed into a scaling circuit which normalizes the signal to the range [0, 1] μA. The same scaling factor is used to attenuate the reference current I_{ref} at the input stage. The normalized current is fed into an anti-aliasing low-pass filter.

The integrator at the end of the channel is used for current-to-voltage conversion. The timing of integration in one of the reference channels (bottom of Figure 1), supplied a constant current equal to the normalized current range (1 μA), sets the voltage range of conversion in the 16 channels. A 16-to-1 multiplexer selects the integrated signal of one of the 16 channels at the output. The output of the second reference channel, supplied half the current of the timing reference channel, serves as a 'zero-level' reference to the other channels in a differential output format, for reduced sensitivity to noise and power supply variations. In hold mode, the differential output from the previous integration cycle is buffered and held at the output while the current integration process is taking place.

The track-and-hold potentiostat was integrated on a 2.25×2.25 mm^2 die fabricated in a 1.2 μm double-poly CMOS process. The chip micrograph is shown in Figure 2. Details on the circuits and characterization of the chip are presented in [8]. Experimentally verified electrical characteristics are summarized in Table I.

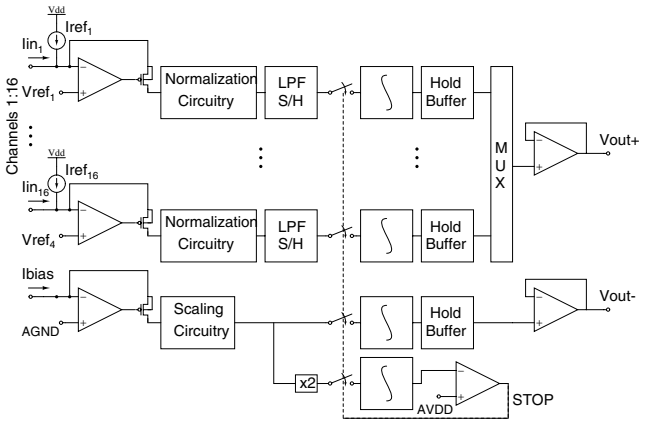

Fig. 1. Block diagram of the current-acquisition integrated neural interface.

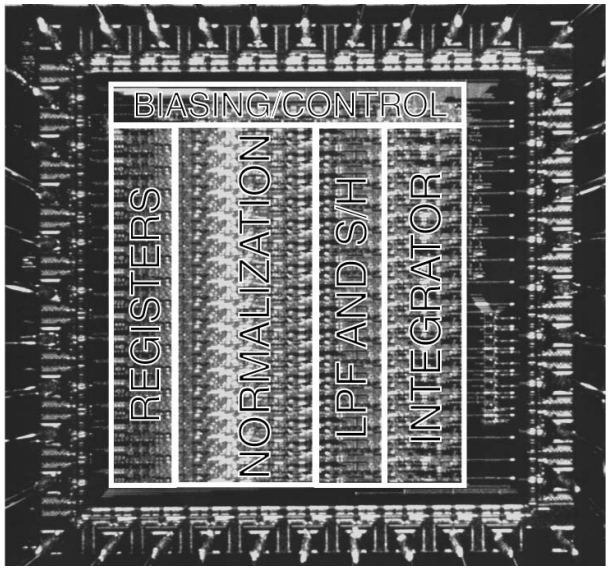

Fig. 2. Chip micrograph of the 16-channel integrated track-and-hold potentiostat. Die size is 2.25×2.25 mm^2 in 1.2 μm CMOS technology.

III. Voltage-Acquisition Voltage-Mode Integrated Neural Interface

For low-noise distributed neural potential field recording, a multi-channel voltage-mode integrated neural interface has been designed and prototyped.

A. Architecture

The voltage-acquisition neural interface records action potentials on 256 independent channels simultaneously. The voltage-mode signal acquisition circuits are organized in a 16×16-cell array. One column of the array is shown in Figure 3.

Each channel in the array is interfaced to recording electrodes through non-passivated top-most metal. Differential recording with respect to a single reference electrode reduces common-mode noise. Each signal acquisition channel contains a high-pass filter (HPF), a low-pass filter (LPF), and two

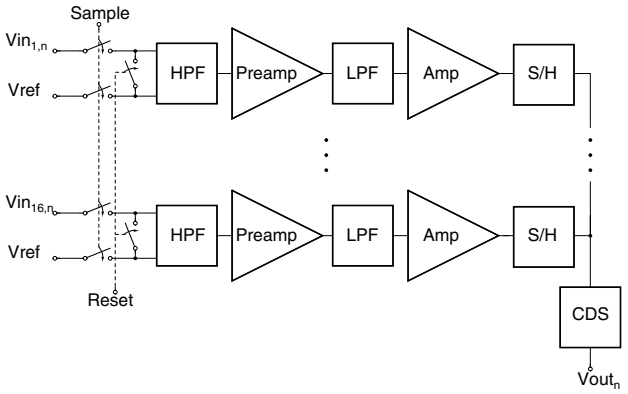

Fig. 3. Block diagram of one column of the voltage-acquisition integrated neural interface.

amplification stages. The channel also includes a sample-and-hold cell with an analog memory (S/H).

Due to process variations, device mismatches among the cells have a random component and thus impair data integrity across the array. Double sampling is employed to subtract unwanted offsets from the desired contaminated signal. Double sampling circuits compute the difference between the amplified recorded signal stored in memory and the output of the channel when it is reset.

In order to reduce low-frequency noise such as flicker noise, the double sampling circuit is configured to perform correlated double sampling (CDS) [10]. In order to do so, the analog memory is implemented as a double memory. The amplified neural activity recording is stored in one memory, the output of the channel when the input is reset is stored in the second one. Both the data being recorded and the reset values are acquired and stored simultaneously on the whole array. The channel-to-channel time correlation of low-frequency noise present in both samples is preserved, avoiding errors due to the rolling readout delay. The difference is then computed by the CDS circuit.

The sample-to-reset time of a channel is limited by the time constant of the LPF. Reducing this time extends the bandwidth of the LPF and, in turn, increases the sampling frequency to satisfy Nyquist theorem. When necessary, increased sampling rate can be traded for lower flicker noise. This trade-off is absent in the case when the input signals are band-limited, yielding further reduction in flicker noise.

Correlated double sampling is time-multiplexed with low-noise signal acquisition without pipelining. This is necessary to minimize substrate noise during the voltage acquisition phase. Once the voltage is amplified and sampled, the substrate noise no longer has a significant effect on the dynamic range of the neural interface. Array readout is implemented in a serial fashion as controlled by row and column address decoders.

B. VLSI Implementation

Most of the frequency content of extracellular action potentials is concentrated between 0.1Hz to 7kHz. Signal amplitudes range from 50 μV to 500 μV, with 100 μV being a typical average value. A single-stage wide-swing cascoded transconductance amplifier with p-channel MOS input differential pair is employed, both for the preamplifier and the amplifier. The first stage has a fixed gain of 100, and the second stage has a programmable gain of 2, 10, 25 and 50. The gain programmability is achieved by selecting the size of the capacitor in the feedback by external digital control signals. The transconductance amplifier is optimized for low thermal noise under the 170 μm pitch cell area constraint. The low-noise amplifier design procedure employed is detailed in [9].

High pass filtering prevents DC signals, generated at the electrode-tissue interface, from saturating the amplifiers. The HPF is implemented as a frequency selective feedback of the first amplifier. An ultra-low value for the HPF cut-off frequency is achieved by employing a high resistance element (on the order of $T\Omega$) in parallel with a capacitor. Such high resistance is realized by two diode-connected MOS transistors biased in deep subthreshold conduction region and connected in series [9].

The sampling to move from continuous time to discrete time requires low-pass filtering to avoid aliasing. The LPF filter is implemented by utilizing the intrinsic low-pass frequency response of the second-stage amplifier. The cut-off frequency is controlled by starving the bias current of this transconductance amplifier.

Correlated double sampling circuit is implemented in the switched capacitor technology. A single-ended cascoded common-source amplifier with linear capacitor input and feedback networks is employed. Additional circuitry for optional post-fabrication recording electrode platinum electroplating is included.

The voltage-acquisition neural interface was implemented on a $3\text{mm} \times 4.5\text{mm}$ die in a 0.35 μm double-poly standard CMOS technology. The simulated characteristics are summarized in Table II.

IV. Neural Interface Technologies Comparison

Table I and Table II offer a side-by-side comparison of the characteristics of the current-acquisition and voltage-acquisition neural interfaces. The tables offer insights at current-mode versus voltage-mode technologies for implementing current-acquisition and voltage acquisition neural interfaces respectively. Design parameters such as channel area density, signal bandwidth, sampling rate, dynamic range, and power dissipation per channel represent various trade-offs in voltage-mode and current-mode technologies. These should be taken into account when designing a custom neural interface.

The current-acquisition potentiostat simultaneously transduces neurotransmitter activity at multiple locations in the brain tissue, e.g., in synaptic clefts. The neural interface acquires oxidation-reduction currents generated at the surface of each sensing electrode. The voltage-acquisition neural interface monitors a two-dimensional action potential field within a brain tissue area under observation. These technologies allow to study various neurophysiological phenomena such as those in sensory-motor systems, hippocampus, auditory

TABLE I
CURRENT-ACQUISITION CURRENT-MODE NEURAL INTERFACE
MEASURED CHARACTERISTICS

Channels	16			
Max Sampling Rate	200kHz			
Input Current Range	-50nA-+50nA	-500nA-+500nA	-5μA–+5μA	-50μA–50μA
Input-Referred RMS Current Noise	46pA	1nA	8nA	25nA
Input Impedance	125Ω			
DC Offset	+/-5mV	+/-5mV	+/-5mV	+/-10mV
Power Dissipation	12.5mW			
Analog Volt. Range	0-5V			
LPF Cut-off Freq.	50Hz - 400kHz			
Power Suppl. Volt.	-2V; +7V			
Technology	1.2μm, BiCMOS (vertical NPN), double poly			
Electrode type	Off-chip			
Die Size	2.25 mm x 2.25 mm			

TABLE II
VOLTAGE-ACQUISITION VOLTAGE-MODE NEURAL INTERFACE
SIMULATED CHARACTERISTICS

Channels	256
Max Sampling Rate	40kHz
Programmable Gain	200, 1000, 2500, 5000
Input-Referred RMS Voltage Noise	15μV
Output Voltage Range	1.5V
DC Offset Compensation	Correlated Double Sampling
LPF Cut-off Freq.	1kHz - 10kHz
HPF Cut-off Freq.	< 0.1Hz
Power Suppl. Volt.	3.3V
Core Power Dissipation	6mW
Technology	0.35μm, mixed-signal CMOS, double poly
Electrode type	On-chip; 170μm pitch
Die Size	3 mm x 4.5 mm

nerve and visual cortex. The availability of the vast amount of data recorded simultaneously from many distributed sites is necessary in studying and analyzing heterogeneity across neural populations.

V. CONCLUSION

We presented a current-acquisition and a voltage-acquisition neural interfaces for simultaneous distributed multi-site electro-chemical activity monitoring. The multi-channel architectures for both signal acquisition microsystems were introduced and VLSI implementations discussed.

The current-mode neural interface has 16 independent acquisition channels for simultaneous recording of redox currents with an input dynamic range spanning over five orders of magnitude down to 46 pA. The sampling rate can be programmed in the range from DC to 200kHz. The power consumption is 12.5 mW at the maximum sampling rate.

The voltage-mode neural interface has a 16×16 array of voltage acquisition cells for two-dimensional simultaneous recording of extracellular action potentials. The input voltage ranges from 50 μV to 500 μV, with a simulated RMS input referred noise of 15 μV. The simulated power consumption is 6 mW at the maximum sampling rate of 40kHz.

Side-by-side qualitative comparison between the two approaches was made to offer insights into design trade-offs between voltage-mode and current-mode neural interface technologies for electro-chemical neural activity monitoring.

REFERENCES

[1] P.M. George, J. Muthuswamy, J. Currie, N.V. Thakor, and M. Paranjape, "Fabrication of screen-printed carbon electrodes for sensing neuronal messengers," *BioMEMS,* vol. **3** (4), pp. 307-313, December 2001.

[2] P. Mohseni, and K. Najafi, "A Battery-Powered 8-Channel Wireless FM IC for BioPotential Recording Applications," *ISSCC Dig. Tech. Papers,* pp. 560-561, February 2005.

[3] T. Akin, K. Najafi, and R.M. Bradley, "A wireless implantable multichannel digital neural recording system for a micromachined sieve electrode," *IEEE Journal on Solid-State Circuits,* vol. **33** (1), pp. 109-118, January 1998.

[4] M. Stanacevic, K. Murari, G. Cauwenberghs, and N. Thakor, "16-channel wide-range VLSI potentiostat array," *IEEE International Workshop on Biomedical Circuits and Systems,* December 1-3, 2004.

[5] K. Murari, N. Thakor, M. Stanacevic, and G. Cauwenberghs, "Wide-Range, Picoampere-Sensitivity Multichannel VLSI Potentiostat for Neurotransmitter Sensing," *Proc. 26th Ann. Int. Conf. IEEE Engineering in Medicine and Biology Society (EMBS'2004),* San Francisco, September 1-4, 2004.

[6] W.R. Patterson, Yoon-Kyu Song, C.W. Bull, I. Ozden, A.P. Deangellis, C. Lay, J.L. McKay, A.V. Nurmikko, J.D. Donoghue, and B.W. Connors, "A microelectrode/microelectronic hybrid device for brain implantable neuroprosthesis applications," *IEEE Transactions on Biomedical Engineering,* vol. **51** (10), October 2004.

[7] B. Eversmann, M. Jenkner, C. Paulus, F. Hofmann, R. Brederlow, B. Holzapfl, P. Fromherz, M. Brenner, M. Schreiter, R. Gabl, K. Plehnert, M. Steinhauser, G. Eckstein, D. Schmitt-Landsiedel, and R. Thewes, "A 128 × 128 CMOS bio-sensor array for extracellular recording of neural activity," *IEEE Journal on Solid-State Circuits,* pp. 2306 - 2317, vol. **38** (12), February 2003.

[8] R. Genov, M. Stanacevic, M. Naware, G. Cauwenberghs, and N. Thakor, "VLSI Multi-Channel Track-and-Hold Potentiostat," in *Microtechnologies for the New Millennium, Bioengineered and Bioinspired Systems 2003,* Proc. SPIE vol. **5119**, May 2003.

[9] R.R. Harrison, and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE Journal on Solid-State Circuits,* vol. **38** (6), pp. 958-965, June 2003.

[10] C.C. Enz, and G.C. Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," *Proceedings of the IEEE,* vol. **84** (11), pp. 1584-1614, November 1996.