Multi-step Binary-weighted Capacitive Digital-to-Analog Converter Architecture

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***Abstract*— We present a capacitive digital-to-analog converter (DAC) architecture combining properties of the binary-weighted and serial charge-redistribution DACs to yield high integration density and high accuracy. The architecture provides the flexibility to trade area with conversion speed based on a set of area-speed-linearity constraints. We validate the architecture using a 10-bit two-step DAC example, simulated in a standard 0.35µm CMOS technology. The 10-bit DAC occupies 32 times less area than the conventional 10-bit binary-weighted DAC, has low INL, good matching, and high tolerance to parasitic capacitance.**

I. INTRODUCTION

Charge-redistribution digital-to-analog converters (DACs) are commonly employed in successive approximation register (SAR) analog-to-digital converter (ADC) designs. In distributed sensory applications, several hundred of such ADCs may be placed on a single chip [1]. This leads to tight area constraints for the data converter block. Low capacitance densities [2] and matching requirements [3] make it difficult to reduce the large area occupied by the DAC capacitors.

Common approaches to reduce the capacitor area in charge-redistribution DACs trade area with linearity, speed and complexity. The binary-weighted DAC (BDAC) [4] and the serial DAC (SDAC) [5], offer a fast conversion speed and use small area respectively. The BDAC occupies large chip area, with a high capacitance spread and cannot achieve resolutions above eight to 10 bits. The SDAC is slow as the conversion time scales linearly with the resolution. It also suffers from linearity errors due to excessive switching.

To overcome the large area constraint of the BDAC, while maintaining high speed, several architectures have been proposed. The two-stage buffer DAC [6] occupies significantly less area but requires a unity gain buffer, increasing the complexity and power consumption. The two-stage capacitor network [7] assumes the top plate parasitics to be negligible and requires a transconductance amplifier to remove the nonlinearities. A more generalized form of the two-stage DAC, the C-2C DAC [8], occupies even smaller area but suffers from high nonlinearities due to the top and bottom plate parasitic capacitances. Several modifications have been discussed to remove these nonlinearities, which either do not sufficiently cancel the effect [9] or have special process requirements. The pseudo C-2C ladder DAC [10] requires a special sandwich capacitor to ensure that the top-plate parasitic capacitance is negligible. Its linearity is sensitive to the ratio of the parasitic capacitance to the desired capacitance. All of the above-mentioned charge redistribution DAC architectures reduce BDAC integration area at the expense of linearity which may limit their utility.

We present a DAC architecture which trades speed for area to achieve high linearity, low circuit complexity, low power dissipation, and very low supply voltages. It is ideally suited for sensory array applications where the speed is not critical but which require compact integration. The architecture combines features from the BDAC and the SDAC. Its unique characteristic is the design flexibility to implement an optimal trade-off given a set of area, speed and linearity constraints. As in SDAC, speed can be traded for higher resolution in run time.

Another approach to trade area with speed is utilized in the two-step DAC [11]. It however occupies twice the capacitor area of the proposed design and requires an operational amplifier with a large feedback capacitor for voltage division. In contrast, the proposed design implements an inherent voltage division by reusing the charge redistribution capacitors reconfigured with three extra switches. In the following sections, we discuss the proposed architecture in detail and provide simulation results validating its utility.

II. ARCHITECTURE

The architecture of a N-bit multi-step binary-weighted DAC (MBDAC) is shown in Figure 1. The input is a binary word

$$B = \sum_{i=1}^{N} 2^{-i} b_i \ , \qquad (1)$$

where b_i are the input binary coefficients. As stated in Section I, the proposed architecture combines features of the binary-

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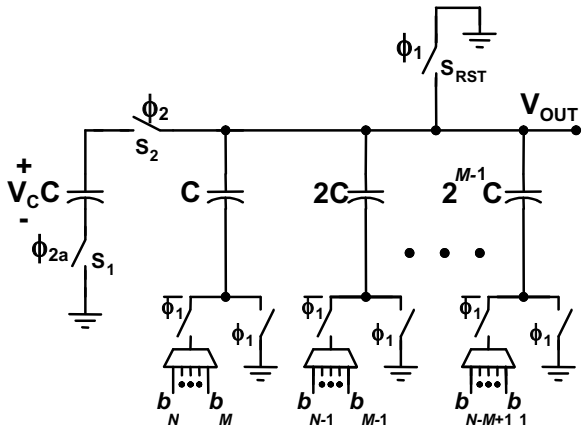

Figure 1. Multi-step binary-weighted DAC architecture.

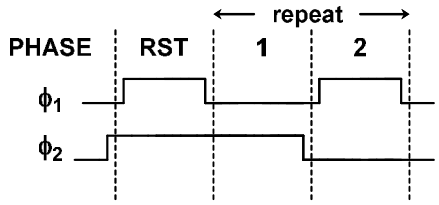

Figure 2. Timing diagram of the multi-step binary-weighted DAC.

weighted and serial DAC architectures. It utilizes the capacitive resources equivalent to a *M*-bit BDAC, with *M* binary-weighted capacitors and a terminating capacitor *C* (the leftmost capacitor in Figure 1). The MBDAC performs each data conversion in several steps, similar to the SDAC. The number of steps is calculated as $K=N/M$, assuming here for simplicity that *N* is an integer multiple of *M*. The MBDAC capacitors have to be matched to at least *N* bits on chip.

The timing diagram of the MBDAC is depicted in Figure 2. The clock ϕ_{2a} (not shown) is an advanced version of the clock ϕ_2. Initially all capacitors are discharged by turning on switches S_1, S_2 and S_{RST}. All nodal voltages are zero. After the reset, switch S_{RST} is turned off.

Each operation step of the MBDAC has two clock phases as follows.

Phase 1 (*M*-bit conversion and charge sharing):

In step 1: The *M* least significant bits of *B* are selected by the input digital multiplexers and applied to the bottom plates of the *M* binary-weighted capacitors. This results in an equivalent *M*-bit analog output voltage

$$V_{OUT}(1) = V_{REF} \sum_{i=1}^{M} 2^{-i} b_{i+N-M} \cdot \qquad (2)$$

In step *k*, $1<k\leq K$: The next *M* less significant bits of *B* are selected by the input digital multiplexers and applied to the bottom plates of the *M* binary-weighted capacitors. This generates an equivalent *M*-bit analog voltage at the output. Simultaneously, the initial charge on the terminating capacitor gets distributed into the rest of the capacitors. This results in a residue voltage division by a factor of 2^M at the output. These two voltage contributions get added to produce an equivalent *kM*-bit DAC output voltage:

$$V_{OUT}(k) = V_{REF} \sum_{j=1}^{k} 2^{-(k-j)M} \left(\sum_{i=1}^{M} 2^{-i} b_{i+N-jM} \right). \qquad (3)$$

Phase 2 (hold and reset):

In each step *k*, $1\leq k\leq K$: the terminating capacitor *C* is disconnected by turning the switches S_1 and S_2 off. It holds the output voltage of the previous phase. All the capacitors except for the terminating capacitor are discharged to ground. The switch S_1 is turned off before the switch S_2 in order to remove input-dependent charge injection into the terminating capacitor [12]. The inherent voltage division by 2^M in phase 1 further reduces the input-independent offset due to charge injected by S_1 and S_{RST} switches.

Phases 1 and 2 are repeated until all the *N* bits have been applied to the DAC. If *M* is not a factor of *N* then extra zeros are padded in front of the MSB. The output voltage after all *K* steps is

$$V_{OUT}(K) = V_{REF} \sum_{i=1}^{N} 2^{-i} b_i \cdot \qquad (4)$$

This corresponds to an *N*-bit digital-to-analog conversion output. With a small overhead of digital multiplexers, the MBDAC provides flexibility in the choice of an optimum area-speed trade-off.

III. Performance Analysis

The MBDAC results in significant savings in integration area as compared to the popular BDAC. The required capacitor area decreases exponentially with the number of steps by a factor of $2^{N-(N/K)}$. For example, for a 10-bit, two-cycle MBDAC, the area savings are by a factor of 32. The significant reduction in area results in corresponding savings in power and an increased speed.

The noise performance of the MBDAC is worse than that of the BDAC, due to multiple sampling of the switching noise. For a two-step conversion, its output noise power is four times higher than that of the BDAC. It can be argued that for a given resolution, the MBDAC requires larger sized unit capacitances than the BDAC to keep the noise voltage less than half the LSB. However, in modern standard CMOS technologies, the capacitor sizes are determined mainly by the matching requirements, which are stricter than those due to noise considerations [3, 13-15]. Moreover, the noise in the MBDAC degrades linearly with the increase in the number of conversion steps whereas the area savings grow exponentially. Correspondingly, the area of the MBDAC is always significantly less than that of the BDAC. The use of only passive components and significantly lower capacitance significantly reduce the requirements on the power dissipation. A low supply voltage can be utilized as a transconductance amplifier is not required (e.g., in a SAR ADC only a comparator is needed).

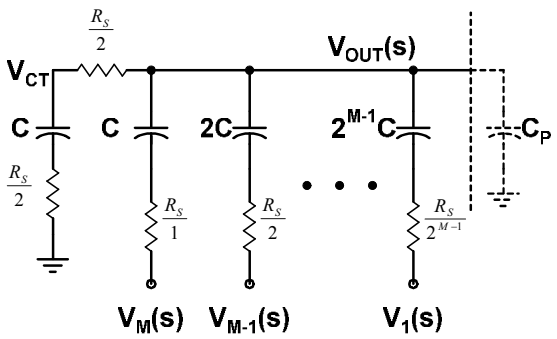

Figure 3. Equivalent RC circuit of the multi-step binary-weighted DAC.

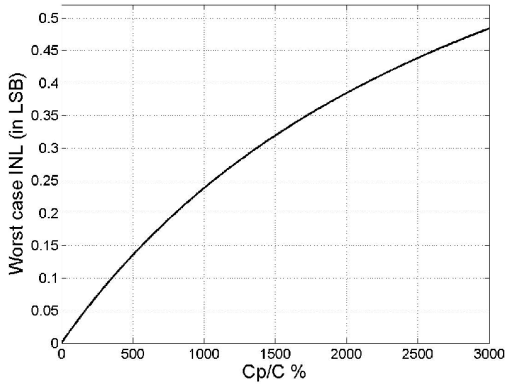

Figure 4. Worst case simulated INL versus C_P/C ratio.

TABLE I. 10-BIT CHARGE-REDISTRIBUTION DACS COMPARISON

D/A type	*Area*	*Speed*	*Linearity*	*Matching*	*Complexity*
Binary-weighted [5]	1024C	1	High	Low	Moderate
Serial [6]	2C	0.1	Low	High	Moderate
Two-stage buffer[7]	64C	1	High	Moderate	High
Two-stage [8]	64C	1	Moderate	Moderate	High
C-2C [9]	29C	>1	Low	High	Low
Pseudo C-2C ladder [11]	38C*	>1	Moderate	High	Low
Two-step[12]	64C	0.5	Moderate	Moderate	High
This work-I	32C	0.5	High	High	Moderate
This work-II	16C	0.33	High	High	Moderate

a. C is the unit capacitance, *b.*Speed is compared relatively, * Using typical value of γ

The MBDAC circuit has a lower time constant compared to an equivalent conventional BDAC. Choosing the resistance values for the switches S_1 and S_2 and for those connected to the inputs V_M to V_1, as shown in Figure 3, results in the zero theoretical intrinsic time constant of the DAC. The effect of the binary-weighted bottom plate parasitic capacitances also gets cancelled. The transfer function neglecting the parasitic capacitance at the node V_{CT}

$$V_{OUT}(s) = \sum_{i=1}^{M} 2^{-i} V_i(s) \frac{1}{1 + 2^{-M}\left(C_P C^{-1} + sR_s C_P\right)}. \quad (5)$$

The addition of a dummy resistor in the terminating capacitor branch of a conventional binary-weighted architecture results in a complete pole-zero cancellation. This resistance corresponds to the total resistance of the switches S_1 and S_2. The transients in a MBDAC are therefore fast, limited only by other parasitic capacitances. Table 1 compares the MBDAC architecture with other charge-redistribution DAC designs for a 10-bit resolution.

IV. SIMULATION RESULTS

A. Effect of Parasitic Capacitances

We validate the architecture using a 10-bit DAC example. Unlike the C-2C DAC, which is prone to errors due to parasitic capacitances [8-10], the MBDAC is resistant to such nonlinearities. As shown in Figure 1, the voltage node V_{OUT} is connected to the top plate of all the capacitors. These top plate parasitics are significantly smaller and shall only contribute to a gain error. Any other parasitic capacitance C_P attached to node V_{OUT}, such as the input capacitance of the connecting comparator/amplifier cause negligible nonlinearity. The nonlinearity effect is significantly reduced by the inherent voltage division in the circuit. The dependence of V_{OUT} on the parasitic capacitance C_P for the 10-bit, two-step MBDAC can be expressed as

$$V_{OUT}(k) = V_{REF} \sum_{j=0}^{1} \left(\frac{C}{2^5 C + C_P} \right)^{(2-j)} \left(\sum_{i=1}^{5} 2^{-i} b_{i+5-5j} \right)$$

Figure 4 shows the MATLAB simulated linearity errors.

B. Effect of Capacitor Mismatches

The MBDAC can achieve high capacitor matching due to less capacitance spread. Smaller capacitors are laid out close to each other with smaller gradient-related mismatch. Figure 5 shows the yield calculated on the basis of the worst-case INL for a given random mismatch variability, using MATLAB simulation. It shows that 0.1 percent matching is sufficient to guarantee 99 percent yield for a 10-bit, 2-step MBDAC. The figure also shows the good yield of a 12-bit BDAC, assuming zero gradient mismatch variability. In practice, however, this is not true and typically BDAC resolution is limited to eight to 10 bits. The large capacitance spread contributes to the high gradient mismatch [13-15]. The MBDAC can achieve this matching, as reflected in the second column in Table 1.

C. Transient response

A sample 10-bit two-step MBDAC has been designed and simulated in a standard 0.35 μm CMOS technology. The conversion speed of the DAC is 25 MHz. NMOS-only switches have been used. The DAC reference voltage is 1.2 V at a 3 V power supply. The unit capacitance size is 100fF as needed to achieve the accuracy requirement. Figure 6 shows the INL plot obtained for all input codes. Figure 7 shows the simulated binary-input-midpoint-transition plot for the DAC. The negative spikes in Figure 7 are due to the grounding of the DAC inputs during the reset phase. Such a behaviour is also observed in the case of a BDAC.

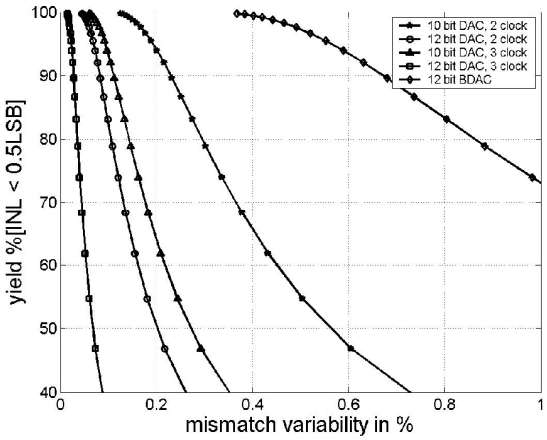

Figure 5. Simulated worst-case yield at the worst case INL as a function of the random mismatch variability parameter σ. Gradient mismatch parameter is assumed to be zero.

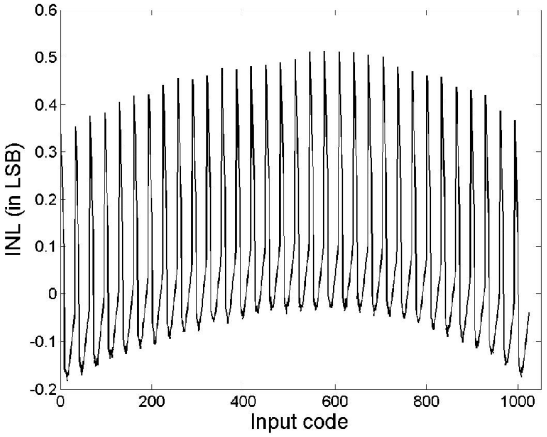

Figure 6. Simulated INL error of the 10-bit, two-step MBDAC.

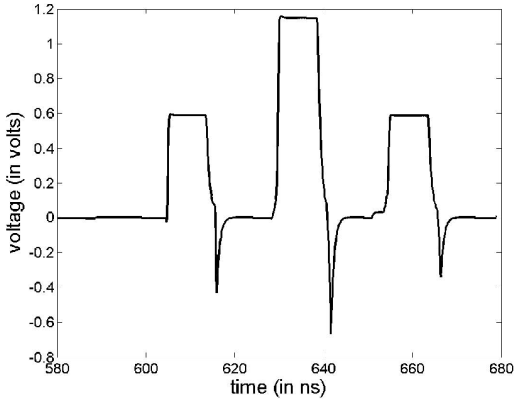

Figure 7. Simulated DAC midpoint transitions.

CONCLUSION

We proposed a simple VLSI architecture for highly-integrated charge-redistribution DACs. The architecture allows for efficient optimization based on the specifications of area, speed and linearity. The significant reduction in area and the lack of an amplifier make the architecture attractive for low-voltage and low-power applications. The less capacitance spread improves matching while the high tolerance to parasitics prevents linearity degradation. The use of a matching resistor for the terminating capacitor yields a high operational speed.

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