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VLSI Multivariate Phase Synchronization Epileptic Seizure Detector

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Abstract— **A low-power VLSI seizure detector is presented. It combines a 256-channel analog neural recording chip and a low-power synthesized digital VLSI processor. The processor computes the bivariate phase synchronization on any two neural inputs from a set of 256 and their instantaneous magnitude. For experimentation with in vitro epilepsy models, a low-cost technique to implement on-chip gold microelectrodes was utilized. Results are shown using an in vitro low Mg2+ mouse epilepsy model and human EEG data.**

I. Introduction

Over 40 million people worldwide suffer from epilepsy. Approximately one-third of epilepsy patients do not respond well to currently available treatments such as antiepileptic drugs [1]. Electrical stimulation of the brain has shown promise in reducing the frequency of seizures in some patients with intractable epilepsy [1], [2], [3].

A closed-loop responsive electrical stimulation device which detects an onset of a seizure and provides a corresponding stimulus can yield lower power dissipation compared with a device that stimulates continuously. This results in a smaller device and fewer surgical operations to recharge or replace the battery [4]. It may also improve the efficacy of seizure control.

Low-power seizure detection hardware implementations have been demonstrated which employ extracting energy bands [5], root-mean-squared (RMS), maximum-minimum, line-length and nonlinear energy [6] and analog wavelet filtering [4], [7] and [8]. These algorithms are typically univariate, i.e. operating on one neural signal at a time. They are selected to minimize power dissipation making VLSI implementation feasible. More advanced algorithms which operate on signals from two or more recording sites simultaneously (bivariate or multivariate, respectively) such as computing the phase synchronization among neural signals can improve the accuracy of seizure detection [9], [10]. Typically these have been demonstrated in software as they are too computationally intensive and thus draw too much power for an implantable device. We previously demonstrated a low-power bivariate VLSI processor architecture [11] that computes the magnitude and phase synchronization between two neural signals. This architecture is employed in this work.

We present a multivariate implantable seizure detector that is realized by combining a synthesized digital VLSI processor based on the architecture in [11] with a 256-channel neural recording chip. On-chip gold electrodes yield a low-cost experimental setup for use with in vitro animal epilepsy models. The rest of the paper is organized as follows. Section II discusses the VLSI architecture of the seizure detector. Section III presents the VLSI implementation of the neural recording chip and the phase sychnronization processor. Section IV contains seizure detection results from extracellular recordings in a mouse hippocampus. Results of seizure detection in humans are also summarized.

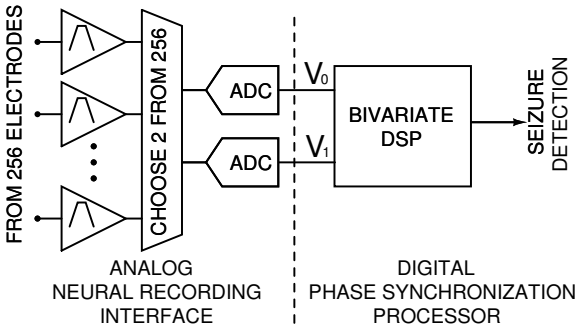

Fig. 1. Top-level seizure detector architecture.

II. VLSI Architecture

The multivariate seizure detector combines two components: a low-power multichannel analog neural recording interface chip [12] and a low-power digital phase synchronization processor [11] as shown in Figure 1. 256 low-noise amplifiers filter and amplify the neural signals. Any two neural signals from the 256 available neural recording channels on the chip can be selected. Next, two analog-to-digital converters (ADCs) convert the two selected neural signals into the digital domain. The two digital signals are sent to the bivariate DSP processor to compute the phase synchronization and magnitude, and then process the data to detect a seizure. Multiple pairs of neural signals can be used as inputs within a single detection time window which enables multivariate signal processing.

III. VLSI Implementation

A. Analog Neural Recording Interface

The 256-channel neural amplifier bank [12] was used to amplify the neural signals. The chip contains an array of 16

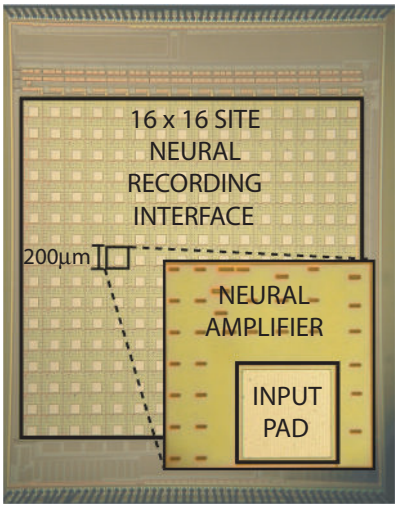

Fig. 2. Micrograph of the analog integrated neural recording interface implemented in a 0.35μm CMOS technology [12].

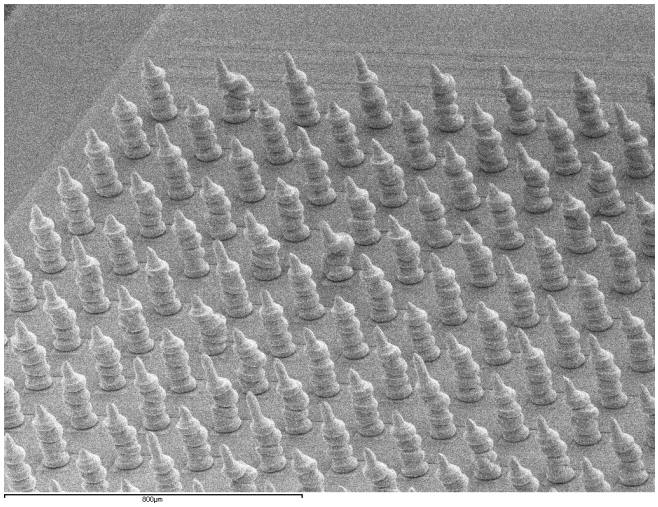

Fig. 3. SEM photograph of microelectrodes fabricated on the surface of the analog neural recording interface chip.

by 16 amplifiers, each 200μm in width as shown in Figure 2. Each amplifier has a maximum programmable bandwidth of 10Hz to 5kHz, exhibits an input-referred noise of 7μV over this band, and has a gain of 1000V/V and power dissipation below 10μW. The microchip was fabricated using a standard 0.35μm CMOS technology and operates from a 3.3V supply.

For experimentation with in vitro epilepsy models, a technique to implement on-chip microelectrodes was utilized. Gold stud bumps were fabricated using a standard wire bonding technology. Four gold-bumps are stacked on top of each other to yield an electrode having an average height of 180μm with a sharp tip to penetrate the neural tissue. Each bondpad on the chip is connected to an input of one of the neural recording channels as shown in the inset of Figure 2 and is directly connected to the gold electrodes depicted in Figure 3. This allows the neural tissue to be placed directly on the surface of the chip. The on-chip electrodes were validated to be functional in recording of epileptic activity from an intact mouse hippocampus in vitro.

B. Digital Phase Synchronization Processor

The digital phase synchronization processor signal path architecture is shown in Figure 4. The inputs are filtered using a high-Q bandpass filter to extract the neural band of interest such as the 30-40Hz frequency band. The bivariate DSP processor first converts the two digitized complex inputs to their real and imaginary components using two sets of FIR filters, one which implements an all-pass digital delay and the other which implements the Hilbert transform to introduce a 90-degree phase shift. Next, the instantaneous phase of each neural signal is computed from its real and imaginary components. The bivariate phase synchronization is then quantified using a phase locking value (PLV):

$$PLV = \frac{1}{N}\sqrt{(\sum_{i=0}^{N-1} sin(\Delta\phi_i))^2 + (\sum_{i=0}^{N-1} cos(\Delta\phi_i))^2} \quad (1)$$

where N is the length of the moving-average FIR filters and $\Delta\phi_i$ is the instantaneous phase difference between the two neural signals in their i-th sample. The univariate magnitude is also computed directly from the real and imaginary components of the two neural signals

$$MAG(V_j) = \sqrt{Re(V_j)^2 + Im(V_j)^2} \quad (2)$$

where $j = 0, 1$. It represents the instantaneous magnitude in the filtered frequency band of interest. When the PLV drops below a threshold and the magnitude increases above a certain value, both averaged and median filtered, a seizure is detected.

The 10-bit processor was synthesized using a standard 0.13μm CMOS technology. It utilizes 41000 digital gates and occupies an area $0.178mm^2$. It employs three Coordinate Rotation Digital Computer (CORDIC) cores as shown in Figure 4 and dissipates approximately 1.1μW per channel when computing at 1kS/s from a 1.2V supply. The all-pass and Hilbert transform filters as shown in Figure 4 have a delay of 16 samples. The moving average FIR filters have a delay of 32 samples. This results in a total latency of 16 samples when computing the magnitude and 48 samples when computing the PLV function. Increasing the sample rate of the system can minimize the latency while trading off power dissipation.

IV. Results

Two off-chip tungsten electrodes and the analog neural recording interface chip were used to record epileptic neural activity. The in vitro recordings use a low-Mg epileptic seizure model in an intact hippocampus of a mouse. Hippocampus is obtained from C57/BL mice aged P10-14. Animals are

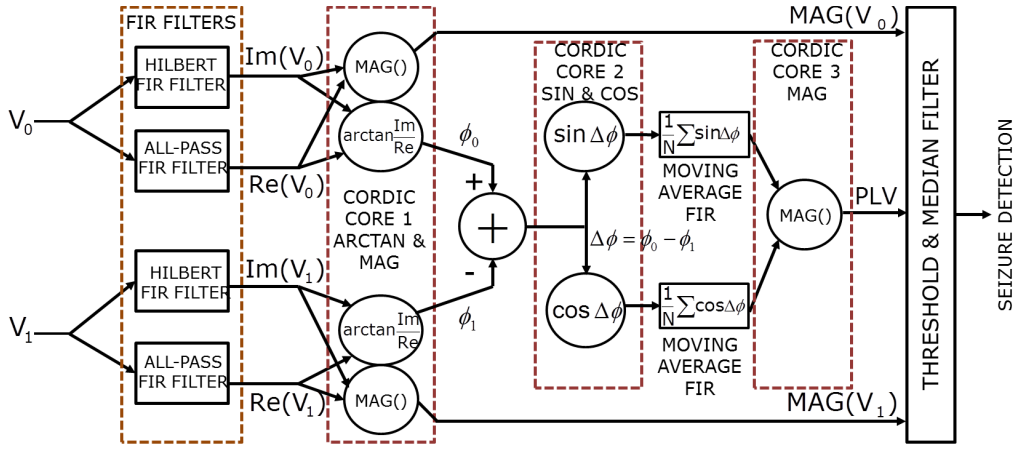

Fig. 4. VLSI architecture of the bivariate DSP that performs seizure detection by computing the magnitudes and the phase synchronization of two neural signals.

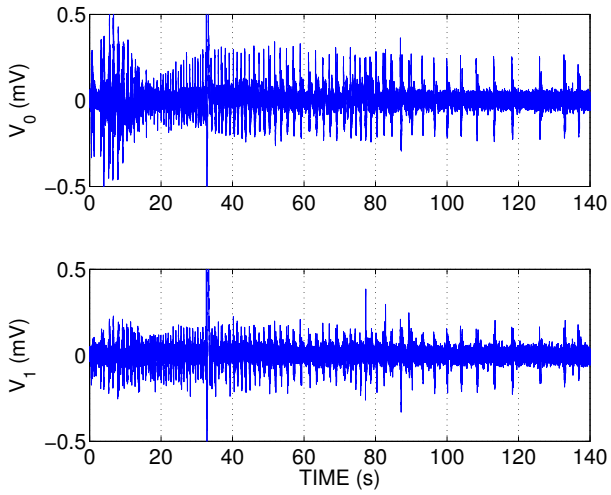

Fig. 5. Epileptic seizure-like neural activity recorded simultaneously on two channels of the neural amplifier chip. A mouse hippocampus was perfused with a low-Mg2+ solution to invoke epileptic activity.

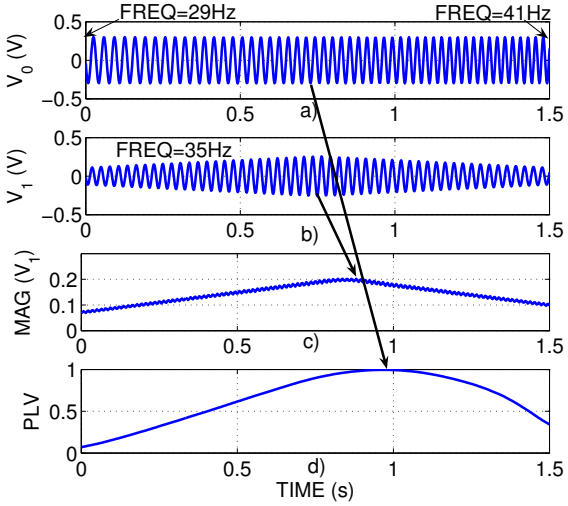

Fig. 6. a) The first input has constant amplitude with frequency linearly increasing from 29Hz to 41Hz. b) The second input has a constant frequency set to 35Hz and an amplitude which follows a ramp envelope. c) The magnitude of the second input and d) the PLV between two inputs computed by the digital processor.

anesthetized with halothane and decapitated in accordance with the Canadian Animal Care Guidelines. The hippocampus is kept inside a circulating-heated artificial cerebrospinal fluid (ACSF). An example of a seizure recorded from two neural recording channels of the chip is shown in Figure 5. All neural signals are then band pass filtered in the 30-40Hz frequency range.

Results of a Simulink model simulation demonstrating the bivariate DSP operating on two sample signals are shown in Figure 6. The resolution and the accuracy of the Simulink model were set to match the performance of an RTL-level simulation of the synthesized processor. One signal has a constant amplitude and its frequency varies linearly between 29Hz to 41Hz. The second signal is held at a constant frequency of 35Hz and has a saw-tooth envelope amplitude. The processor computes the magnitude which follows the envelope of the 35Hz sinusoid as shown in Figure 6(c). Lastly, the PLV is computed, and it peaks near the center of Figure 6 as both frequencies are set to 35Hz. The latency in Figures 6(c) and (d) marked by the two arrows is due to the delay in the moving average FIR filters.

The recorded data from the chip were digitized by two on-board ADCs and were input into the processor Simulink model off-line. Approximately three hours of data are shown in Figure 7. Figures 7(a) and 7(b) display the raw data of the epileptic activity recorded by the analog neural recording chip from an intact mouse hippocampus. At least six seizure-like events can be observed. Figure 7(c) depicts the magnitude of

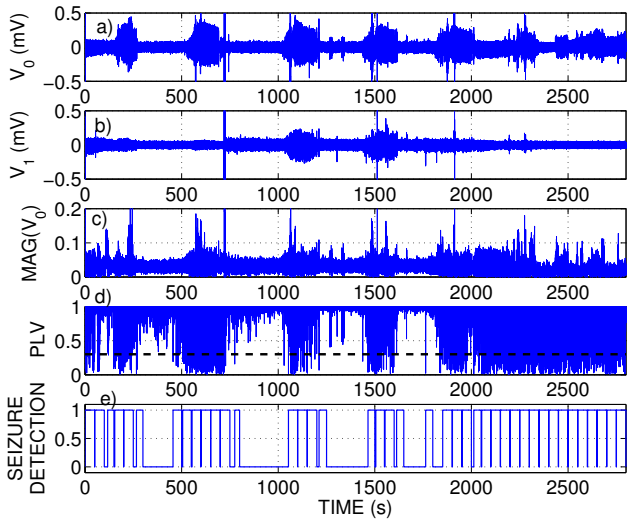

Fig. 7. Experimental results of seizure-like event detection in low-Mg2+ mouse epilepsy model. (a), (b) Two input neural signals recorded by the analog neural recording interface chip. c) Magnitude of the signal shown in (a) after it is bandpass filtered in the 30Hz to 40Hz frequency range. d) PLV in the 30-40Hz frequency band computed between the two inputs. e) Result of thresholding and median filtering of the PLV waveform to determine if a seizure occurs.

the signal shown in Figure 7(a) in the 30Hz to 40Hz frequency band computed by the processor. During each seizure, the magnitude increases at least two-fold over the noise floor. The processor also computes the phase synchronization between the two neural inputs. The resulting PLV is shown in Figure 7(d), with a threshold set to 0.3. The result of thresholding depicted in Figure 7(e) indicates if a seizure is present. A seizure is detected if the average PLV drops below 0.3. True detection and false positives can be traded off by adjusting the threshold. The in-band (i.e. 30-40Hz) magnitude, as it is amplitude dependent, is much more susceptible to artifacts when compared to the frequency dependent phase synchronization between two inputs. This can be observed in Figure 7. Other frequency bands besides the 30-40Hz band for this animal seizure model did not exhibit useful information for phase synchronization, but still contained additional magnitude information.

The proposed seizure detector was also validated in recorded EEG data from multiple human subjects. Using the EEG human data from [13] we computed a true positive rate (TPR) of close to 70 percent with a false positive rate (FPR) of 0.67 false positives per hour (FPH). The detection and false-positive rates are comparable to those of computationally complex software based phase synchronization seizure detection algorithms [14], [15].

V. Conclusions

A low-power VLSI seizure detector combines a 256-channel analog neural recording interface chip and a synthesized digital phase synchronization processor model. Results from an in vitro mouse hippocampus using low-Mg2+ epilepsy model demonstrate the functionality of the multivariate seizure detector in the animal model. Promising off-line seizure detection results in human patients are also reported. The integration area is $0.08mm^2$ per pair of neural recording channels and $0.178mm^2$ for the digital processor. The power dissipation is $25\mu W$ per pair of neural recording channels and $1.1\mu W$ for the processor. These specifications are well within the requirements for neurological electronic implants in humans.

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