# Brain–Silicon Interface for High-Resolution *in vitro* Neural Recording

Joseph N. Y. Aziz, *Student Member, IEEE*, Roman Genov, *Member, IEEE*, Berj L. Bardakjian, *Member, IEEE*, Miron Derchansky, and Peter L. Carlen

*Invited Paper*

***Abstract*—A 256-channel integrated interface for simultaneous recording of distributed neural activity from acute brain slices is presented. An array of 16 × 16 Au recording electrodes are fabricated directly on the die. Each channel implements differential voltage acquisition, amplification and band-pass filtering. In-channel analog memory stores an electronic image of neural activity. A 3 mm × 4.5 mm integrated prototype fabricated in a 0.35-$\mu$m CMOS technology is experimentally validated in single-channel extracellular *in vitro* recordings from the hippocampus of mice and in multichannel simultaneous recordings in a controlled environment.**

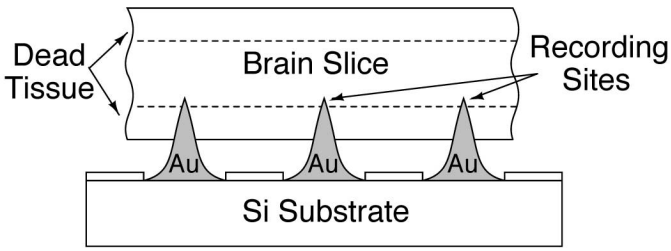
***Index Terms*—Acute brain slices, integrated neural interfaces, neural amplifier, on-chip microelectrodes.**

## I. Introduction

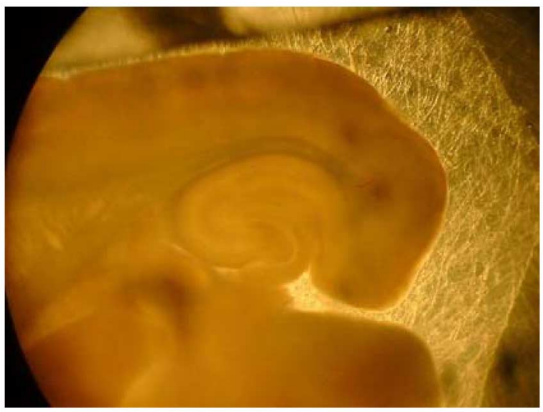
THE electrophysiology of the human brain governs a complex array of neurological functions. The human brain is a large-scale interconnected network with common behavioral properties extending across large spatial areas. To gain full understanding of how biological neural networks encode and process information, it is necessary to simultaneously record signals from many neighboring neurons.

Significant insights have been gained into ways of neural information coding through the use of microelectrodes that record the activity of single neurons and neural populations in the brain. Recording of neural activity has been traditionally performed using bench-top biomedical instrumentation equipment. These instruments are generally stationary, bulky, limited to one or a few acquisition channels, and prone to excessive noise due to wiring. Integrated neural interfaces, fabricated on a single miniature physical substrate, lack these drawbacks. They offer a small, low-power, low-noise, and cost effective chronically implantable alternative to commercial bench-top instruments. Integrated neural interfaces perform signal acquisition, amplification, filtering, and, in some instances, quantization and neural stimulation [1]–[7]. They may also provide wireless data interface on the same chip [8].

Recording microsystems with 3-D electrode arrays of various configurations have been reported such as with electrodes co-planar with the die [9]. Implementations with 3-D electrode arrays bonded directly to the surface of the chip have been proposed [6], [10]. Previously reported neural interfaces integrated with on-chip 3-D microelectrodes have been typically limited to 100 channels [10]. Implementations with higher number of




*(a)*



*(b)*

Fig. 1. (a) Cross section of the proposed microsystem for recording from acute brain slices. (b) Mouse hippocampal-entorhinal cortex slice in a recording chamber.

Manuscript received December 21, 2006; revised January 15, 2007. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada (NSERC) and Krembil Fund. This paper was recommended by Associate Editor R. Butera.

J. N. Y. Aziz was with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M4Y 2P8, Canada. He is now with Broadcom Corporation, 757716 Singapore.

R. Genov is with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M4Y 2P8, Canada (e-mail: roman@eecg.utoronto.ca).

B. L. Bardakjian is with the Institute of Biomaterials and Biomedical Engineering, Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada (e-mail: berj@cbl.utoronto.ca).

M. Derchansky, and P. L. Carlen are with the Toronto Western Research Institute and the Department of Physiology, University of Toronto, Toronto, ON M4Y 2P8, Canada (e-mail: carlen@uhnres.utoronto.ca).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TBCAS.2007.893181

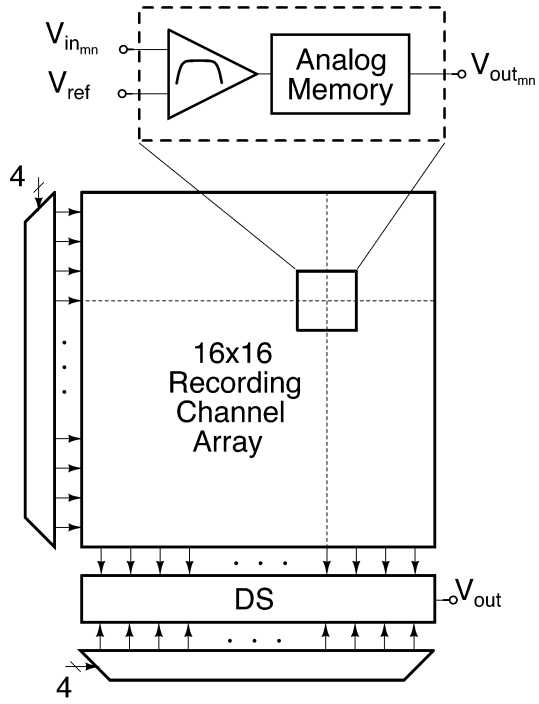



Fig. 2. Top-level architecture of the brain–silicon interface.

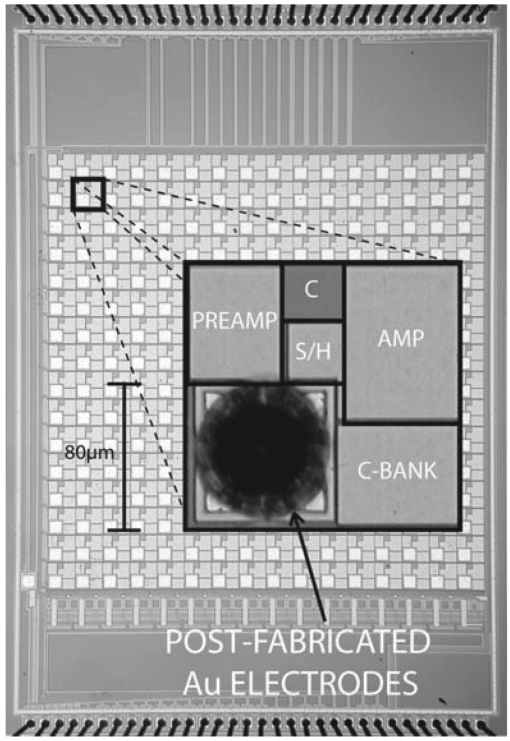



Fig. 3. Micrograph of the 256-channel integrated neural interface. The $3 \times 4.5$ $mm^2$ die was fabricated in a 0.35-$\mu$m CMOS technology. Electrode pitch is 170 $\mu$m.

channels have been reported without electrodes and at the cost of increased circuit noise [11].

We present a CMOS brain–silicon interface for high-resolution *in vitro* recording from acute brain slices. Neurophysiological studies of acute brain slices such as those of hippocampus are critical in investigating therapies for such debilitating neurological disorders as epilepsy and Alzheimer's disease. A region of interest in the brain is extracted from an animal and sliced. The thickness of a slice is typically in the order of several hundreds of microns. As a result of slicing, acute brain slices have an outer layer of dead tissue which needs to be penetrated by recording electrodes. Its thickness can be in the order of tens of microns. For this purpose, golden 3-D electrodes are post-fabricated on the surface of the die of the proposed integrated neural recording interface. The cross section of the proposed microsystem is depicted in Fig. 1(a). Au electrodes are individually bonded directly onto the surface of the chip employing conventional die bonding equipment. This fabrication method yields low manufacturing costs, high yield, and flexibility in electrode location and shape. The size and geometry of the electrodes are chosen specifically for recording from acute brain slices of mice such as the hippocampal-entorhinal cortex slice shown in Fig. 1(b). The slice is inserted onto the recording electrodes and is placed into a fluidic chamber. The slice rests on the bases of the electrodes and is held in place by a slice anchor (or harp). This allows the tissue slice to be perfused from both above and below in order to maintain its vitality.

Each channel of the integrated neural interface contains a low-noise amplifier with up to 74 dB of programmable gain, a tunable antialiasing low-pass filter (LPF), and a high-pass filter (HPF) that removes a dc voltage offset present at the electrode-tissue interface. The brain–chip interface records action potentials in the range of tens of microvolts to hundreds of millivolts in the tunable 0.1–10 kHz frequency band in order to capture relevant neural activity, as required for analysis and treatment of neurological disorders [12]. Each channel also has a sample-and-hold circuit with analog memory, allowing for truly simultaneous signal acquisition across all channels, with subsequent multiplexed array readout and off-chip serial analog-to-digital conversion. A column-parallel double-sampling circuit removes fixed pattern noise.

The rest of this paper is organized as follows. Section II presents the architecture of the integrated prototype and describes the electrode manufacturing process. Section II-C provides details of VLSI implementation of the recording channel. The low-noise transconductance amplifier is presented in Section II-D. The recording frame buffer implementation is described in Section II-E. All presented results are experimentally recorded from the integrated prototype.

## II. Architecture and VLSI Implementation

### A. Architecture

Most of the frequency content of extracellular neural activity in the brain is concentrated between 0.1 Hz and 10 kHz. Signal amplitudes range from a few microvolts to hundreds of millivolts. For low-noise distributed neural potential field recording, a multichannel integrated neural interface has been designed and prototyped.

The presented neural interface simultaneously acquires voltages on 256 independent channels organized in a $16 \times 16$ array as shown in Fig. 2. Each channel contains a band-pass filter

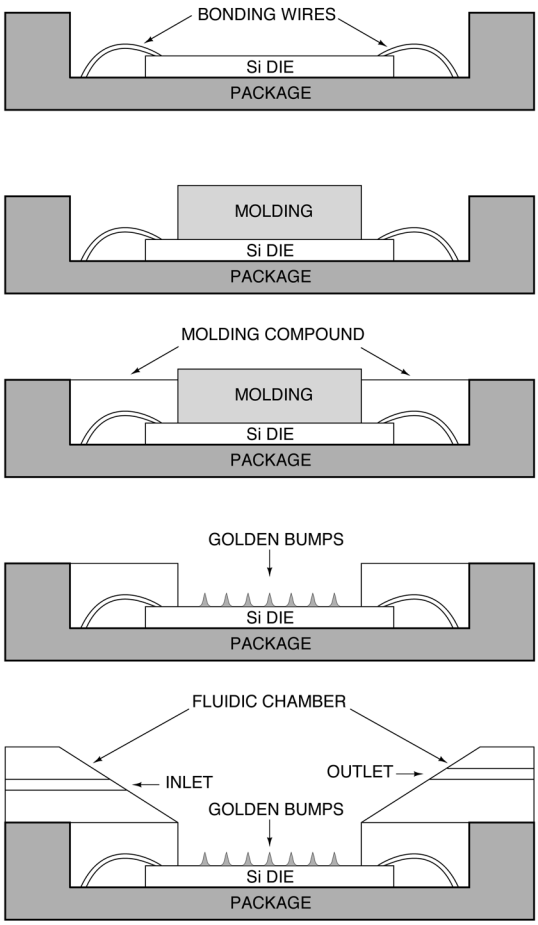



Fig. 4. Fabrication steps in the the brain–silicon interface hybrid integration procedure.

with a nominal amplification gain. Each channel also contains a sample-and-hold (S/H) cell. A bank of double sampling (DS) circuits sample the analog memories one row at a time to remove offsets resulting from device mismatches. Array readout is implemented in a serial fashion as controlled by row and column address decoders.

The 256-channel integrated neural interface was fabricated in a 0.35-$\mu$m double-poly standard CMOS technology. The 3 mm $\times$ 4.5 mm die micrograph is shown in Fig. 3. Each channel is connected to one on-chip data recording site and a reference recording site, for low-noise differential recording. Each recording site is comprised of a stack of several aluminum layers with the topmost layer left unpassivated similarly to a conventional bonding pad. One on-chip reference recording pad is shared by all recording channels. An off-chip reference voltage can also be supplied from an external recording electrode.

### B. Microsystem Integration

*In vitro* neural recording procedure requires preserving the vitality of a brain slice by its continuous perfusion. The perfusion fluid such as as artificial cerebrospinal fluid (ACSF) is electrically conductive. The close proximity of bonding wires to the recording array necessitates their electrical insulation. To simplify the process of electrical insulation of bonding wires all wire-bonded pads are located on the two opposite sides of

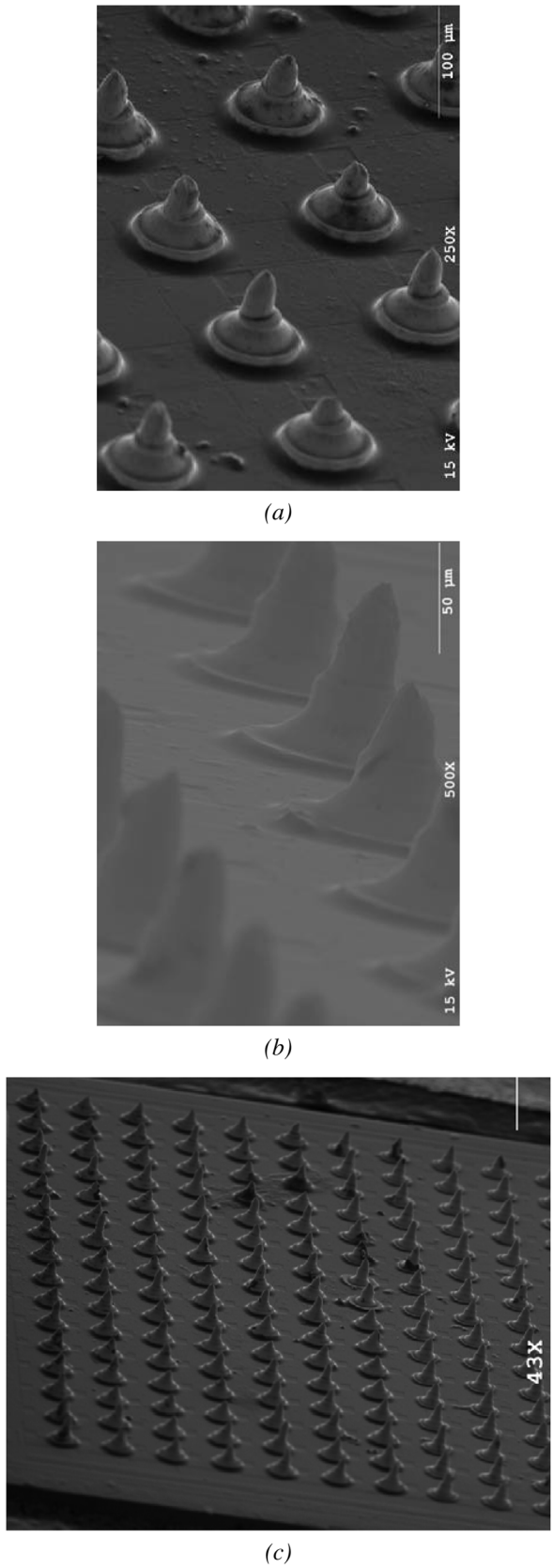



Fig. 5. SEM photographs of golden electrodes fabricated on the surface of the chip. (a) Midangle view. (b) Low-angle view. (c) Partial array view.

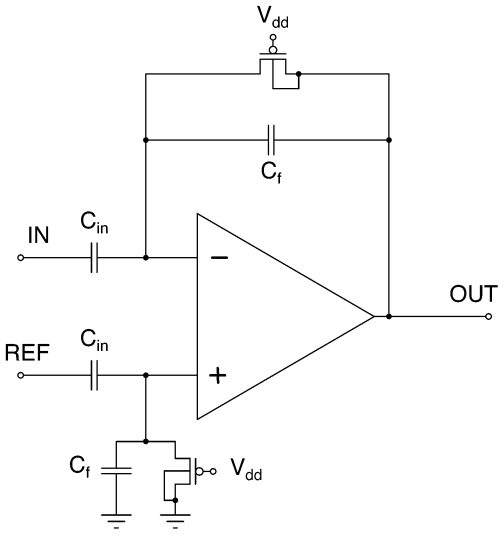



Fig. 6. Circuit diagram of the first stage of the recording channel.

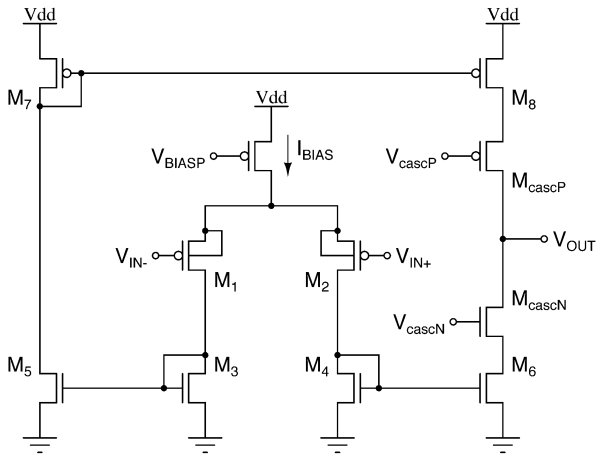



Fig. 7. Current-mirror OTA circuit diagram.

the die as shown in Fig. 3. A margin of several hundred microns between the array and the wire-bonded pads on each of the two sides of the die relaxes the precision requirements on the bonding wires insulation process.

The microsystem electrode-silicon hybrid integration process is comprised of several fabrication steps as depicted in Fig. 4. The neural recording die is packaged in an open-cavity ceramic package. To make a recording well for holding a mouse hippocampal slice, a prefabricated rectangular rubber molding is placed on the surface of the recording array. The molding size is approximately 4 mm $\times$ 12 mm as needed for a typical mouse hippocampal slice. With pressure applied to the surface of the molding, a biocompatible dental molding compound is poured around the molding. The molding compound fills the package cavity flash with its surface. The resulting recording well electrically insulates and mechanically protects all bonding wires. The surface of the die is plasma-cleaned to eliminate any residual contamination. Golden electrodes are then fabricated on the surface of the partially encapsulated die as described in more detail below. A machined bio-compatible plexiglass fluidic chamber is placed on the surface of the package with its rectangular tapered opening aligned with the fabricated recording well. A liquid gasket waterproofs the gap between the package and the fluidic chamber. Two horizontal circular openings in the fluidic chamber serve as an inlet and an outlet for the perfusion fluid.

The recording electrodes are fabricated utilizing conventional die-bonding equipment. Golden studs are manufactured on nonpassivated aluminum recording pads by attaching melted gold to the pads, stretching it up, and breaking it off at a controlled height. The diameter of the base of an electrode is 80 $\mu$m. A typical electrode has a tapered shape with the tip of several microns in diameter. The height of each electrode is approximately 100 $\mu$m. This geometry is optimum for recording from acute hippocampal slices as it allows to penetrate the dead outer layer of an acute brain slice and perform a localized recording from within the live layer of the tissue. A set of three scanning electron microscopy (SEM) photographs of the fabricated electrodes at different angles is shown in Fig. 5.

### C. Recording Channel

The primary function of the acquisition channel is to amplify the weak neural signal with minimal circuit noise and nonlinearities added to the output while consuming little power. Power dissipation is limited so that the surrounding tissue is not damaged by heat. Due to electrochemical effects at the tissue-electrode interface, dc voltage offsets several orders of magnitude above the actual signal level are common [5]. The recording channel requires a HPF to prevent the dc component from saturating the amplifiers. Sampling of the signal requires an antialiasing LPF. Post processing of the neural recording is performed in the discrete domain by means of switched capacitor circuits.

As a high closed-loop gain is required in the recording channel, it employs a two-stage amplifier. This yields higher linearity and maintains capacitor sizes within the recording cell pitch requirement. Fig. 6 shows the circuit diagram of the first stage of the recording channel. The first stage is a continuous-time difference amplifier. The channel inputs are capacitively coupled to the first stage operational transconductance amplifier (OTA) which insures dc input rejection of the amplifier. To achieve a subhertz HPF cut-off frequency a large resistor, in the order of gigaohms, should be employed in the feedback network. A linear resistance with such value consumes large silicon area. Therefore, the resistive element is implemented as a MOS device biased in the subthreshold region [5], [13]. The second stage is a single-ended capacitively coupled continuous-time amplifier.

For truly simultaneous multichannel recording, the output of the two-stage amplifier is sampled by a switched capacitor sample-and-hold circuit. The voltage is stored on a capacitor buffered by a source follower with a column-shared current source. To prevent aliasing, the cut-off frequency of the LPF is set by the bias current of the first stage OTA.

### D. Low-Noise Transconductance Amplifier

An important factor in the channel design is the amount of noise added by the sensing circuits. The challenge in designing a low-noise amplifier for this application is to optimize the noise

TABLE I
TRANSISTOR SIZES AND OPERATING POINTS

| Transistor | W/L ($\mu m$) | $I_D(nA)$ | $g_m(\mu A/V)$ | $g_m/I_D(V^{-1})$ |
|---|---|---|---|---|
| $M_{1,2}$ | 400/15 | 125 | 3.14 | 25.17 |
| $M_{3-6}$ | 10/400 | 125 | 0.83 | 6.64 |
| $M_{7,8}$ | 10/200 | 125 | 0.65 | 5.2 |
| $M_9$ | 45/45 | 250 | 3.79 | 15.16 |
| $M_{cascN}$ | 18/8 | 125 | 3.1 | 24.8 |
| $M_{cascP}$ | 25/8 | 125 | 2.65 | 21.2 |

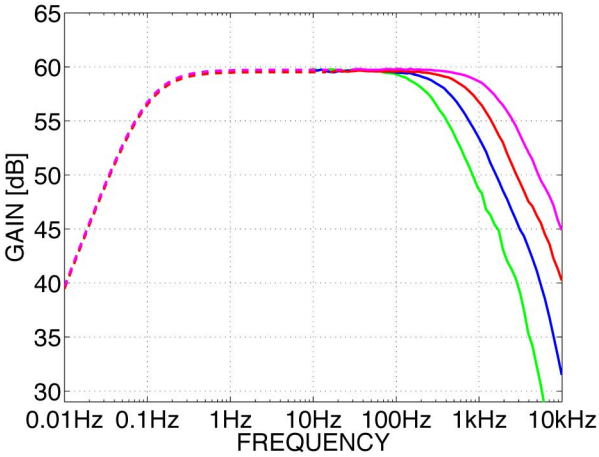



Fig. 8. Experimentally measured frequency response of a single recording channel. Bandwidth can be varied by adjusting the bias current.

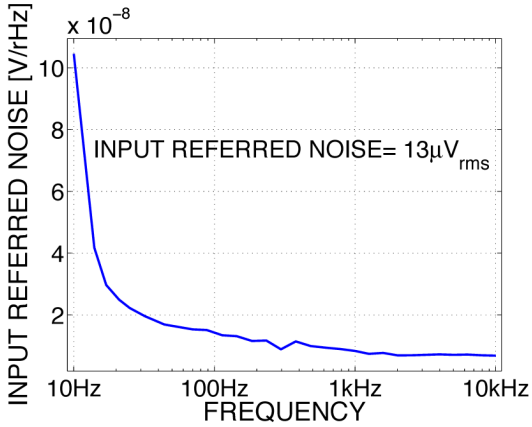



Fig. 9. Experimentally measured input-referred noise of a single recording channel.

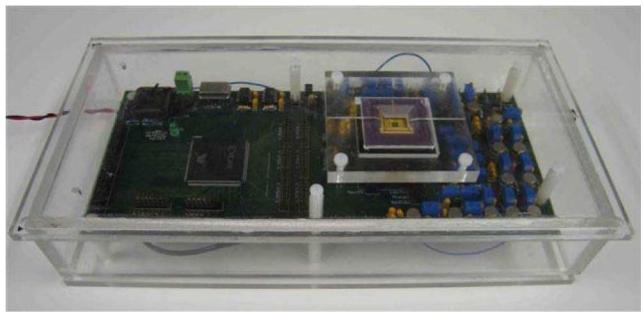


Fig. 10. Fluidic chamber attached to the top of the testing printed circuit board.

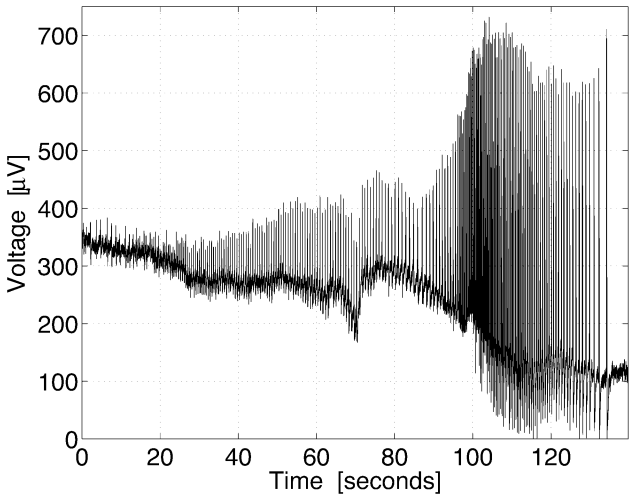



Fig. 11. Epileptic seizure in a mouse hippocampus experimentally recorded on one channel of the integrated neural interface.

performance given a small power budget. Fig. 7 shows the circuit diagram of the OTA employed in each stage of the channel.

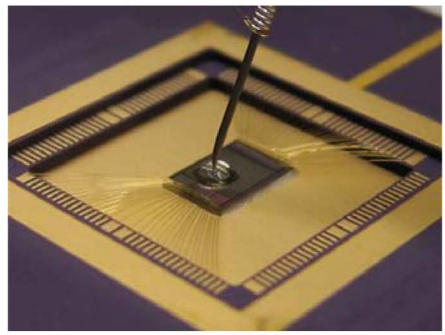
The input pair is chosen to be a p-channel MOS with a large gate area to minimize the flicker noise contribution. According to the circuit noise analysis presented in [5] and [14], the thermal noise component of the OTA can be reduced by biasing the input pair $(M_{1,2})$ in week inversion and the mirroring transistors $(M_{3-8})$ in strong inversion. Thus, the thermal noise contribution is optimized for a given current value. The thermal noise level can be further decreased by increasing the biasing current and thus the power consumption. Table I summarizes the size and the dc operating point for each transistor.

Fig. 8 depicts the experimentally measured frequency response of a single channel configured for a nominal gain of 1000 (60 dB). The solid line represents the measurements done with a spectrum analyzer. Due to limitations of the available measurement equipment, the high-pass corner frequency is estimated by applying a step signal at the amplifier input and observing the amplifier transient response time constant.

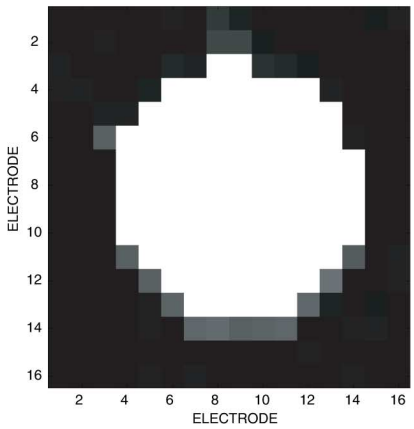
Fig. 9 shows the experimentally measured input referred noise of one channel. The measurement is obtained by recording the noise spectrum at the output of the amplifier and referring it back to the input. The total rms noise is 13 $\mu$V over the 10 Hz–10 kHz bandwidth.

For experimental recordings the neural recording interface prototype is placed in a custom-manufactured fluidic chamber. The fluidic chamber is positioned on the surface of the chip package and attached to the top of a protective plexiglass box to form a hydraulic seal as shown in Fig. 10. The testing printed circuit board generates necessary analog and digital signals, quantizes recorded neural data and sends the data to a personal computer through a high-speed digital interface. The recorded data are buffered and displayed in Matlab.

Fig. 11 depicts an extracellular neural activity recording from a mouse hippocampus performed on one channel of the integrated neural interface prototype. Hippocampus was obtained



*(a)*




*(b)*

Fig. 12. (a) Water drop placed on the surface of the die. (b) 2-D experimental recording of a water drop driven by a sinusoidal signal.

from male Wilstar rats (5–25 days old). Animals were anesthetized with halothane and decapitated in accordance with the Canadian Animal Care Guidelines. The brains were dissected and maintained in oxygenated ice-cold ACSF. The recording represents an epileptic seizure-like activity induced *in vitro* in the presence of low $Mg^{2+}$ ACSF.

### *E. Frame Buffer*

Accurate distributed multisite sensing requires maintaining a high degree of correlation in time between all channels. Multisite recording time-multiplexed architectures do not preserve cross-channel correlation unless the sampling frequency is much higher than the neural signal bandwidth. This necessitates a memory buffer in each recording cell to store the sampled signal. Frames of samples across the whole array are captured simultaneously. This eliminates the rolling delay during serial read-out. The local memory cell also allows for delaying high-noise on-chip digital switching until after a recording has been completed. Low-noise signal acquisition is time-multiplexed with high-noise peripheral switch capacitor signal processing and read-out. This ensures no high-amplitude switching activity during the signal acquisition phase and thus prevents substrate noise from coupling into the low-amplitude signal being acquired.

TABLE II
EXPERIMENTALLY MEASURED CHARACTERISTICS

| | |
|---|---|
| Channels | 256 |
| Max Sampling Rate | 40kHz |
| Programmable Gain | 200, 1000, 2500, 5000 |
| Input-Referred RMS Voltage Noise | $13\mu V$ over 10kHz |
| Output Voltage Range | 1.5V |
| DC Offset Compensation | Double Sampling |
| LPF cut-off Frequency | 1kHz-10kHz |
| HPF cut-off Frequency | $<$0.1Hz |
| Supply Voltage | 3.3V |
| Core Power Dissipation | 6mW |
| Technology | $0.35\mu m$, mixed-signal CMOS, double poly |
| Electrode Type | On-chip, Au; $100\mu m$ |
| Cell Pitch | $170\mu m$ |
| Die Size | $3\times4.5\ mm^2$ |

In order to validate the 2-D recording functionality of the array the following experiment was conducted. A drop of distilled water was placed on the surface of the $16 \times 16$ electrode array similarly to the one shown in Fig. 12(a) and driven by a 2-mV peak-to-peak sinusoidal voltage. The stimulus signal was recorded at 5-kHz sampling rate and displayed in real time as an "electronic video" stream. Fig. 12(b) shows a two dimensional intensity map of a recording frame corresponding to a particular instantaneous value of the input sinusoid.

The experimentally measured characteristics are summarized in Table II. The measured core power dissipation of 6 mW on the $3 \times 4.5$ mm$^2$ die area falls within the limits of power density considered safe for brain tissue [15], [16].

## III. CONCLUSION

We have presented the architecture and VLSI implementation of an integrated neural interface for simultaneous recording of distributed neural activity. A 3 mm $\times$ 4.5 mm integrated prototype was fabricated in a 0.35-$\mu$m CMOS technology. Two hundred fifty-six (256) 100-$\mu$m low-cost Au electrodes were fabricated directly on the surface of the chip for high-resolution electronic imaging of neural activity in acute brain slices. The microsystem was validated in extracellular *in vitro* recordings from a mouse hippocampus.

## ACKNOWLEDGMENT

The authors would like to thank the Canadian Microelectronics Corporation (CMC), Kingston, ON, Canada, for providing chip fabrication services.

## REFERENCES

[1] J. Aziz and R. Genov, "Multi-channel integrated neural interfaces for distributed electro-chemical sensing," in *Proc. IEEE Midwest Symp. Circuits Syst.*, Aug. 2005, pp. 1782–1785.

[2] J. Aziz and R. Genov, "Electro-chemical multichannel integrated neural interface technologies," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2006, pp. 2201–2204.

[3] M. Naware, A. Rege, R. Genov, M. Stanacevic, G. Cauwenberghs, and N. Thakor, "Integrated multielectrode fluidic nitric-oxide sensor and VLSI potentiostat array," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2004, vol. 4, pp. 25–28.

[4] M. Stanacevic, K. Murari, G. Cauwenberghs, and N. Thakor, "16-channel wide-range VLSI potentiostat array," in *Proc. IEEE Int. Workshop Biomed. Circuits Syst.*, Dec. 2004, pp. 17–20.
[5] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applicatoins," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.
[6] W. Patterson, Y. Song, C. Bull, I. Ozden, A. Deangellis, C. Lay, J. McKay, A. Nurmikko, J. Donoghue, and B. Connors, "A microelectrode/microelectronic hybrid device for brain implantable neuroprosthesis applications," *IEEE Trans. Biomed. Eng.*, vol. 51, no. 10, pp. 1845–1853, Oct. 2004.
[7] R. Genov, M. Stanacevic, M. Naware, G. Cauwenberghs, and N. Thakor, "VLSI multichannel track-and-hold potentiostat," in *Proc. SPIE Bioengineered Bioinspired Syst.*, Apr. 2003, vol. 5119, pp. 117–128.
[8] P. Mohseni and K. Najafi, "A battery-powered 8-channel wireless FM IC for biopotential recording applications," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2005, pp. 560–562.
[9] R. H. Olsson and K. D. Wise, "A three-dimensional neural recording microsystem with implantable data compression circuitry," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2796–2804, Dec. 2005.
[10] R. Harrison, P. Watkins, R. Kier, R. Lovejoy, D. Black, R. Normann, and F. Solzbacher, "A low-power integrated circuit for a wireless 100-electrode neural recording system," in *Proc. IEEE Int. Conf. Solid-State Circuits Dig. Tech. Papers*, Feb. 2006, pp. 2258–2267.
[11] B. Eversmann, M. Jenkner, F. Hofmann, C. Paulus, R. Brederlow, B. Holzapfl, P. Fromherz, M. Merz, M. Brenner, M. Schreiter, R. Gabl, K. Plehnert, M. Steinhauser, G. Eckstein, D. Schmitt-Landsiedel, and R. Thewes, "A $128 \times 128$ CMOS biosensor array for extracellular recording of neural activity," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2306–2317, Dec. 2003.
[12] J. Aziz, R. Karakiewicz, R. Genov, B. L. Bardakjian, M. Derchansky, and P. L. Carlen, "Real-time seizure monitoring and spectral analysis microsystem," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2006, pp. 2133–2136.
[13] T. Delbruck and C. A. Mead, "Adaptive photoreceptor with wide dynamic range," in *IEEE Int. Symp. Circuits Syst.*, Jun. 1994, pp. 339–342.
[14] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed. New York: McGraw-Hill, 2000, ch. 7, pp. 233–239.
[15] T. M. Seese, H. Harasaki, G. M. Saidel, and C. Davies, "Characterization of tissue morphology, angiogenesis, and temperature in the adaptive response of muscle tissue in chronic heating," *Lab. Invest.*, vol. 78, pp. 1553–1562, 1998.
[16] S. Kim, R. A. Normann, R. Harrison, and F. Solzbacher, "Preliminary study of the thermal impact of a microelectrode array implanted in the brain," in *Proc. IEEE Eng. Med. Biol. Conf.*, Sep. 2006, pp. 2986–2989.

**Joseph N. Y. Aziz** (S'05) received the B.Sc. degree in electronics and electrical communications engineering from Cairo University, Giza, Egypt, in 2003, and the M.A.Sc. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2007.

He is currently with Broadcom Corporation, Singapore. His current research interests focus on the design of mixed-signal integrated circuits.

**Roman Genov** (S'96–M'02) received the B.S. degree (first rank) in electrical engineering from Rochester Institute of Technology, Rochester, NY in 1996, and the M.S. and Ph.D. degrees in electrical and computer engineering from The Johns Hopkins University, Baltimore, MD, in 1998 and 2002, respectively.

He held engineering positions at Atmel Corporation, Columbia, MD, in 1995 and Xerox Corporation, Rochester, NY, in 1996. He was a Visiting Researcher in the Laboratory of Intelligent Systems, Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 1998 and in the Center for Biological and Computational Learning, Massachusetts Institute of Technology, Cambridge, in 1999. He is presently an Assistant Professor in the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada. His research interests include analog and digital VLSI circuits, systems and algorithms for energy-efficient signal processing with applications to electrical, chemical and photonic sensory information acquisition, biosensor arrays, brain–silicon interfaces, parallel signal processing, adaptive computing for pattern recognition, and implantable and wearable biomedical electronics.

Dr. Genov received the Canadian Institutes of Health Research (CIHR) Next Generation Award in 2005 and the DALSA Corporation Componentware/CAD Award in 2006. He is an Associate Editor of IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS.

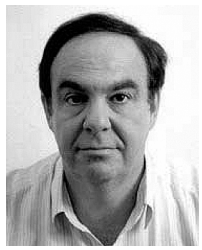
**Berj L. Bardakjian** (M'05) received the Ph.D. degree in electrical engineering (Biomedical Engineering Group) from McMaster University, Hamilton, ON, Canada.

His previous positions included being a Medical Research Council (MRC) Postdoctoral Fellow in the Department of Physiology, then a MRC Scholar in the Institute of Biomaterials and Biomedical Engineering, both at the University of Toronto, Toronto, ON, Canada, and an Investigator in the Playfair Neuroscience Unit at the Toronto Western Hospital. He is currently a Professor of Biomedical and Electrical Engineering at the University of Toronto, Toronto, ON, Canada. His research interests include biological and artificial neural networks, generation and coupling mechanisms of neural bioelectricity, prediction and control of epileptic seizures, modeling of nonlinear physiological systems, biological clocks, and spatiotemporal processing of nonstationary electrical signals from the brain.

Dr. Bardakjian is an Associate Editor for *Annals of Biomedical Engineering*.

**Miron Derchansky** received the M.B.A. degree from the University of Massachusetts, Amherst, and the Ph.D. degree in physiology and neuroscience at the University of Toronto, Toronto, ON, Canada.

Utilizing extracted brain tissues, his primary interests include the electrophysiological mechanisms and spread of seizure activity. To address this issue, he employs single-cell and multisite field recordings, coupled with voltage sensitive dyes. He is currently the co-founder of a startup biotechnology company focused on developing electrophysiological laboratory equipment, adaptive signal processing algorithms, and medical devices for the prediction and control of dynamic brain states.



**Peter L. Carlen** received the M.D. degree from the University of Toronto, Toronto, ON, Canada, in 1967, where he was trained in medicine and neurology.

He is a Clinical Neurologist specializing in epilepsy and neurodegenerative diseases at the Toronto Western Hospital of the University Health Network. He studied cellular electrophysiology for three years at the Neurobiology Department of the Hebrew University of Jerusalem. From 1975, he was a staff Neurologist and Researcher at the Toronto Western Hospital and the Addiction Research Foundation. In 1989, he was appointed Director of the Playfair Neuroscience Unit and Neuroscience Research at the University Health Network for a ten-year term, where he is now a Senior Scientist and Head of the Division of Fundamental Neuroscience. He is also a Professor in the Departments of Medicine (Neurology), Physiology and the Institute of Biomaterials and Biomedical Engineering, University of Toronto, Toronto, ON, Canada. He has over 200 peer-reviewed biomedical publications and six patents. His main research interests are mechanisms of epilepsy and neurodegeneration.