The 128-Channel Fully Differential Digital Integrated Neural Recording and Stimulation Interface

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***Abstract*—We present a fully differential 128-channel integrated neural interface. It consists of an array of 8×16 low-power low-noise signal–recording and generation circuits for electrical neural activity monitoring and stimulation, respectively. The recording channel has two stages of signal amplification and conditioning with and a fully differential 8-b column-parallel successive approximation (SAR) analog-to-digital converter (ADC). The total measured power consumption of each recording channel, including the SAR ADC, is 15.5 μW. The measured input-referred noise is 6.08 μ V_{rms} over a 5-kHz bandwidth, resulting in a noise efficiency factor of 5.6. The stimulation channel performs monophasic or biphasic voltage-mode stimulation, with a maximum stimulation current of 5 mA and a quiescent power dissipation of 51.5 μW. The design is implemented in 0.35-μm complementary metal–oxide semiconductor technology with the channel pitch of 200 μm for a total die size of 3.4 mm $\times$ 2.5 mm and a total power consumption of 9.33 mW. The neural interface was validated in *in vitro* recording of a low-Mg^{2+}/high-K^{+} epileptic seizure model in an intact hippocampus of a mouse.**

***Index Terms*—Brain, extracellular recording, hippocampus, implantable, multichannel neural recording, multichannel neural stimulation, neural amplifier, SAR analog-to-digital converter (ADC).**

I. Introduction

THERE is a great demand for miniature implantable integrated microsystems that treat neurological disorders, such as epilepsy, depression, and Parkinson's disease. Recording brain neural activity facilitates diagnosis. Neural stimulation may prevent the onset of detrimental neural activity such as that resulting in a tremor.

A conceptual implantable neural recording and stimulation microsystem vision is shown in Fig. 1(a). In this microsystem, the recording and stimulation interface circuits require multichannel operation to record from multiple areas of the brain, a small overall form factor to ensure implantation is feasible, and low-power dissipation to avoid thermal damage of the tissue.

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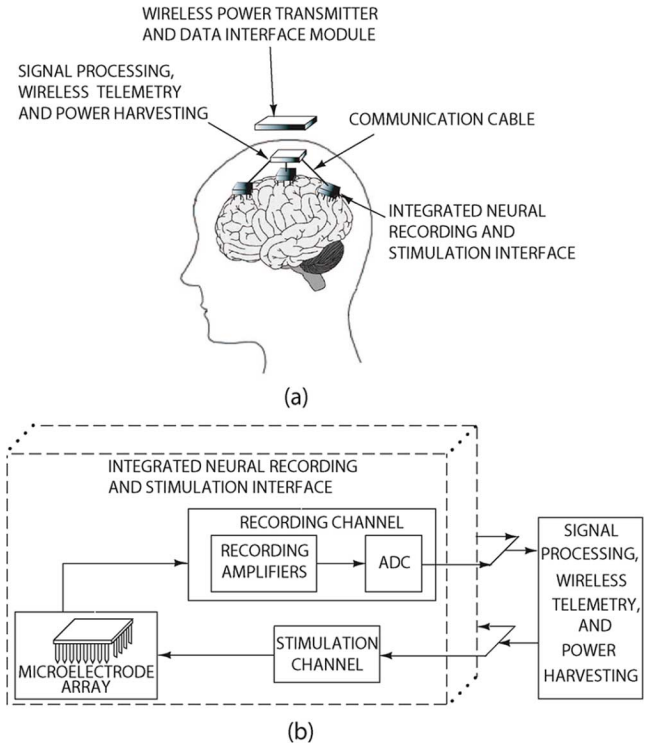

Fig. 1. (a) Implantable system for cortical recording and stimulation. (b) Block diagram of the implanted components of the system.

Fig. 1(b) shows a system-level block diagram of a desired neural recording and stimulation interface. Multichannel neural interfaces are needed for simultaneous neural recording and simultaneous neural stimulation at multiple sites in the brain. The recording channel, which consists of recording amplifiers and ADCs, performs signal acquisition through the microelectrode array. The recorded signals are transmitted wirelessly through the telemetry unit. The wireless telemetry unit can also receive stimulation waveform data for the stimulation channel. Local signal processing can also be implemented for automated neural disorders treatment.

Extracellular action potentials have a wide dynamic range with signal amplitudes approximately between 20 μV to 5 mV [1]–[3]. Most of the neural activity lies within the frequency range of 0.1 Hz to 5 kHz. The dynamic range of the neural recording interface is typically limited by the input signal noise [3]. The total noise at the input of a neural recording interface consists of the background thermal noise of the neural potential field and the thermal noise of the recording electrode. The resulting total input noise is approximately 20 μ V_{rms} [3],

[4]. This corresponds to a dynamic range of approximately 48 dB requiring 8 b of resolution. Other nonidealities that affect the performance of a neural recording interface are common-mode noise and interference from digital circuitry. Fully differential architectures are required since they provide high common-mode rejection ratio (CMRR) and power-supply rejection ratio (PSRR) to suppress common-mode noise and interference from the power-supply and on-chip digital circuits.

Since neural signal amplitudes can be very small, the input-referred noise of the recording interface has to be minimized in order to achieve a large dynamic range. In order to prevent damage at the electrode tissue interface, the maximum temperature increase in the cortex has to be smaller than 1 °C. This corresponds to a maximum power density of 0.8 mW/mm^2 of exposed tissue area [5], [6]. For implantable neural interfaces, low-power dissipation is also desired for wireless power harvesting or prolonged battery life. The small form factor is another important design constraint for neural recording and stimulation interfaces. High-density integrated neural interfaces facilitate implantation and reduce fabrication costs. Noise and gain requirements determine the size of the capacitors and amplifiers of the recording and stimulation circuits. A channel pitch of 200 μm is chosen based on the gain and noise requirements of the channel. This channel pitch also facilitates integration with existing microelectrode arrays, such as the Utah electrode array (UEA) [7]. In order to ensure neural activity is recorded and modulated in a 2-D plane, it is important to organize a large number of channels into an array and then directly bond the microelectrodes to the top of the chip. This minimizes the form factor of the microsystem, simplifies integration, and minimizes routing from the electrodes to the integrated circuit (IC).

In recent years, there has been significant progress in developing low-noise low-power integrated neural interfaces. Generally, single-ended designs [1], [8]–[17] suffer from interference by any digital circuits implemented on the same chip or by other sources of interference in the brain tissue. Fully differential architectures [18]–[23] are advantageous as they suppress common-mode noise and interference.

A number of single-channel fully differential neural recording interface implementations have been reported where the channel area is not a significant constraint [18], [19]. A one-stage recording channel with a programmable cutoff frequency in [18] minimizes signal distortion. A two-stage recording channel in [19] achieves high gain by employing one OTA in the first stage and three OTAs in the second stage.

Multichannel fully differential designs allow for spatial neural recording at multiple sites [20]–[23] but require dense integration. A 16-channel neural recording interface without an ADC is presented in [20]. The design in [21] has 16 channels of bandpass amplifiers with $\Delta\Sigma$-modulated ADCs that occupy an area of 3 mm $\times$ 3 mm and consume 1.8 mW of power. A 100-channel recording interface consisting of chopper amplifiers, an ADC, and a wireless transmitter is described in [22] where up to 50 channels can record simultaneously. Low input-referred noise of 3.2 μW is achieved at the expense of a total power consumption of 8.5 mW. A 128-channel wireless neural recording interface is reported in [23] where signal quantization, spike detection, and sorting, and wireless telemetry are performed on-chip. A low power consumption of 6 mW is obtained within the die area of 8.8 mm $\times$ 7.2 mm.

Neural stimulation is an effective means for the treatment of many neurological disorders. Extracellular neural stimulation is performed in two modes: 1) current mode and 2) voltage mode. In the current-mode stimulation, the stimulator output is a current whose amplitude is directly controlled. Current-mode stimulators are extensively employed. A high-voltage compliance current-mode stimulator is presented in [24] where constant current levels are achieved by the high-output impedance. The design in [25] implements a programmable current-mode stimulator with voltage and current monitoring circuits. Studies show that applying prolonged constant current may cause electrolysis at the electrode-tissue interface which leads to permanent damage of the central nervous system [26]. In order to prevent such permanent damage of the tissue, additional safety features are required as detailed in [27] and [28]. These safety features add more area and complexity to the circuits.

Current-mode stimulation requires significant power [29]. Typically, voltage-mode stimulation delivers higher output current to the tissue for a given supply voltage. The voltage stimulator also has a small area in comparison to a current stimulator of the same output current, making it suitable for a system with a large channel count. However, the tissue impedance is often unknown, making it difficult to control how much charge is delivered to the tissue when using voltage-mode stimulation.

Several reported multichannel fully differential neural interfaces provide neural recording and stimulation [30], [31]. A 64-channel programmable deep brain stimulator with eight-channel neural amplifiers and a logarithmic ADC is presented in [30]. A 6.5 mm $\times$ 6.5 mm 128-channel array in [31] with column-parallel ADCs performs recording and stimulation with a total power consumption of 120 mW.

We present a 128-channel fully differential neural interface array which performs simultaneous recording and simultaneous stimulation on all channels first reported in [32]. It has a fully digital interface including on-chip SAR ADCs and biphasic neural stimulators. Voltage stimulation is chosen as it prolongs the battery life and allows for future integration with a wireless power transmitter as the one described in [33]. The neural recording interface has an input-referred noise of 6.08μ $\mathrm{V_{rms}}$ over a 5-kHz bandwidth, occupies an area of 3.4 mm $\times$ 2.5 mm and has a total power consumption of 2.4 mW and 7 mW for the recording and stimulation modes, respectively. The rest of this paper is organized as follows. Section II describes the system architecture of the neural interface. Section III presents the neural recording channel including the neural amplifiers and the ADC. Section IV describes the stimulation circuit. Section V explains the artifact removal methodology. Section VI demonstrates the experimental validation of the integrated neural recording and stimulation interface in applications.

II. System Architecture

The neural recording and stimulation interface consists of an array of 8 $\times$ 16 channels with column-parallel ADCs. The 128-channel fully differential digital recording and stimulation neural interface was fabricated in a standard 0.35-μm double-

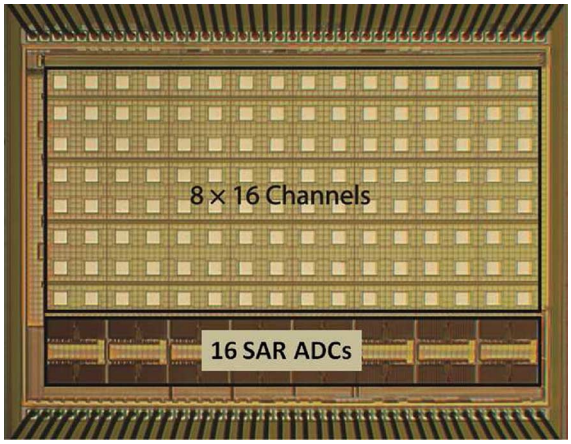

Fig. 2. Micrograph of the neural recording and stimulation interface.

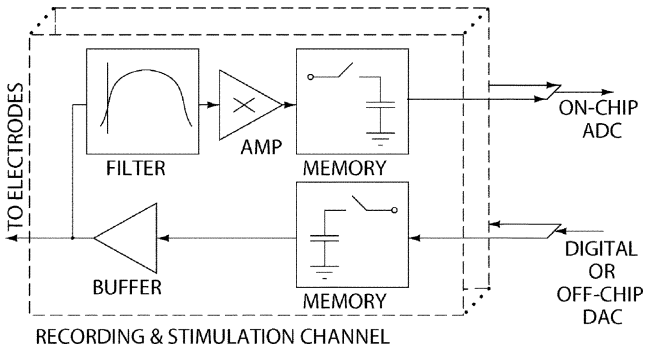

Fig. 3. Architecture of one column of the neural recording and stimulation interface. Each recording amplifier and stimulator is in-channel and the ADC is column parallel.

poly CMOS technology. Fig. 2 shows the micrograph of the die. The die dimensions are 2.5 mm × 3.4 mm. Low power dissipation, low noise, and small channel area are the key design constraints.

Fig. 3 depicts the column architecture of the array. The recording channel has two stages of fully differential low-noise amplifiers that also implement a bandpass filter. Both the low-pass and high-pass frequencies are adjustable. The gain can be digitally tuned from 54 dB to 73 dB with eight programmable gain modes. Simultaneous recording among all channels is achieved by sampling and storing the analog output onto the in-channel memory. The analog outputs of each row are sequentially fed into the column-parallel ADCs for on-chip signal digitization. The column-parallel ADCs are fully differential SAR ADCs. The in-channel stimulation circuit performs voltage-mode monophasic or biphasic stimulation. The in-channel memory enables simultaneous stimulation on all channels. Artifact removal functionality is included to allow neural activity recording shortly after stimulation by improving the slow transient response of the saturated recording amplifier.

III. Neural Recording Channel

A. Channel Architecture

Each recording channel combines two stages of fully differential signal amplification. A sample-and-hold (S/H) circuit [34] is included in each channel in order to ensure simultaneous recording among all array channels. Fig. 4 illustrates the architecture of the recording channel.

Signal amplification is performed in two stages in order to achieve high gain without degrading the signal linearity. Fully differential signaling is utilized to reduce common-mode noise and interference from on-chip digital circuitry.

The first stage is implemented as a high-pass filter (HPF) with dc rejection in order to remove the dc offset that typically appears at the electrode tissue interface. The large input capacitance of the first stage rejects dc offset signals and prevents the amplifier from saturation. The closed-loop gain of the first stage is determined by the ratio $C_{\rm in}/C_f$. The midband gain is designed to be 33 dB by selecting $C_{\rm in} = 4.5$ pF and $C_f = 100$ fF. The capacitor values are optimized based on gain accuracy, noise, and area considerations. The HPF is implemented by utilizing resistors and capacitors in the negative feedback. The HPF cutoff frequency is determined by $1/(2\pi R_f C_f)$. As the low-frequency content of the neural local action field potentials contains important information, the HPF cutoff frequency needs to be in the order of subhertz. In order to achieve these low HPF cutoff frequencies, a large feedback resistor is required.

The large feedback resistance is implemented as PMOS transistors biased in the subthreshold region [1]. The HPF cutoff frequency is tunable from 0.5 Hz to 50 Hz by changing the bias voltage of the PMOS transistors. The PMOS transistors in the feedback path also act as reset switches that periodically bring the amplifier into a unity gain configuration in order to eliminate dc drift caused by junction leakage [31]. The reset switches are also employed for artifact removal as explained in Section V.

The first stage has a tunable low-pass filter (LPF) 3-dB frequency between 500 Hz and 10 kHz which is controlled by the bias current of the OTA. The LPF acts as an antialiasing filter for the on-chip ADC. The first-stage OTA is a fully differential telescopic amplifier as explained in more detail in Section III-B.

The second stage is a variable-gain fully differential amplifier. The closed-loop gain is determined by $C'_{\rm in}/C'_f$, where $C_{\rm in} = 2.5$ pF and C'_f is a programmable bank of four capacitors with the values of 25 fF, 50 fF, 50 fF, and 75 fF. The second stage provides a programmable closed-loop gain of 21 dB to 40 dB with eight different gain modes. Since the second stage is capacitively coupled, its supply voltage is reset periodically in order to compensate for drift at the input nodes of the OTA. The LPF cutoff frequency of the second stage can be adjusted by changing the bias current of its OTA. A second-order antialiasing filter is implemented by setting the LPF cutoff frequency of the second stage equal to that of the first stage. The second-stage amplifier requires a high output signal swing but its noise requirement is relaxed. A folded-cascode topology is employed in the second stage OTA as explained in Section III-B in more detail.

The second-stage amplifier is followed by a S/H circuit in order to ensure simultaneous sampling of signals among all recording channels. The sample-and-hold is a switched capacitor circuit with bottom-plate sampling in order to eliminate input signal-dependent charge injection. Its design is explained in detail in [35].

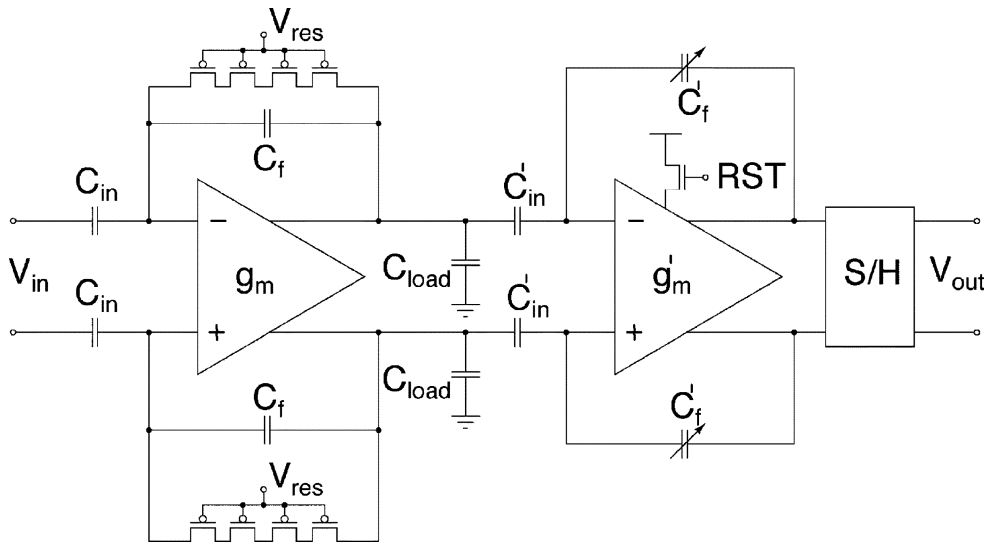

Fig. 4. Recording channel architecture.

B. Neural Amplifier

The design of the first-stage OTA is of particular importance. The first stage determines the overall noise of the recording channel as its noise contribution is significantly higher than that of the following stages. The main design requirements for the first-stage OTA are low noise, low power consumption, and small area. The first stage does not require high-output signal swing as the amplified output signal is in the range of tens of millivolts to a few hundred millivolts. Several fully differential OTA topologies with low power consumption and low noise have been reported. A wide-swing current mirror transconductance amplifier in [20] achieves low noise at the expense of high-power dissipation and large area. The designs in [18] employ a wide-swing current mirror topology optimized for low noise and low power, but occupy a large area. A folded-cascode architecture with low-noise contribution is reported in [31] that has high-power dissipation and large integration area. A two-stage amplifier is reported in [21] with low-noise and low-power operation. The common topologies employed in previous designs provide a high output dynamic range which is not required for the first-stage amplifier. In this design, the telescopic topology is chosen. Since high dynamic range is not required at the output of the first stage, the telescopic topology is suitable and reduces the power consumption due to a few dc current branches. The fully differential telescopic OTA of the first stage and its common-mode feedback (CMFB) circuit are illustrated in Fig. 5. Table I lists the transistor sizing for the telescopic amplifier.

The overall noise of the telescopic amplifier is composed of a thermal noise component and a flicker noise component as shown in (1). These noise sources can be modeled as voltages sources in series with the input. The input-referred noise voltage per unit bandwidth is given by

$$\overline{V_n^2} = 2\left[\frac{4kT}{g_{m1}}\left(\frac{2}{3}\right)\left(1+\frac{g_{m7}}{g_{m1}}\right)\right] + 2\left[\frac{K_P}{C_{\rm ox}W_1L_1} + \frac{K_N}{C_{\rm ox}W_7L_7}\left(\frac{g_{m7}}{g_{m1}}\right)^2\right]\frac{1}{f}, \quad (1)$$

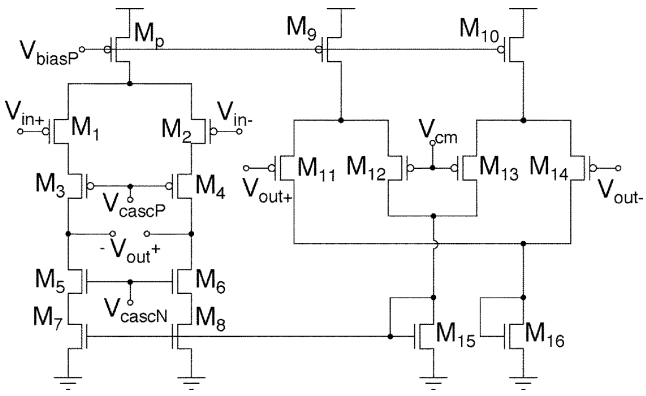

Fig. 5. Fully differential telescopic OTA.

TABLE I
TELESCOPIC OTA TRANSISTOR SIZING

Transistor	W/L (μm)
$M_{1,2}$	$4 \times 5/7.5$
$M_{3,4}$	$2 \times 4.25/12$
$M_{5,6}$	$2/10$
$M_{7,8}$	$1/20$
M_p	$2/6$
$M_{9,10}$	$2/7$
$M_{11,12,13,14}$	$1/20$
$M_{15,16}$	$1/20$

where k is Boltzmann's constant, T is the temperature in degrees Kelvin, g_m is the transconductance, $C_{\rm ox}$ is the metal–oxide semiconductor (MOS) oxide capacitance, and K_N and K_P are the 1/f noise coefficients of NMOS and PMOS transistors, respectively. The first line of (1) represents the thermal noise, and the second line refers to the flicker $1/f$ noise of the telescopic OTA. The transistors that contribute to the thermal noise are $M_{1,2,7,8}$. The thermal noise component can be significantly reduced by increasing $g_{m1,2}$ so that $g_{m1,2} \gg g_{m7,8}$. At a fixed bias current, the thermal noise is minimized by selecting

TABLE II
SIMULATED TELESCOPIC OTA ELECTRICAL CHARACTERISTICS

DC Gain	101dB
Unity Gain Frequency (12pF)	300kHz
Loop Gain Unity Gain Frequency	5kHz
Output Voltage Swing	$0.55V_{pp}$
Total Bias Current (with CMFB)	$2.8\mu A$
Input-Referred Thermal Noise	$59.9nV_{rms}/\sqrt{Hz}$
Supply Voltage	3.0V

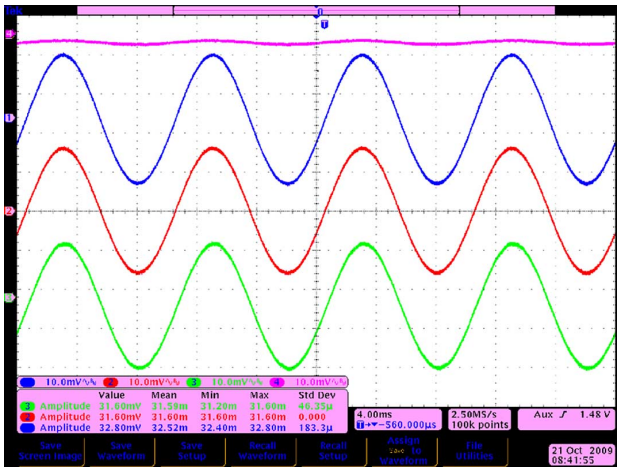

Fig. 6. Output of three different neural channels, with a 0.8-mV input (top waveform).

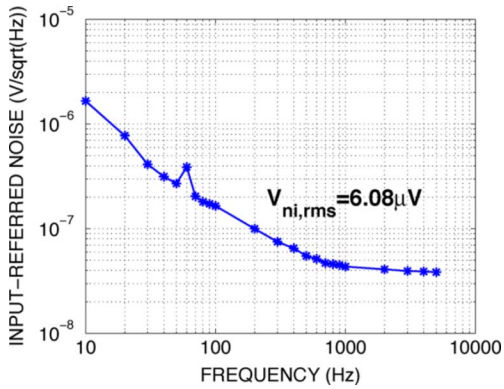

Fig. 7. Measured input-referred voltage noise density for the first stage of the amplifier between 10 Hz and 5 kHz.

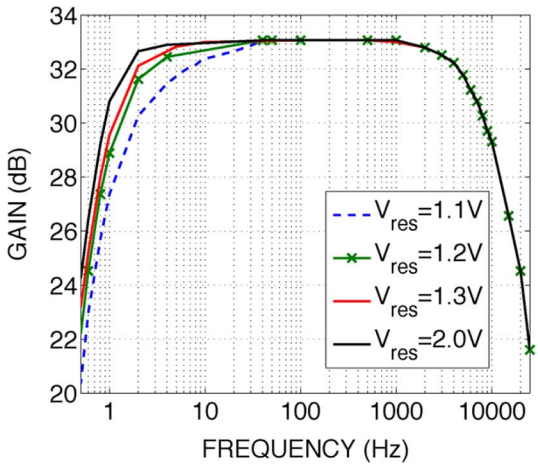

Fig. 8. Measured amplitude frequency response of the first-stage amplifier with programmable HPF cutoff frequency adjusted by changing the bias voltage of feedback resistors $\mathrm{V_{res}}$.

$W/L|_{1,2} \gg W/L|_{7,8}$ so that $M_{1,2}$ are biased in weak inversion and $M_{7,8}$ are in strong inversion. Increasing the bias current leads to a further increase in $g_{m1,2}$ and a subsequent decrease in the thermal noise. Transistors $M_{1,2}$ are dominant in their $1/f$ noise contribution. $M_{1,2}$ are chosen as large PMOS transistors in order to reduce the $1/f$ noise component.

The CMFB circuit [36] draws the same bias current as the first stage of the OTA. In order to increase the linear range of operation for the CMFB circuit, the input transistors M_{11-14} should have a high gate-to-source effective voltage V_{eff}. At a fixed bias current, high V_{eff} is achieved by selecting $W/L|_{11-14}$ at the minimum value of 1 μm/20 μm. Thus, sufficient output dynamic range is achieved for the first-stage OTA.

Table II summarizes the simulated results for the telescopic OTA. In order to achieve a gain accuracy of better than 0.1%, an open-loop gain of higher than 94 dB is required. The open loop of the telescopic amplifier is 101 dB which provides this gain accuracy. The experimentally measured input-referred noise density of the first stage of the amplifier in the frequency range of 10 Hz to 5 kHz is illustrated in Fig. 7. Integrating the noise over this bandwidth yields an rms noise voltage of 6.08 μV. The measured CMRR of the recording amplifier is 60 dB. Fig. 8 shows the experimentally measured frequency response of the first-stage amplifier. The HPF cutoff frequency is adjusted by changing the bias voltage V_{res} of the feedback resistors. For multichannel operation, a 0.7-mV sinusoid at 100 Hz was input into three different neural amplifiers on the chip. The gain from the first stage of the three channels is 33.0 dB, 33.0 dB, and 33.4 dB as shown in Fig. 6.

Table III shows the performance of the fully differential first-stage neural amplifier of this design in comparison to designs reported in [20], [21], [30], [31], and [37]. The best noise efficiency factor (NEF) was reported in [37] and [17] with NEF's of 4.1 and 4.6, respectively. However, the large area for these designs makes it difficult to integrate a large number of channels. They also have low bandwidth not suitable for spike recordings.

The second stage has relaxed noise requirements since its noise contribution is divided by the gain of the first stage. In the second stage of signal amplification, a higher dynamic range is required. A folded cascode topology is selected for the second-stage OTA amplifier. Fig. 9 depicts the folded cascode OTA with its CMFB circuit. Table IV lists the transistor sizing for the folded cascode amplifier. Since the second-stage noise contribution is small, its power consumption is reduced. The bias current of the folded cascode OTA is set to be half that of the telescopic OTA of the first stage. The LPF cutoff frequency of the folded cascode amplifiers is set by the bias current to a nominal value of 5 kHz, the same as that of the first stage in order to provide an effective second-order filter. The load capacitance

TABLE III
COMPARISON OF NEURAL AMPLIFIER CHARACTERISTICS

	OTA Topology	Tech. [μm]	Fully Diff.	Noise [μV]	Bandwidth [Hz]	Power [μW]	Voltage [V]	NEF	Gain [dB]	Area [mm^2]
[21]	Two-stage	0.5	Yes	7.8	0.1 - 10k	114.8	3	18.7	40	0.107
[30]	Two-stage	0.18	No	5.29	16 - 5.3k	9	1.8	-	40	-
[31]	Folded cascode	0.6	No	5.9	10 - 100k	160	5	8.1	20	0.062
[37]	Chopper-Stablized	0.5	Yes	0.59	0.5-100	6.9	3	4.1	48	0.45
[17]	Chopper-Stablized	0.8	No	0.95	0.05-100	1.8	1.8-3.3	4.6	41	0.7
This work	Telescopic	0.35	Yes	6.08	10 - 5k	8.4	3	5.55	33	0.02

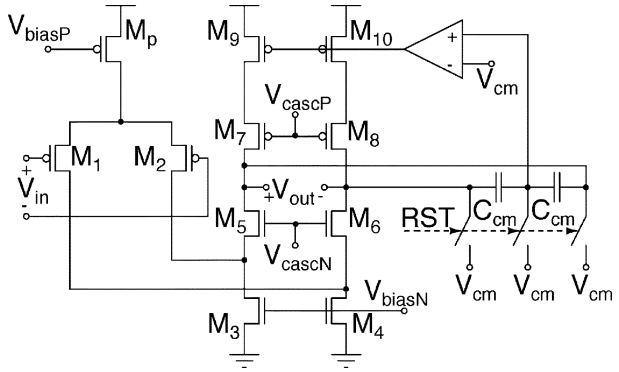

Fig. 9. Fully differential folded cascode OTA.

TABLE IV
FOLDED CASCODE OTA TRANSISTOR SIZING

Transistor	W/L (μm)
$M_{1,2}$	1/12
$M_{3,4}$	1/10
$M_{5,6}$	1/10
$M_{7,8,9,10}$	1/5
M_p	1/6

seen by the second-stage folded cascode amplifier is the parallel combination of feedback capacitors C_f' and S/H input capacitance in series with the input capacitance of the folded cascode amplifier. In order to achieve an LPF cutoff frequency of 5 kHz without adding extra load capacitance, the current in the output stage is made larger than that of the input stage by choosing $W/L|_{7-10} > W/L|_{1,2}$. Transistors M_{5-6} are sized with a large W/L ratio equal to that of transistors M_{3-4}. This results in a small drain-to-source voltage ($V_{\rm DS}$) drop across transistors M_{3-4} and increases the output voltage swing.

The CMFB circuit utilized in the first-stage amplifier [36] limits the output signal swing. Since the second-stage OTA requires a high output dynamic range, a capacitive divider is utilized as its CMFB circuit. The capacitive divider functions similar to the resistive dividers commonly used in CMFB circuits

TABLE V
SIMULATED FOLDED CASCODE OTA ELECTRICAL CHARACTERISTICS

DC Gain	82dB
Unity Gain Frequency (200fF)	568kHz
Output Voltage Swing	$2.25V_{pp}$
Total Bias Current (with CMFB)	$1.4\mu A$
Supply Voltage	3.0V

where the average of the output signals is taken and subtracted from a reference common-mode voltage. The capacitive divider is reset to the reference common-mode voltage value once every thousand cycles [38] in order to prevent floating nodes at the capacitor terminals.

Table V summarizes the simulated results for the folded cascode OTA. The second-stage amplifier has a variable capacitive load. In the worst case, an open-loop gain of 80 dB is required to achieve a closed-loop gain accuracy of better than 1%.

C. Analog-to-Digital Converter

Implantable neural interfaces require ultra-low power signal digitization to ensure long battery life. In order to avoid antialiasing, the sampling rate of the ADC has to be higher than the Nyquist rate by a margin accounting for the antialiasing filter pass-band rolloff. A sampling rate of 14 kHz per channel for a 5-kHz bandwidth is achieved by designing column-parallel ADCs sampling at 111 kSamples/s.

A number of ADC architectures, such as oversampling modulators, algorithmic converters, and SAR ADCs meet our requirements in terms of the sampling rate, power consumption, and resolution. Energy-efficient converters using the named architectures are reported in [38]–[41]. Oversampling modulators are best suited for low-bandwidth applications. In order to achieve a sampling rate of more than 100 kSamples/s, algorithmic or SAR ADCs are required. The SAR architecture is selected in this design since it typically has lower power consumption, and it only consists of one comparator, a capacitor array, and logic circuits, without requiring an explicit S/H circuit.

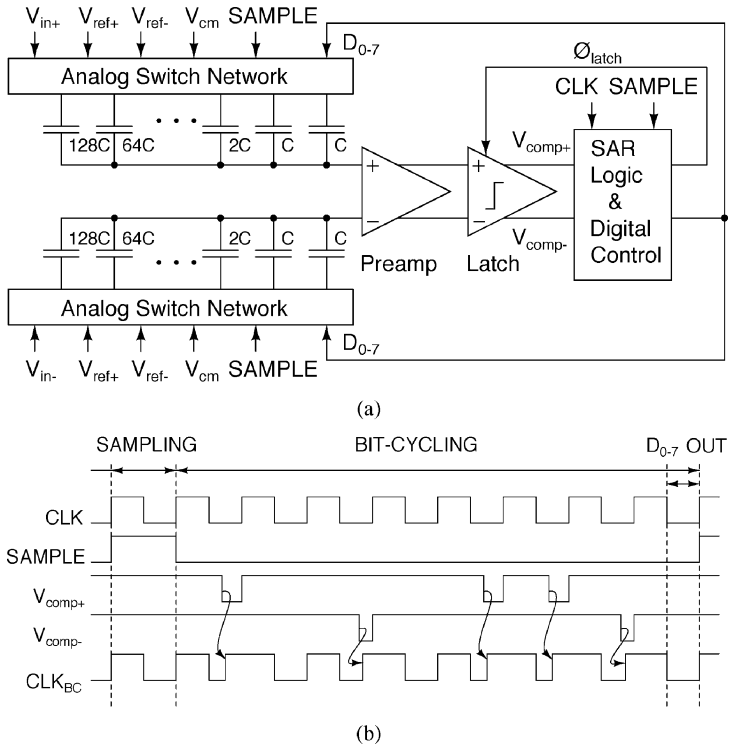

Fig. 10. (a) Self-timing successive approximation ADC architecture. (b) Sample timing diagram of the SAR ADC.

The column-parallel ADC is a fully differential successive approximation (SAR) ADC. SAR ADCs offer low-power dissipation for medium resolutions and medium sampling rates, 8 b, and 100 kSamples/s, respectively, in this design. Column-parallel ADCs are advantageous over a single ADC as they enable design scalability.

Fig. 10(a) shows the architecture of the ADC and Fig. 10(b) illustrates the timing of the ADC. The differential input signal is sampled when SAMPLE goes high and is applied to the differential capacitor array through the analog switch network. The output of the capacitor array is fed to the comparator. The comparator consists of the preamplifier and the latch. Once the comparator makes a decision, its output is sent to the SAR register where the digital output bits are evaluated after eight clock cycles and fed back to the capacitor array. In order to further reduce the power dissipation, a self-timing methodology is incorporated to start bit-cycling immediately after the comparator makes a decision [42], [43]. As illustrated in Fig. 10(b), the asynchronous clock $\mathrm{CLK_{BC}}$ goes high and bit cycling starts as soon as the comparator output voltages are resolved. Clocks are generated off-chip using a field-programmable gate array (FPGA).

Fig. 11(a) and (b) illustrates the circuit diagrams of the preamplifier and the regenerative latch, respectively. The preamplifier stage is employed in order to reduce the offset and prevent kickback from the regenerative feedback to the sensitive input signal [36]. The bias current is set to 1 μA. The latch is a sense-amplifier flip flop similar to the conventional design in [44]. In [44], the drain terminals of transistors M_1 and M_2 are shorted together during the reset phase. However, in this design, these drain terminals are directly connected to V_{dd} during the reset phase when Φ_{latch} is low. Two inverters are placed at the latch output in order to restore the outputs to logic high and low values. Transistor sizing of the preamplifier and the latch are

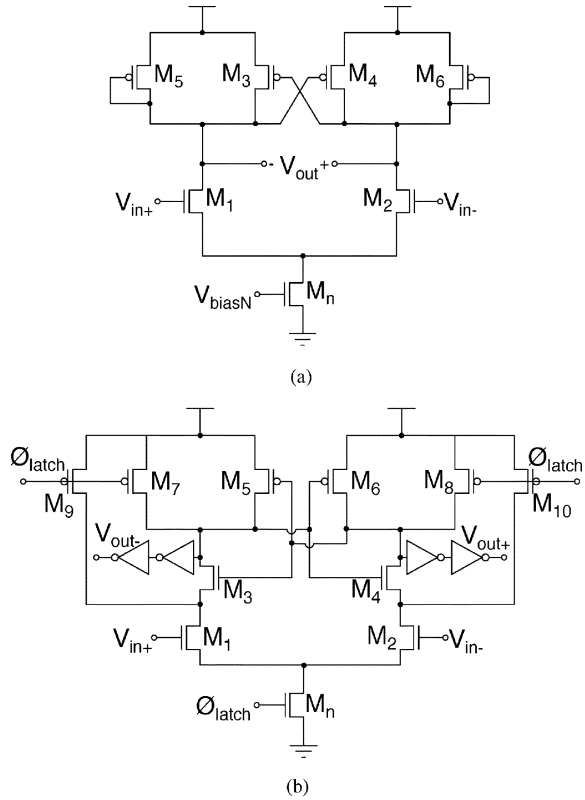

Fig. 11. (a) Preamplifier and (b) comparator circuits.

TABLE VI
COMPARATOR TRANSISTOR SIZING

Transistor	Preampli£er W/L (μm)	Latch W/L (μm)
$M_{1,2}$	$2/3$	$2/1$
$M_{3,4}$	$2/1$	$1/0.35$
$M_{5,6}$	$4/1$	$2/0.35$
$M_{7,8,9,10}$	-	$0.8/0.35$
M_n	$1/2$	$1/1$

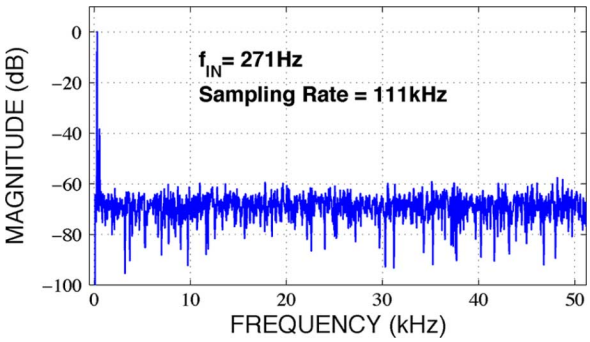

Fig. 12. Measured output spectrum of ADC for a 271-Hz sinusoid input sampled at 111 kilosamples/s.

listed in Table VI. The layout of the preamplifier and latch input pairs M_1 and M_2 utilize the common-centroid technique to reduce mismatch errors, thus minimizing the comparator offset voltage.

The ADC was experimentally characterized. A 271-Hz full-range sinusoid was applied to the ADC. The experimentally measured output spectrum is depicted in Fig. 12. The second harmonic reduces the effective number of bits (ENOB) of the ADC to 6 b. The differential nature of the ADC suppresses the second harmonic. Removal of the second harmonic yields an ENOB greater than 7 b. Static dc testing revealed that there were no missing codes for the ADC.

The functionality of the full 8×16 neural recording interface was experimentally validated when recording an entire signal frame with all channels connected to the same input. A neural spike waveform was emulated with a signal generator to model extracellular neural activity. An emulated neural spike with an amplitude of 1 mV $_{pp}$ was the input signal to all channels. The input signal was amplified and digitized using the on-chip amplifiers and ADCs. The digitized output corresponds to a differential output of 440 mV and is depicted in Fig. 13. In this figure, the digitized output shows an amplitude of 22% of the ADC full signal range.

IV. NEURAL STIMULATION CIRCUIT

As explained in Section II, each channel performs neural recording and stimulation. The channel architecture of the in-channel voltage-mode stimulator is illustrated in Fig. 14(a). The voltage-mode stimulator consists of a sample-and-hold circuit, a class AB buffer, and a switch network. The sample-and-hold circuit is included in all 128 channels and allows for simultaneous stimulation on all channels. A 128-sample stimulation frame is sequentially loaded onto the

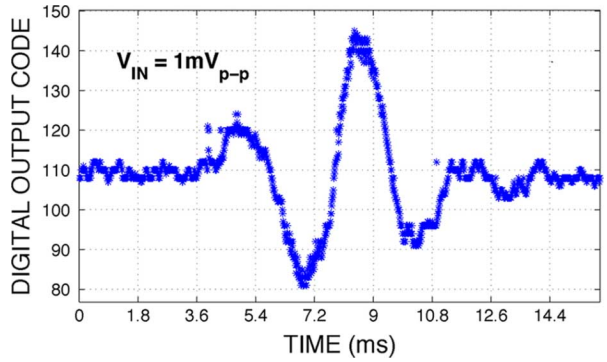

Fig. 13. Measured digitized output of the full recording channel including the amplifier and ADC with an emulated neural spike input of 1 m V_{PP}.

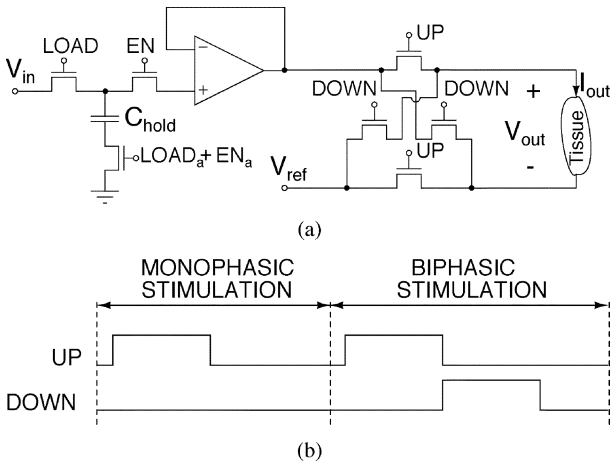

Fig. 14. (a) In-channel voltage-mode biphasic stimulator. (b) Stimulator timing diagram.

capacitor array when LOAD is high and is activated on all channels at the arrival of an EN pulse. Charge injection is minimized by opening the capacitor bottom plate slightly in advance of the other two switches.

Voltage stimulation can be configured as a monophasic or biphasic sequence. Monophasic stimulation leads to charge accumulation at the electrode-tissue site and can damage the tissue. Biphasic stimulation, where each pulse is followed by a pulse of reversed polarity, ensures charge balancing and prevents damage at the electrode-tissue interface. The cross-coupled switches in Fig. 14(a) implement monophasic and biphasic voltage stimulation [45]. The direction of the stimulator's output voltage is set by signals UP and DOWN. Fig. 14(b) shows the timing diagram of the stimulator and its output voltage. Both monophasic and biphasic sequences are illustrated. Fig. 15 illustrates the experimentally measured output voltage of the biphasic voltage stimulator.

The voltage-mode stimulator should be capable of providing large currents since it has a variable load. The load of the stimulation circuit changes based on the electrode-tissue site characteristics and impedance. A buffer with low-output impedance can drive a variable load. The buffer is implemented as a class AB output stage where the negative input is tied to the output voltage [31]. The design is described in detail in [46]. Fig. 16 shows the circuit diagram of the class AB output stage with

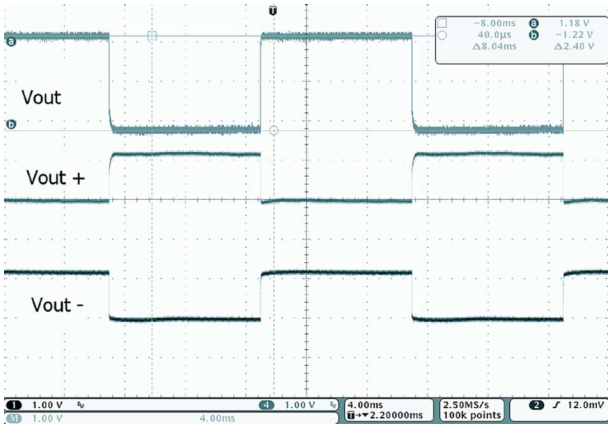

Fig. 15. Experimentally measured biphasic voltage stimulator output.

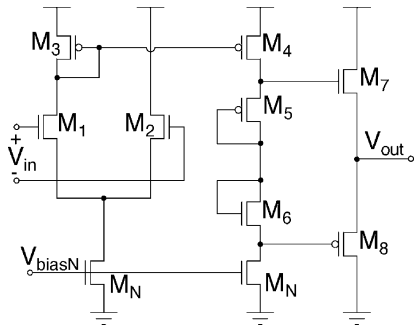

Fig. 16. Class AB buffer output stage.

TABLE VII
STIMULATOR SIMULATED ELECTRICAL CHARACTERISTICS

Bias Current	$2.4\mu A$
Quiescent Current	$10.7\mu A$
Maximum Output Current	5mA
Slew Rate (20nF)	$30V/ms$
Total Power Consumption	$51.15\mu W$
Supply Voltage	3.3V

transistor sizing listed in Table VIII. Table VII summarizes the simulated electrical characteristics of the class AB output stage. The quiescent current and total power consumption values are found when no input signal is applied to the circuit. The stimulator can deliver a maximum power of 16.5 mW at the supply voltage of 3.3 V. In order to reduce the overall power consumption of the neural interface, the stimulation circuit is turned on only when a channel is selected for stimulation. The stimulation circuit is powered down during recording or when a channel is not selected for stimulation. The stimulator's input can be a digital or analog voltage. An off-chip DAC is used to generate analog voltage at the input of the stimulator. Analog input voltage stimulation allows for stimulation with arbitrary-shaped analog waveforms that are of particular importance in neurological research applications.

Table IX shows the performance of the voltage stimulator of this design in comparison to current- and voltage-mode neural

TABLE VIII
CLASS AB BUFFER TRANSISTOR SIZING

Transistor	W/L (μm)
$M_{1,2}$	$4 \times 2/0.35$
M_3	$1/2$
M_4	$2/2$
M_5	$1/0.35$
M_6	$2.5/0.35$
M_7	$7.5/0.35$
M_8	$3/0.35$
M_N	$1/3$

stimulators reported in [30], [31], and [47]–[49]. The voltage stimulators are capable of providing higher maximum current to the load for a given supply voltage. At a supply voltage of 3.3 V with a nominal load of 10 kΩ, current stimulators can theoretically provide a maximum current of 330 μA. Voltage-mode stimulation is chosen in order to provide higher output current at the load. The voltage stimulator also has a small area in comparison to the listed current stimulators.

V. ARTIFACT REMOVAL

One of the major obstacles in bidirectional neural recording and stimulation interfaces is the presence of stimulation artifact. Stimulation artifact is the transient signal distortion that is generated near the stimulation site after the stimulation. The stimulation artifact has a duration of tens to hundreds of milliseconds [50]. The artifact may be large enough to saturate the recording channel amplifiers for an extended period of time. In order to record immediately after stimulation, the stimulation artifact has to be minimized. Several designs have addressed the stimulation artifact removal. Among the common approaches are postprocessing of the recorded data and spectral cancelation of the artifact [51] as well as artifact subtraction by averaging [52]. Postprocessing of the recorded data removes the distortion caused by the artifact. However, the recording amplifiers would still saturate within the duration of the artifact. Any neural activity that takes place during this time is not recorded. Real-time processing of the recorded data would be computationally expensive and the recording amplifiers would also be saturated and have to be reset regardless. Another approach is to use an additional amplifier to provide a low-impedance path immediately after the stimulation in order to discharge the electrode from the trapped charge at the electrode-tissue interface [53].

In this design, the artifact removal is achieved by resetting the recording channel immediately after stimulation takes place. Artifact removal is performed by simultaneous reset of the feedback PMOS transistors of the first stage. The duration of the reset signal depends on the amplitude and frequency of the stimulation pulse. A longer reset pulse has to be applied for higher values of stimulation voltage amplitude and slower stimulation frequencies. The reset pulse is applied to the recording channel in order to prevent the long-lasting transient response of the saturated amplifiers. This is shown in Fig. 17(a) where the reset signal is held low during and for 50 ms after the stimulation

TABLE IX
COMPARATIVE ANALYSIS OF MULTICHANNEL CURRENT AND VOLTAGE-MODE NEURAL STIMULATORS

	Technology [μm]	Channels	Channel Area [mm^2]	Mode	Supply Voltage [V]	Resolution	Maximum Current [mA]
[47]	1	4	0.38	Current	6	4-bit	1.0
[48]	1.5	8	0.6	Current	± 6	6-bit	0.6
[30]	0.18	64	-	Current	1.8	7-bit	0.135
[49]	1.5	32	0.1	Current	5	5-bit	0.25
[31]	0.6	128	-	Voltage	5	8-bit	10
This work	0.35	128	0.02	Voltage	3.3	Analog S/H	5

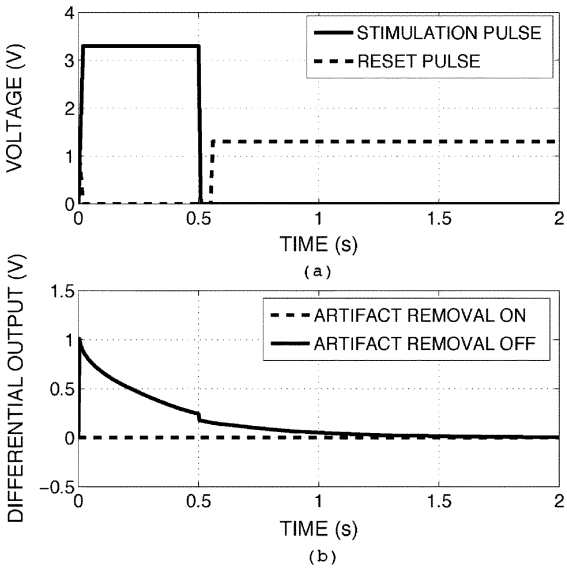

Fig. 17. (a) Stimulation pulse applied to the input of the recording amplifier with a corresponding reset signal to minimize artifacts. (b) Output of the recording amplifier with and without a reset signal applied to the feedback transistor.

TABLE X
RECORDING CHANNEL EXPERIMENTAL CHARACTERISTICS

Programmable Gain	54-73 dB
Low Frequency Cut-off	0.5-50Hz
High Frequency Cut-off	500Hz-10k
Input-Referred Noise	6.08μV, 10Hz-5kHz
Power Dissipation per Channel	12.75μW
NEF of 1st Stage	5.6

pulse. Fig. 17(b) plots the differential output voltage of the amplifier after a 500-ms, 1.5-V stimulation voltage is applied to the input terminals. It takes approximately 1.5 s for the amplifier to settle after the stimulation pulse is applied without artifact removal and less than 0.1 ms when the reset pulse is applied to the amplifier, as shown in Fig. 17(b).

VI. EXPERIMENTAL VALIDATION IN APPLICATIONS

The experimental results for the recording channel are summarized in Table X. The experimental results for the whole chip are shown in Table XI. A custom printed-circuit board (PCB) with an onboard Xilinx Virtex FPGA, off-the-shelf power regulators and digital-to–analog converters (DACs) were used to supply power to the chip and set the proper voltage and current biases. The FPGA synchronizes with a PC PCI card.

TABLE XI
SYSTEM-LEVEL EXPERIMENTAL RESULTS

CMOS Technology	0.35μm
Supply Voltage:	
Recording Array	3.0V
Stimulation Array	3.3V
Die Dimensions	3.4mm$\times$2.5mm
Area per Channel	200$\mu m \times 200\mu m$
Number of Recording Channels	128
Number of Stimulation Channels	128
ADC Input Range	2V$_{pp}$
Sampling Rate of ADC	111kS/s
ENOB of ADC	6.2 bits
Power Dissipation:	
Recording Array	1.63mW
Stimulation Array (Quiescent)	6.59mW
Read-out Circuits	0.44mW
ADC Bank	0.36mW
Total (Recording Mode)	2.43mW
Total (Stimulation Mode)	7.03mW

The neural interface is validated in *in vitro* recording of a low-Mg^{2+}/high-K^{+} epileptic seizure model in an intact hippocampus of a mouse. Hippocampus is obtained from C57/BL mice-aged P10-14. Animals are anesthetized with halothane and decapitated in accordance with the Canadian Animal Care Guidelines. The hippocampus is kept inside a circulating-heated artificial cerebrospinal fluid (ACSF). The off-chip electrodes are ultra-fine tungsten electrodes with 400-μm-length tips that allow access to the cellular layer of the

TABLE XII
COMPARATIVE ANALYSIS OF LOW-POWER NEURAL INTERFACES

			Recording					ADC			Stimulation	
	Tech. $[\mu m]$	Area $[mm^2]$	Channel Count	Power/Ch. $[\mu W]$	NEF	Gain [dB]	Fully Diff.	Topology	Power/Ch. $[\mu W]$	ENOB [bits]	Channel Count	Output Current [mA]
[20]	0.6	12	16	-	-	46	Yes	N/A	N/A	N/A	N/A	N/A
[21]	0.5	9	16	40.26	18.7	40	Yes	$\Delta\Sigma$	76	9.0	N/A	N/A
[30]	0.18	2.7	8	9	-	40	No	Log Pipeline	12.25	7.0	64	0.135
[31]	0.6	42	128	160	8.1	70	Yes	SAR	-	8.0	128	10
This Work	0.35	8.5	128	12.75	5.55	73	Yes	SAR	2.77	6.0	128	5

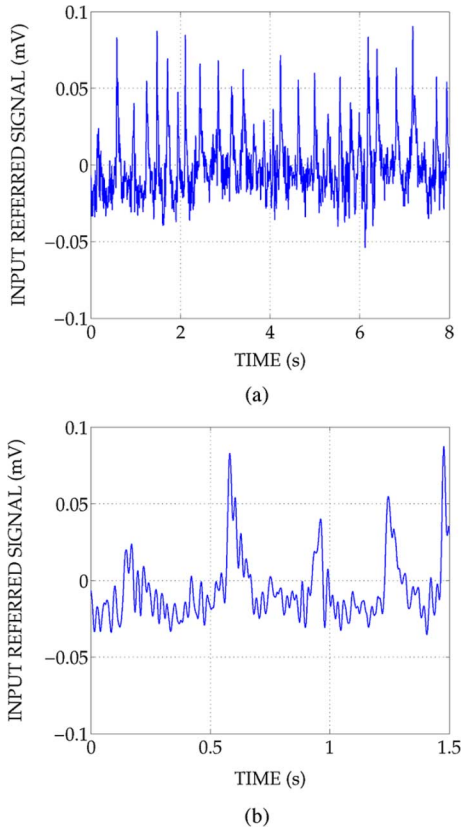

Fig. 18. Experimentally measured epileptic seizure events that were chemically induced in an intact hippocampus of a mouse by applying low-Mg^{2+}/high-K^{+}.

CA3 hippocampal region where seizure activity is recorded. The epileptic seizure-like events are chemically induced in the hippocampus by applying low-Mg^{2+}/high-K^{+} to the circulating ACSF. Neural activity is experimentally recorded and digitized by the on-chip neural recording interface through off-chip recording electrodes. Fig. 18 depicts the epileptic seizure-like events recorded and digitized by the chip.

VII. SUMMARY

Table XII compares the presented bidirectional neural recording and stimulation interface to the reported designs in [20], [21], [30], and [31]. The neural interfaces in [30] and [31] implement neural recording and stimulation. This design is comparable to [30] in terms of recording channel power consumption but there are major improvements to the recording channel gain, ADC power consumption, stimulator maximum output current, and the number of recording and stimulation channels. This design also has the best reported NEF. The improvement in the recording channel gain is a result of two stages of signal amplification. The die area in [30] is smaller due to the lower channel count, and newer technology and the area per recording/stimulation channel are comparable to [30].

VIII. CONCLUSION

We have presented a 128-channel fully differential integrated neural interface for neural recording and stimulation. In the recording mode, the fully differential channels simultaneously amplify neural signals and convert them to the digital domain. In the stimulation mode, the buffered stimulation signal is configured to perform simultaneous voltage-mode monophasic or biphasic stimulation on some or all electrodes. The total measured power dissipation of the recording and the stimulation modes is 2.4 mW and 7 mW, respectively. The NEF of the recording amplifier is 5.6.

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