16-Channel CMOS Impedance Spectroscopy DNA Analyzer With Dual-Slope Multiplying ADCs

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Abstract—We present a 16-channel, mixed-signal CMOS DNA analyzer that utilizes frequency response analysis (FRA) to extract the real and imaginary impedance components of the biosensor. Two computationally intensive operations, the multiplication and integration required by the FRA algorithm, are performed by an in-channel dual-slope multiplying ADC in the mixed-signal domain resulting in minimal area and power consumption. Multiplication of the input current by a digital coefficient is implemented by modulating the counter-controlled duration of the charging phase of the ADC. Integration is implemented by accumulating output digital bits in the ADC counter over multiple input samples. The 1.05 mm $\times$ 1.6 mm prototype fabricated in a 0.13 μm standard CMOS technology has been validated in prostate cancer DNA detection. Each channel occupies an area of only 0.06 mm^2 and consumes 42 μW of power from a 1.2 V supply.

Index Terms—Biosensor, DNA, electrochemical sensor, frequency response analysis, impedance spectroscopy, multiplying ADC.

I. INTRODUCTION

A NUMBER of integrated circuits for DNA detection on a disposable CMOS substrate platform have been introduced in recent years [1]–[7]. The on-chip electrochemical amperometric sensing DNA detection method shows promise over optical methods due to the real-time nature of DNA analysis [8]. Fig. 1 depicts a basic electrochemical cell employed in amperometric sensing. It consists of a working electrode (WE) and a reference electrode (RE). A transducer holds the working electrode at a known potential V_{WE} while recording the redox current generated as a result of the voltage difference between the two electrodes. The reference electrode potential V_{RE} is set to either a constant voltage for constant-potential amperometry, a bidirectional ramp voltage for cyclic voltammetry, or a small-amplitude sinusoid for impedance spectroscopy.

In biochemical sensors, biologically active compounds such as artificial antibodies, enzymes or receptors are integrated onto the working electrode. The integration process is performed by immobilization and stabilization of biological molecules
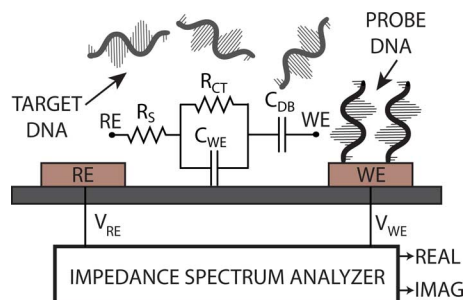
Fig. 1. Conceptual view of a biosensor impedance spectroscopy system.

on the electrode surface. In DNA sensing applications, the surface of the working electrode is functionalized with a probe DNA. Binding of the probe DNA with the target DNA results in a variation of the working electrode surface properties such as the impedance or the surface charge. The variation of the surface properties results in a change in the waveform features of the redox current, thus indicating changes in the kinetics and thermodynamics of the chemical reactions at the sensory interface [9]–[11]. In most applications, the recorded redox current is in the range of pA to nA and the biosensor frequency response covers a range of 1 Hz to 10 kHz [13]–[17].

Impedance spectroscopy is a popular method of quantitative and qualitative monitoring of chemical reactions in many biosensors. A wide range of biosensors have been developed which rely on impedance spectroscopy, including sensors for detection of enzymes, antibodies and DNA [19], [20]. Fig. 1 also shows the basic principle of electrochemical impedance spectroscopy in DNA sensing applications. Binding of the probe DNA with the target DNA changes the impedance between the reference and the working electrodes. To detect this change, an impedance spectrum analyzer extracts the real and imaginary components of the biosensor impedance. A generic $R-C$ biosensor impedance model is depicted in Fig. 1. In this model R_S represents the electrolyte resistance between the working and reference electrode, C_{WE} represents the diffusion layer capacitance, C_{DB} models the interfacial double-layer capacitance at the WE-electrolyte interface and R_{CT} models the charge transfer resistance at the WE-electrolyte interface [21].

Several impedance spectroscopy integrated circuits have been reported [21]–[23]. The design in [22] is a single-channel impedance extractor based on a lock-in amplifier that extracts the sensor impedance from 1 Hz to 10 kHz. The implementation in [21] is a 100-channel impedance-to-digital converter based on a delta-sigma modulator capable of extracting sensor impedance from 1 mHz to 10 kHz at the expense of a long

conversion cycle. A direct conversion receiver without an on-chip ADC [23] extracts the electrode impedance from 10 Hz to 50 MHz at the cost of consuming 104 mW of power.

This paper presents a scalable, multi-channel, compact and low-power CMOS impedance spectroscopy DNA analyzer. Frequency response analysis (FRA) algorithm is utilized to extract the real and imaginary components of the biosensor impedance [24]. The proposed microsystem consists of a programable on-chip waveform generator and 16 impedance extraction channels. Each channel includes a current-mode input dual-slope multiplying ADC. It efficiently performs multiplication and integration, two computationally inten-sive operations required to implement the FRA algorithm. Multiplication of the input current by a digital coefficient is implemented by modulating the counter-controlled duration of the charging phase of the ADC by that coefficient. Integration is implemented by accumulating the output digital bits in the ADC counter. The dual-slope multiplying ADC utilizes mostly the same circuits as a conventional dual-slope ADC, and the multiplication and integration are achieved by modifying the ADC algorithm. The rest of the paper is organized as follows. Section II presents the principle of DNA detection on a CMOS die. Section III presents the impedance spectroscopy VLSI architecture. Section IV details the circuit implementation of the VLSI architecture. Section V demonstrates the electrical experimental results obtained from a 0.13 μm CMOS proto-type. In Section VI, results of on-chip impedance spectroscopy of DNA in prostate cancer screening are presented.

II. DNA DETECTION PRINCIPLE

The principle of the label-free DNA detection method is shown in Fig. 2. It employs potassium ferrocyanide $K_4[Fe(CN_6)]$ reporter. Potassium ferrocyanide is a nega-tively charged redox complex with well-defined electrochem-ical signature exhibiting oxidation and reduction currents at $V_{WE} - V_{RE}$ of -450 mV and -200 mV respectively [25]. The maximum electron transfer between the electrode and potassium ferrocyanide is achieved in the absence of DNA target and probe as illustrated in Fig. 2(a). The oxidization current I_{OX} drops when the Au electrode surface is hybridized with negatively charged probe DNA, as illustrated in Fig. 2(b). When the complementary DNA binds with the probe DNA, the surface negative charge further increases and the oxidization current is further reduced, as shown in Fig. 2(c). This change in the current is an indicator of the target DNA presence and con-centration. In other words, the presence of negatively charged DNA on the biosensor surface is translated to a decrease in the potassium ferrocyanide oxidation/reduction current creating a detectible signal change [26], [27].

The DNA sensing electrodes are created by first forming passivation openings on the top metal layer (aluminum) of the CMOS die similarly to how it is done for wire bond pads. Electroless electroplating is then employed to deposit nickel (2 μm), palladium (0.2 μm) and gold (0.1 μm) on the exposed Al surface to form a bio-compatible electrode surface. After the electrode fabrication, the die is wire-bonded and the bonding wires are insulated with a biocompatible epoxy to enable
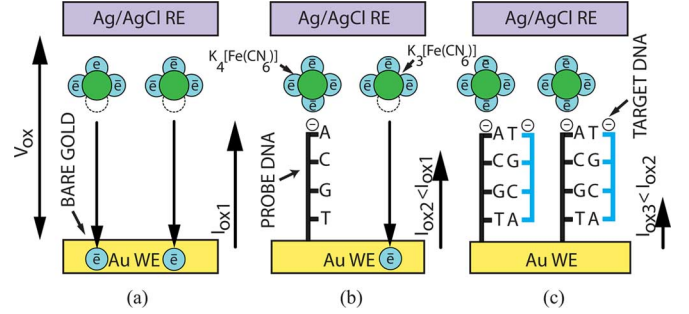

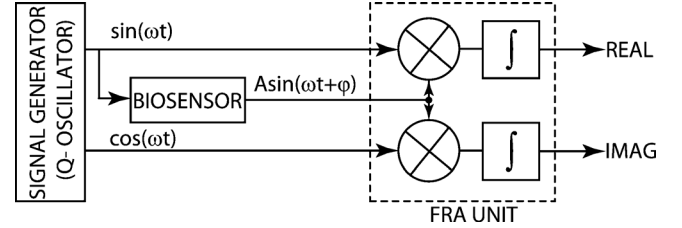Fig. 2. Label-free electrochemical DNA detection principle.

Fig. 3. Block diagram of a frequency-response analyzer (FRA) system for biosensor impedance spectroscopy.

on-chip electrochemical experiments without damaging the bonding wires [18].

III. IMPEDANCE SPECTROSCOPY VLSI ARCHITECTURE

A small-signal model of the electrode-electrolyte interface in an electrochemical cell is shown in the center of Fig. 1. Fast fourier transform (FFT) and frequency-response analyzer (FRA) are two methods widely used for characterizing the electrode impedance [24]. Compared to the FFT, the FRA method requires simple circuitry and can be implemented on a small silicon area, making it suitable for sensory array mi-crosystems. A functional block diagram of the FRA algorithm is shown in Fig. 3. The sensor is interrogated with a sinusoidal voltage. Multiplication of the sensor response $A \sin(\omega t + \phi)$ with $\sin(\omega t)$ or $\cos(\omega t)$ and integration of the results over one cycle of the interrogation signal results in separation of the real and the imaginary components of the sensor impedance as follows [24]

$$
\begin{aligned}
Real &= \int_0^T A sin(\omega t + \phi) \times sin(\omega t)\, \mathrm{d}t, \\
&= \int_0^T 0.5 \times (A \cos(\phi) + \cos(2\omega t + \phi))\, \mathrm{d}t, \\
&= \frac{0.5T}{\pi} \times A \cos(\phi) \qquad (1) \\
Imag &= \int_0^T A \sin(\omega t + \phi) \times \cos(\omega t)\, \mathrm{d}t, \\
&= \int_0^T 0.5 \times (A \sin(\phi) + \sin(2\omega t + \phi))\, \mathrm{d}t, \\
&= \frac{0.5T}{\pi} \times A \sin(\phi) \qquad (2)
\end{aligned}
$$

where A represents the amplitude, ϕ represents the phase of the sensor impedance and T is the period of the interrogation
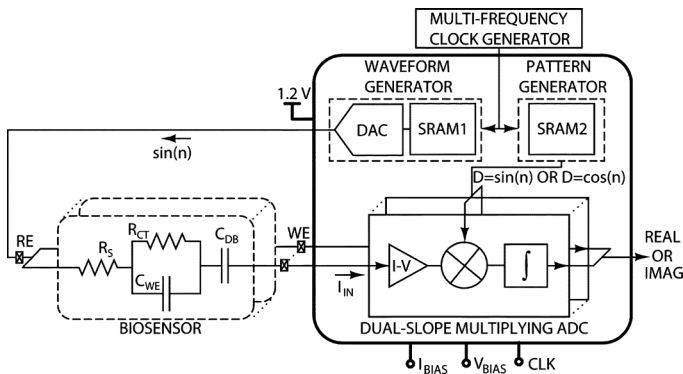
Fig. 4. Impedance spectroscopy microsystem functional block diagram.

Fig. 5. Waveform generator functional block diagram.

signal. $A\cos(\phi)$ is the real portion and $A\sin(\phi)$ is the imaginary portion of the sensor impedance. These values over a wide frequency range are sufficient to fully describe the sensor impedance.

In this work the FRA algorithm has been chosen to implement a sensory array impedance spectroscopy microsystem. The two key components in this system are the multiplier and the digital integrator. Both of these operations are implemented with an in-channel multiplying dual-slope ADC that reuses the circuits of a conventional dual-slope ADC [28].

IV. CIRCUIT IMPLEMENTATION

A. Multi-Channel System-Level Architecture

The functional block diagram of the impedance spectroscopy microsystem based on the FRA algorithm is shown in Fig. 4. The microsystem is comprised of a programable analog waveform generator, a programmable digital pattern generator and an array of impedance extraction units. The waveform generator produces the interrogation waveform $\sin(\omega t)$ and drives the reference electrode with it. The digital pattern generator generates digital multiplication coefficients representing either sine wave or cosine wave that are synchronized with the interrogation waveform. Each impedance extraction unit consists of a dual-slope multiplying ADC (DS-MADC). The front-end current-to-voltage converter is an analog integrator that acquires an input current at the low-impedance input node set to a controlled potential. The DS-MADC multiplies the biosensor response I_{IN} with a set of digital coefficients D representing $\sin(\omega t)$ or $\cos(\omega t)$ that are synchronized with the analog sinusoidal interrogation voltage on the reference electrode. Next the DS-MADC accumulates the results over one period of the interrogation signal using a digital integrator (counter), thus extracting the real or the imaginary components of the biosensor impedance.

B. Waveform Generator and Pattern Generator

The frequency response analysis implementation is the simplest when rectangular waveforms are used instead of sine wave for both the interrogation and the multiplication signals. The problem is that severe systematic errors appear due to the higher order harmonics existing in the rectangular waveforms. Stepwise approximation of the interrogation waveform and the multiplication signals reduces the effect of higher order harmonics
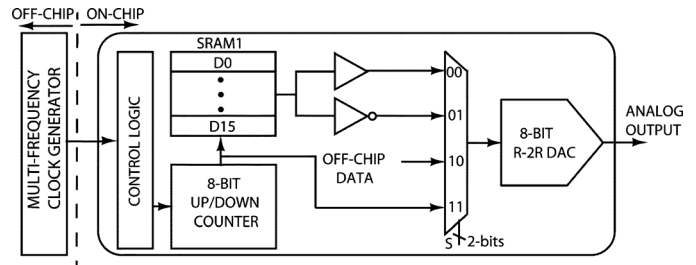
and increases the measurement accuracy. It has been shown [22] that representing both the interrogation signal and the multiplication signals by a coarsely quantized approximation can significantly reduces the error due to the higher order harmonics and can significantly reduce the measurement inaccuracy.

In this work a programmable analog waveform generator is utilized to generate the stepwise approximation of the interrogation signal. The block diagram of the programmable waveform generator is shown in Fig. 5. It is composed of an 8-bit R-2R DAC, an on-chip SRAM1 and a bidirectional counter. The DAC coefficients are stored in the on-chip SRAM1. The on-chip waveform generator generates both stepwise sinusoidal and cyclic voltammetry (CV) ramp waveforms. It provides a wide range of user-controlled rate and amplitude parameters with a maximum CV scan range of 1.2 V, and scan rate ranging between 0.1 mV/sec to 400 V/sec and the sinusoidal frequency range from 100 mHz to 50 kHz. An off-chip clock generator provides the variable frequency clock signal enabling the waveform generator to generate the interrogation signal at different frequencies. The DAC occupies an area of 0.012 mm^2 and dissipates 1.1 mW of power from a 1.2 V supply when driving a load of 5 nF at 50 kHz. At low frequencies the interrogation sine wave is represented by 64 samples per period. The DAC coefficients for the first 16 samples (D_0 to D_{15}) of the waveform generator output waveform and for the corresponding digital sin/cos multiplication coefficients are stored in two on-chip global SRAM banks (SRAM1 and SRAM2, respectively), as shown in Fig. 4. The SRAMs occupy an area of 0.028 mm^2 and dissipate 0.9 μW of power when clocked at 50 kHz. By symmetry, 64 samples in one period are generated from the 16 samples stored on-chip. As shown in Fig. 6, for a sine wave, the first 16 samples stored in the SRAM1 generates the first quadrant of the sine wave. In this case the counter controlling the SRAM1 is counting up and S is set to 00, in Fig. 5. In the next quadrant the counter controlling the SRAM1 counts down thus reversing the order of the samples and generating the second quadrant of the sine wave. S is set to 00 in this case. The third and forth quadrants are generated in the same manner but in this case the polarities of the samples fed into the DAC are reversed (by setting S to 01). To generate a cosine, the cycle starts from the second quadrant instate of the first one. If a CV waveform is required the up/down counter is directly interfaced to the waveform generator DAC (by setting S to 11).

As the interrogation frequency increases, the number of samples representing the interrogation and multiplication signals decreases and at 10 kHz both signals are represented by three
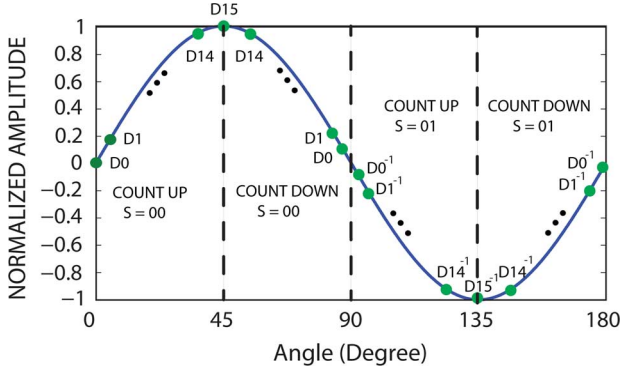
Fig. 6. Principle of the sine wave generation.

samples. This greatly reduces the ADC speed requirement while the error caused by the reduction in number of samples is kept low by averaging the results over multiple cycles.

An ideal model of the impedance spectroscopy microsystem has been constructed using verilog-A model components (ideal analog integrator and multiplying ADC) to study the effect of step-wise approximation of the interrogation signal on the overall system accuracy. First a simulation was performed where a sinusoidal voltage stimulus (8-bit accurate generated by an ideal DAC) with the frequency swept from 0.1 Hz to 10 kHz was applied to the biosensor model shown in Fig. 4. The value of R_S was set to 1 GΩ, C_{WE} was set to 500 pF, C_{DB} was set to 300 pF and R_{CT} was set to 1 MΩ. The sensor response was recorded with the ideal analog integrator and multiplied, using an ideal multiplying dual-slope ADC, by an 8-bit accurate digital multiplication coefficient representing sine or cosine in the FRA algorithm in Fig. 3. Next, the same set of simulations were performed in which both digital multiplication coefficients and the analog sinusoidal voltage interrogation signal are represented by 64 samples per period at low frequencies. In this simulation as the interrogation frequency increases, the number of samples representing the interrogation and multiplication signals decreases. Also, in this simulation the results are averaged over multiple cycles (N) to reduce the errors caused by reduction in the number of samples. The absolute value of the relative error of the biosensor impedance computed using 8-bit accurate interrogation signal and 8-bit accurate multiplication coefficients versus the simulated biosensor impedance obtained from stepwise approximation of these signals is shown in Fig. 7. The absolute value of the relative error stays below 0.9% and 1.0% for real and imaginary component of the biosensor, respectively.

C. Dual-Slope Multiplying ADC Channel

The VLSI architecture of one channel of the integrated spectrum analyzer is depicted in Fig. 8(a). Each channel consists of an integrating amplifier with an on-chip 10 pF capacitor C_F, a high-speed latched comparator and digital blocks. The integrator switches are implemented with low-leakage switches as shown.

The conventional dual-slope ADC operates in two phases as depicted in Fig. 9. In phase I the integrating capacitor C_F is charged for a predetermined period of time T_1. Next, during the
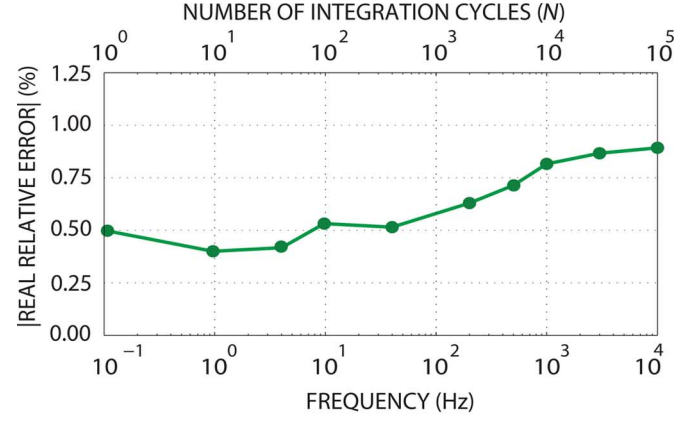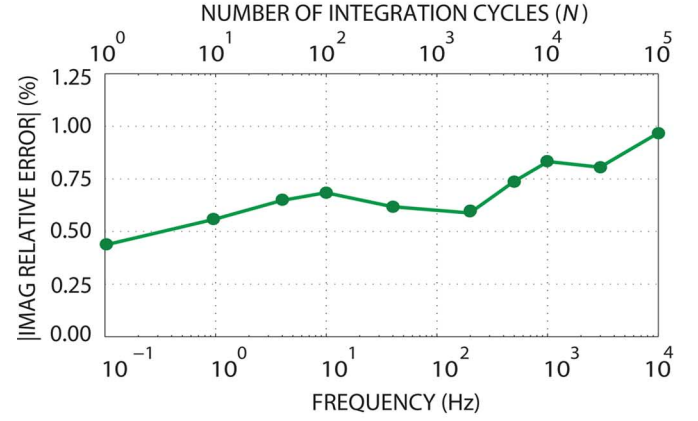
Fig. 7. Absolute value of the relative error of the biosensor $R - C$ model impedance as a function of frequency due to stepwise approximation of the interrogation signal for the (a) real and (b) imaginary components.

second phase of the operation, the capacitor is discharged to zero by a DC reference current. By counting the time T_2, a digital representation of I_{IN} can thus be obtained as $(T_2/T_1) \times I_{REF}$. To implement multiplication of the input current by a digital sin/cos coefficient (D_1 to D_{15}) as needed by the FRA algorithm, the duration of phase I is scaled with a constant coefficient $D < 1$ as shown in Fig. 9. In this case by counting the time DT_2, a digital representation of DI_{IN} can be obtained as $D \times (T_2/T_1) \times I_{REF}$. To extract the real and imaginary components of the biosensor impedance, the input current I_{IN} is multiplied by the reference sine or cosine digital coefficient denoted as D (stored in SRAM2, in Fig. 4) and the results are integrated over one period by a 16-bit counter as follows:

$$Real = \int_0^T I_{IN} \times \sin(\omega t)dt$$

$$= \sum_1^{N/2} I_{IN} \times |\sin[n]| - \sum_{N/2+1}^N I_{IN} \times |\sin[n]| \quad (3)$$

$$Imag = \int_0^T I_{IN} \times \cos(\omega t)dt$$

$$= \sum_1^{N/2} I_{IN} \times |\cos[n]| - \sum_{N/2+1}^N I_{IN} \times |\cos[n]| \quad (4)$$
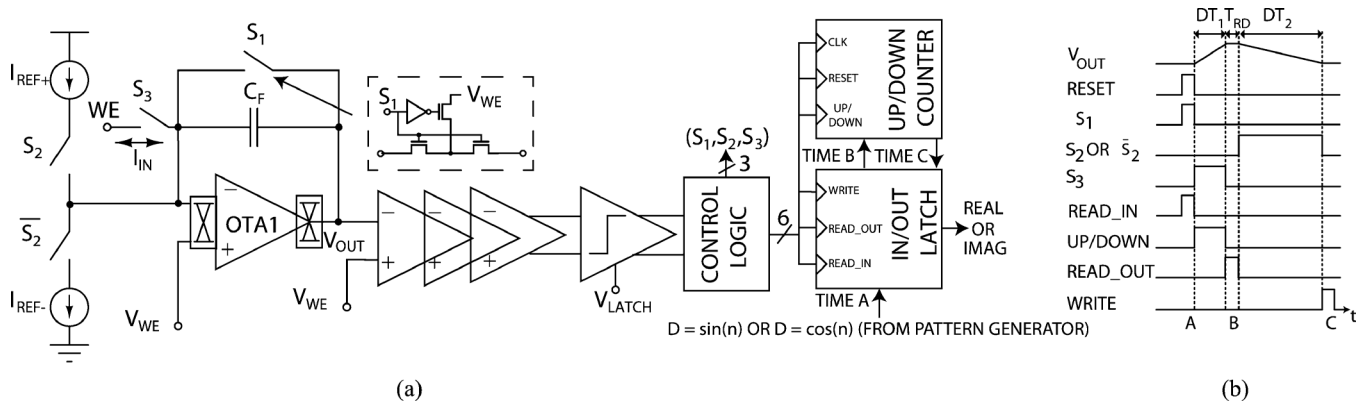
Fig. 8.   (a) Dual-slope multiplying ADC VLSI architecture. (b) Timing diagram of all relevant signals.
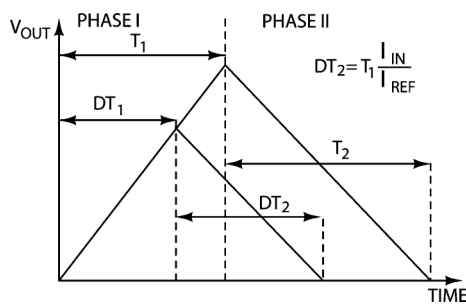

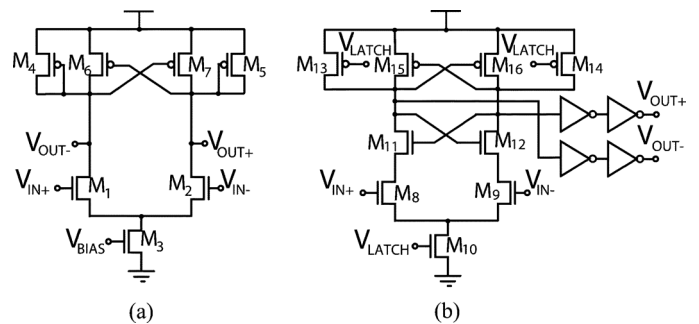Fig. 9.   Timing diagram illustrating the ADC multiplication function.

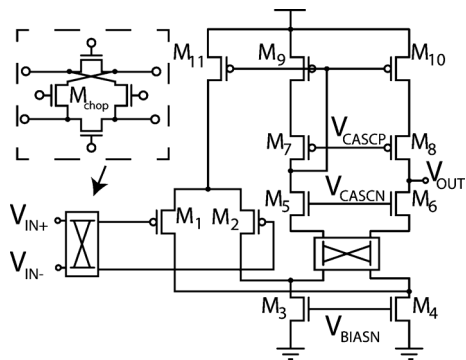Fig. 11.   Comparator circuit diagram. (a) One of the three identical gain stages. (b) The high-speed latch.

Fig. 10.   Chopper-stabilized folded-cascode OTA1 in the analog integrator.

Fig. 12.   Simulated input-referred noise spectrum of the analog integrator with the chopper on and off (clocked at 100 kHz) from 0.01 Hz to 10 kHz.

where N is the number of samples in one period and $\sin[n]$ and $\cos[n]$ are the digital multiplication coefficients D that are stored in the SRAM2. The multiplying dual slope ADC performs the multiplication required by (3) and (4), thus the need for 16 digital multipliers is eliminated.

The timing diagram of the ADC for a typical conversion cycle is shown in Fig. 8(b). First, the integrating counter is reset. At the same time, the sin/cos multiplication coefficient, D, is loaded into the in-channel input latch (time A). Next, the in-channel counter counts up from zero to time DT_1 and the input current is integrated onto capacitor C_F. After time DT_1, the voltage on the capacitor is held constant for a fixed time interval T_{RD}. During this time the content of the output latch (zero for the first conversion cycle) is loaded into the counter (time B). During time DT_2, depending on the comparator
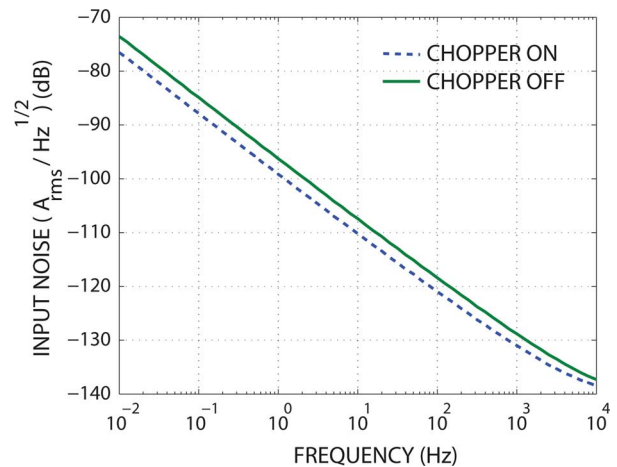
output, the integrating capacitor is discharged using the appropriate current source, I_{REF+} or I_{REF-}. During time DT_2 the counter counts up or down depending on the sign of the input current in phase I and the final value of the counter is written into the output latch (time C). This part of the ADC conversion cycle performs the summation which implements integration required by the FRA algorithm. This process is repeated for one full cycle of the sinusoidal stimulation waveform and the final value stored in the output latch corresponds to the real or imaginary component of the biosensor impedance, for sin and cos multipliers respectively.
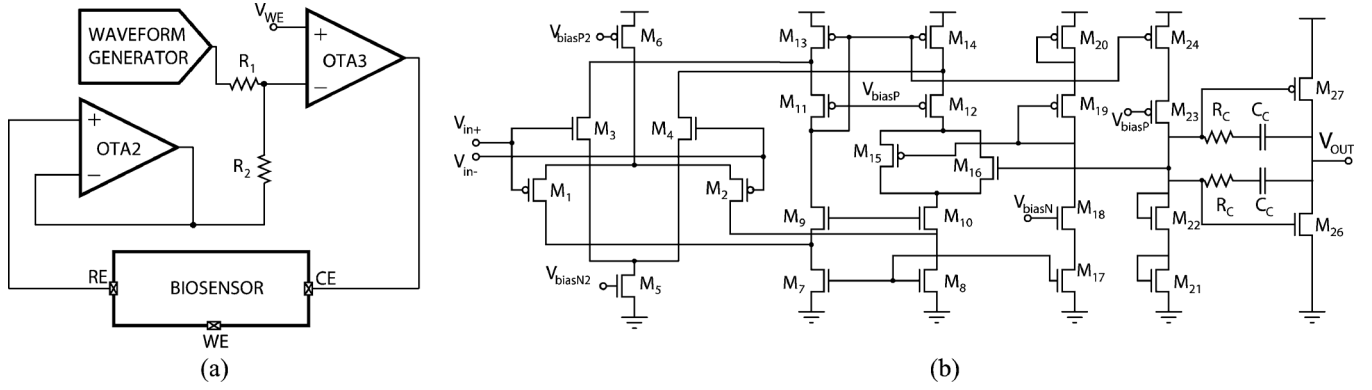
Fig. 13. (a) Circuit architecture of the three-electrode regulation loop. (b) OTA2 and OTA3 circuit schematic.

TABLE I
OTA1 AND COMPARATOR TRANSISTOR SIZING

OTA1 Transistor	W/L (μm)	Comparator Transistor	W/L (μm)
$M_{1,2}$	$8 \times 3/1$	$M_{1,2}$	$12 \times 12/0.2$
$M_{3,4}$	$2 \times 1/4$	M_3	$3 \times 2/4$
$M_{5,6}$	$4 \times 1/1$	$M_{4,5}$	$2 \times 1.5/0.4$
$M_{7,8}$	$8 \times 1/1$	$M_{6,7}$	$2 \times 1.5/0.4$
$M_{9,10}$	$4 \times 1/4$	$M_{8,9}$	$6 \times 6/0.5$
M_{11}	$8 \times 1/2$	M_{10}	$3 \times 2/4$
–	–	$M_{11,12}$	$6 \times 6/0.5$
–	–	$M_{13,14}$	$2 \times 1.5/1$

TABLE II
ANALOG INTEGRATOR NOISE SUMMARY

Transistor	Noise Source	Total Noise, Chopper OFF	Total Noise, Chopper ON
$M_{3,4}$	Flicker	26.4%	11.02%
$M_{1,2}$	Flicker	22.1%	10. 3%
$M_{3,4}$	Thermal	21.2%	23.4%
$M_{1,2}$	Thermal	18.3%	22.1%
$M_{9,10}$	Flicker	5.25%	17.50%
$M_{9,10}$	Thermal	3.26%	8.26%
$M_{5,6}$	Flicker	1.1%	3.38%
$M_{7,8}$	Flicker	1.04%	1.19%
$M_{5,6}$	Thermal	0.9%	1.0%
$M_{7,8}$	Thermal	0.8%	0.9%

TABLE III
OTA2 AND OTA3 TRANSISTORS SIZING

Transistor	W/L (μm)	Transistor	W/L (μm)
$M_{1,2}$	$6 \times 2/6$	M_{16}	$1 \times 1.2/1$
$M_{3,4}$	$2 \times 1.5/0.4$	M_{17}	$1 \times 1.2/1$
$M_{5,6}$	$2 \times 1.5/0.4$	M_{18}	$1 \times 1.2/1$
$M_{7,8}$	$3 \times 2/0.12$	$M_{19,20}$	$1 \times 1.2/1$
$M_{9,10}$	$3 \times 2/0.12$	$M_{21,22,23,24}$	$3 \times 2/0.12$
M_{11}	$1 \times 1.2/1$	M_{25}	$3 \times 2/0.12$
$M_{12,13,14,15}$	$3 \times 2/0.12$	M_{26}	$1 \times 1.2/1$
$M_{9,10}$	$3 \times 2/0.12$		

The analog integrator amplifier shown in Fig. 10 is a folded-cascode transconductance amplifier consuming 6 μW from a 1.2 V supply. Impedance spectroscopy is performed over the frequency range of 1 Hz to 10 kHz. To reduce the effect of flicker noise, the amplifier utilizes input PMOS devices with a high aspect ratio and internal chopping. As shown in Fig. 10, the chopper switches are placed at the input of the OTA. Another set is placed between the cascoded NMOS current mirrors. This significantly reduces the flicker noise and DC offsets caused by the input pair transistors and the NMOS current mirror transistors.

The simulated input-referred noise of the integrator for the cases where the chopper is disabled and enabled is shown in Fig. 12. The integrated input-referred noise from 0.01 Hz to 10 kHz is 0.12 pA when the chopper is disabled and 0.07 pA when the chopper is enabled. The integrator transistor sizes are shown in Table I. Contribution of each transistor to the total input-referred noise is shown Table II. When the chopper is disabled the main contributions are from the OTA current mirror transistors M_3 and M_4 and the input pair transistors M_1 and M_2. When the chopper is enabled, the current mirror transistors M_9 and M_{10} are the main contributors to the input-referred noise.

The comparator is implemented with three pre-amplifier stages [Fig. 11(a)], with a total gain of 60 dB, and a high-speed output latch as shown in Fig. 11(b). The comparator is verified in simulation to operate at up to 40 MHz. The full channel consumes 42 μW of power from a 1.2 V supply when clocked at 10 MHz. The comparator transistor sizes are shown in Table I.

D. Three-Electrode Regulation Loop

The functional block diagram of the regulation loop is shown in Fig. 13(a). A three-electrode potentiostat configuration [29] is employed as opposed to the basic two-electrode configuration shown in Fig. 1. In a two-electrode configuration the current flowing between the two electrodes alters the voltage drop across C_{DB} due to the non-zero impedance of the electrolyte solution and the electrode-electrolyte interface. In the three-electrode configuration, a third, counter electrode (CE), rather than the reference electrode is placed in the current path. The reference electrode does not sink/source an electric current. Thus the voltage difference between the working and reference electrode is maintained at a known voltage independent of the electrochemical cell impedance. The three-electrode regulation loop is composed of the two OTAs as shown in Fig. 13(a). To allow for wide input and output swings class-AB OTAs with both NMOS and PMOS input differential pairs are used for the potentiostat as shown in Fig. 13(b). OTA transistor sizing is given
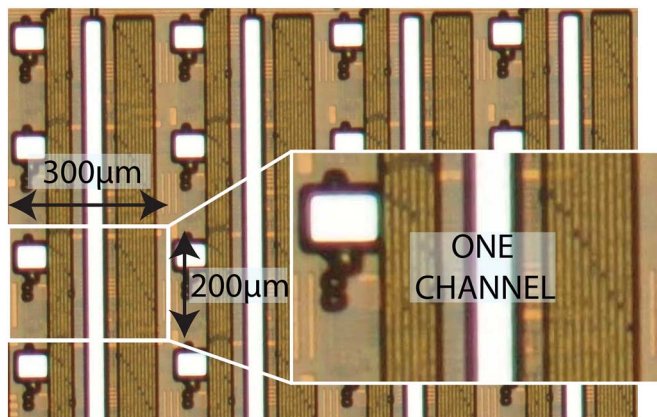
Fig. 14.   Die micrograph of the 1.05 mm×1.6 mm 16-channel integrated impedance spectrum analyzer fabricated in a 0.13 μm standard CMOS technology.
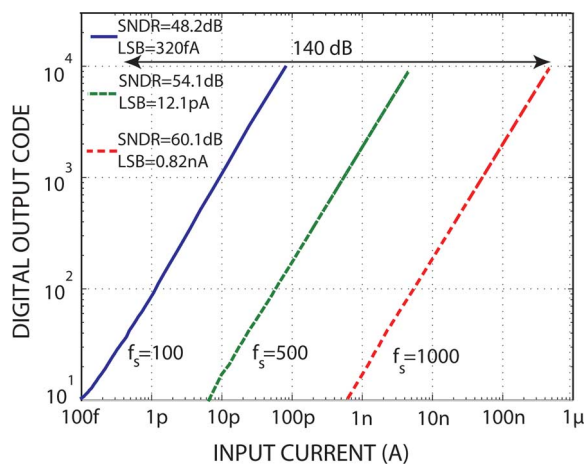

Fig. 15.   Experimentally measured transfer characteristics of the impedance spectrum analyzer channel for three sampling frequencies.
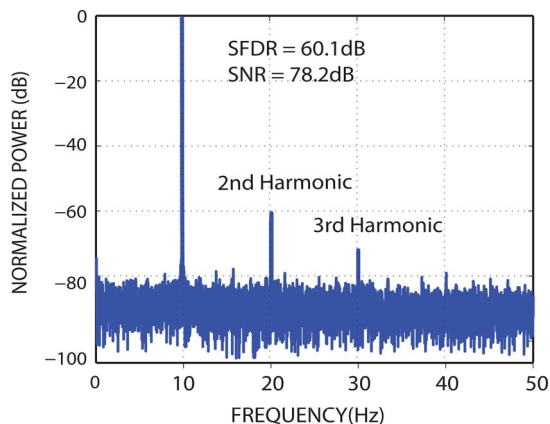

Fig. 16.   Experimentally measured output spectrum of the ADC for a 10 Hz sinusoidal input.

Fig. 17.   Waveform generator DNL.
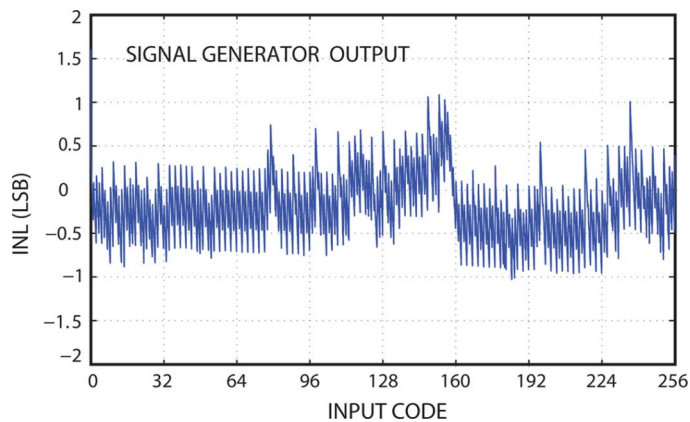
Fig. 18.   Waveform generator INL.
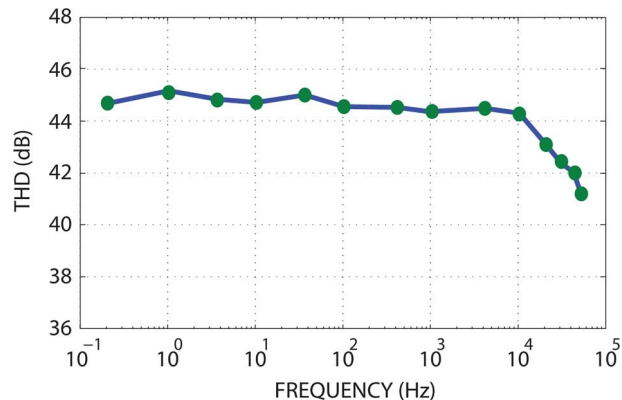
Fig. 19.   Total harmonic distortion of waveform generator DAC.

V. Electrical Experimental Results

The 16-channel 1.2×1.6 mm^2 integrated impedance spectrum analyzer prototype was implemented in a 0.13 μm CMOS process with a 1.2 V supply. The die micrograph is shown in Fig. 14. Each channel consists of 4 WEs, with different WE sizes (55 μm $\times$ 55 μm, 5 μm $\times$ 5 μm, and two 2 μm $\times$ 2 μm) to cover a wide combined dynamic range. Each column of four working electrodes shares a 45 μm-wide Au reference and counter electrodes driven by the on-chip waveform generator. Each channel consists of the analog integrator, dual-slope multiplying ADC and in-channel bias and clock generator. Each channel WE can

in Table III. Assuming that V_{WE} is fixed by the analog integrator, the regulation loop configuration ensures that $V_{RE} - V_{WE}$ tracks the voltage difference between the output of the waveform generator and the positive terminal of the OTA3.
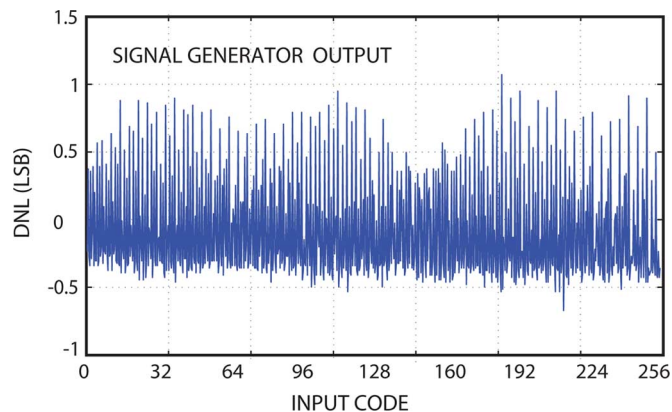
TABLE IV
EXPERIMENTALLY MEASURED CHARACTERISTICS

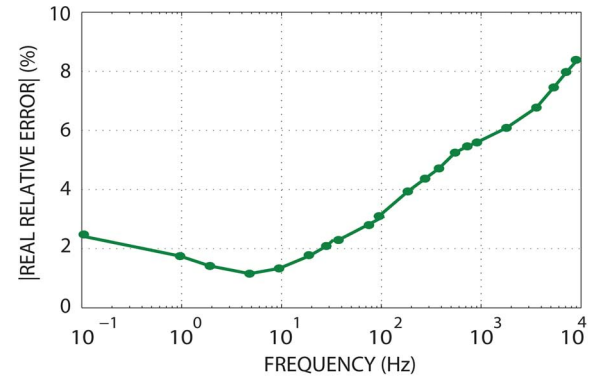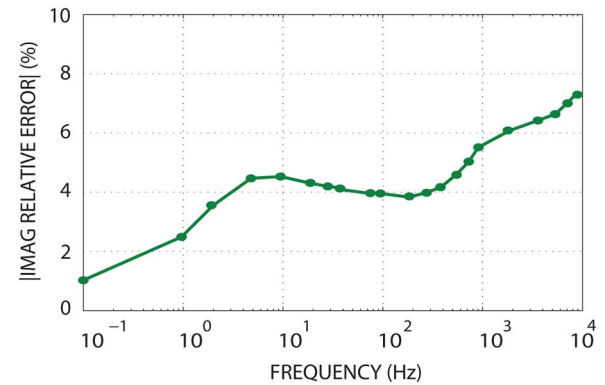|	
Technology	0.13μm CMOS
Supply Voltage	1.2V
Area	1.05mm×1.6mm
Array Dimensions	4×4 channels
Channel Size	300μm×200μm
Sensitivity	320fA
Channel SNR (f_{clk}=10MHz)	78.2dB
Channel SFDR (f_{clk}=10MHz)	60.1dB
Power Consumption	
DAC	1.1mW
SRAM	1.3μW
Analog Integrator	8μW
Comparator	19μW
Biasing	4μW
Digital	11μW
Total (channel)	42μW

Fig. 20. Off-chip biosensor model impedance as a function of frequency experimentally measured by the impedance spectroscopy microsystem. (a) Real. (b) Imaginary components.

Fig. 21. Absolute value of the relative error of the off-chip biosensor model impedance as a function of frequency. (a) Real. (b) Imaginary components.

be set to a specific voltage independently, allowing for simultaneous detection of different DNA strands.

The digital output of one channel for the input current swept between 100 fA and 400 nA is shown in Fig. 15. The static input dynamic range is 140 dB cumulatively for the three sampling frequency settings, or 55.4 dB at 1 MHz clock. The dynamic range for each setting is computed by taking the ratio of the maximum signal that saturates the ADC to the LSB for a given sampling frequency setting. Dynamic performance of an entire channel was measured by applying a 10 Hz full scale (400 nA)

sinusoidal input current with the ADC clocked at 10 MHz. Fig. 16 shows the 65536-point FFT of the measured ADC output. The strong second harmonic is due to the single-ended architecture of the ADC. The resulting effective number of bits (ENOB) is 9.3. The DNL and INL of the waveform generator are shown in Figs. 17 and 18, respectively. The waveform generator achieves an static accuracy of 8 bits. Dynamic performance of the waveform generator was characterized by measuring the total harmonic distortion of the DAC versus frequency. Fig. 19 shows the THD of the measured DAC output. The DAC archives a THD of greater than 42 dB over the operating frequency range.

The electrode model shown in Fig. 1 was used first to emulate the biosensor. The value of R_S was set to 1 G Ω, C_{WE} was set to 500 pF, C_{DB} was set to 300 pF and R_{CT} was set to 1 MΩ. To verify the impedance extraction capability of the microsystem, a sinusoidal voltage stimulus (generated by the on-chip DAC) with the frequency swept from 0.1 Hz to 10 kHz was applied to the biosensor model. Fig. 20(a) and (b) demonstrate that the fabricated prototype tracks the theoretical model well over the full range of frequencies. The absolute value of the relative error of the ideal biosensor impedance verses the measured biosensor impedance as a function of frequency is shown in Fig. 21. The absolute value of the relative error stays below 8.4% and 7.5% for real and imaginary component of the biosensor respectively.

Table IV provides a summary of experimentally measured characteristics of the integrated impedance spectroscopy microsystem.
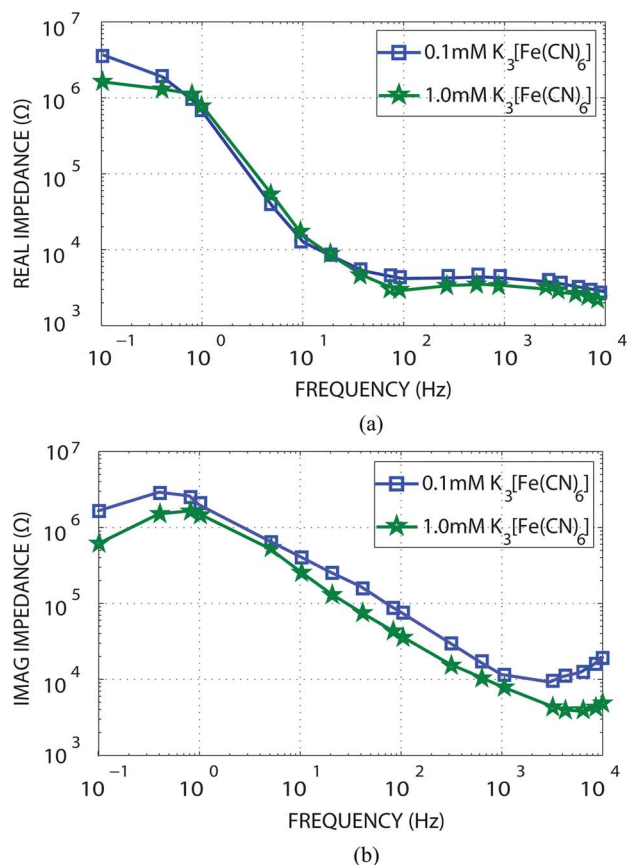
Fig. 22. Potassium ferricyanide solution impedance as a function of frequency experimentally measured by the impedance spectroscopy microsystem. (a) Real. (b) Imaginary components.

VI. ELECTROCHEMICAL EXPERIMENTAL RESULTS

A set of electrochemical experiments have been conducted to validate the functionality of the impedance spectroscopy microsystem. In these tests a 3-electrode setup has been utilized with on-chip gold-plated 55 μm × 55 μm working electrode, on-chip gold plated counter electrode and an off-chip Ag-AgCl reference electrode. The reference and counter electrodes are driven by the on-chip three-electrode regulation loop as shown in Fig. 13(a) and all the excitation waveforms are generated using the on-chip waveform generator.

First, in order to validate the design, impedance spectroscopy recordings of 0.1 mM and 1 mM potassium ferricyanide in 1 μM potassium phosphate buffer (pH 7.3) were carried out. A 9 mV 0.1 Hz to 10 kHz sine wave was applied between the WEs and an off-chip Ag-AgCl reference electrode. The real and imaginary impedance results obtained from the two concentrations of the potassium ferricyanide solution are shown in Figs. 22(a) and (b). An increase in the concentration of the potassium ferricyanide results in a decrease in value of R_S and R_{CT} and increase in value of C_{WE}. The measurements of potassium ferricyanide validate impedance spectroscopy microsystem in DNA sensing applications.

The SoC was also extensively validated in DNA analysis for detection of prostate cancer. Fig. 23(a) shows real and imaginary impedance components of an on-chip Au electrode hybridized with 5 μM single-stranded prostate cancer probe DNA.
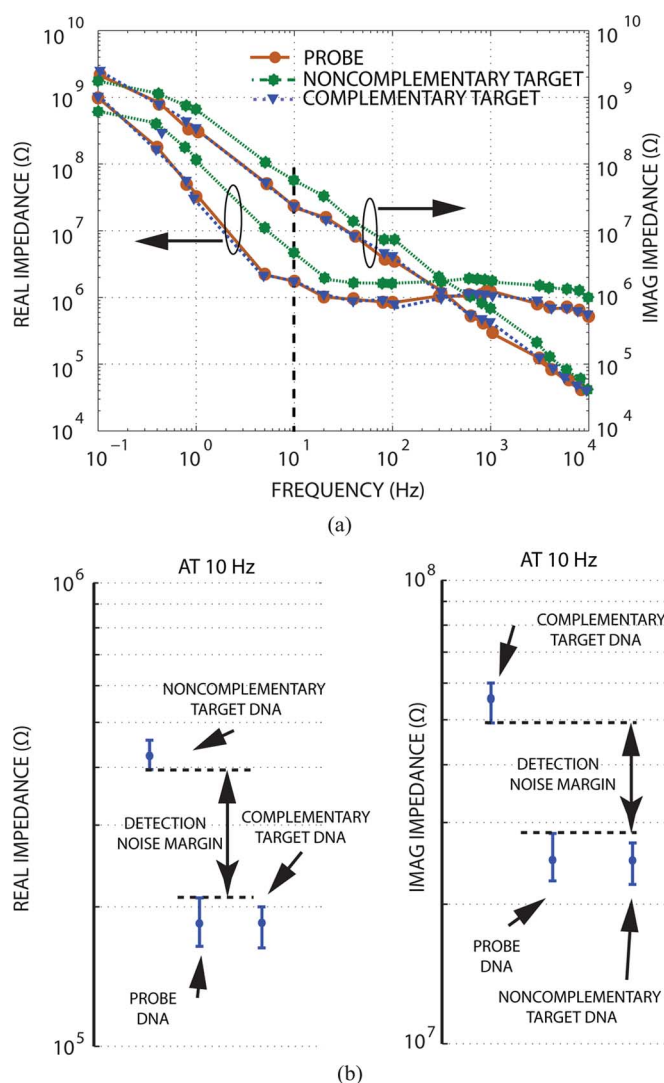
Fig. 23. (a) Impedance spectrum of 5 μM prostate cancer DNA probe, complementary, and non-complementary targets. (b) The corresponding 3-sigma error bars (from 3 chips, 20 measurements each).

Adding a 5 μM noncomplementary target DNA does not significantly change the real and imaginary components of the electrode impedance indicating that non-specific adsorption is negligible. Adding a 5 μM complementary prostate cancer target DNA leads to significant reduction of potassium ferrocyanide redox current, resulting in increase in both real and imaginary components of the electrode impedance. This is due to the additional negative surface charge resulting from formation of double-stranded DNA on the electrode surface. The 3-sigma error bars (from 3 chips) with the real and imaginary impedance detection noise margins of approximately 18.3 KΩ and 20.9 MΩ respectively are shown in Fig. 23(b).

Table V provides a comparative analysis of the presented design and existing amperometric biochemical sensory microsystems. The design presented in this work achieves the highest dynamic range and the lowest sensitivity in terms of LSB. Also, the design presented in this paper requires less time to extract real and imaginary components of the biosensor compared to

TABLE V
COMPARATIVE ANALYSIS OF REPORTED AMPROMETRIC SENSORY MICROSYSTEM

System	ISSCC 08 [1]	JSSC 08 [8]	JSSC 09 [21]	ISSCC 10 [4]	ISSCC 10 [3]	TBIOCAS 07 [16]	This Work
Technology(CMOS)	$0.18\mu m$	$0.25\mu m$	$0.5\mu m$	$0.35\mu m$	$0.6\mu m$	$0.5\mu m$	$0.13\mu m$
Power	25mW	160mW	0.6mW	84.5mW	—	1.2mW	0.35mW
Supply Voltage	5.0V	2.5V	3.0V	3.3V	3.3V	3.0V	1.2V
Chip Area	$11.2mm^2$	$15mm^2$	$2.25mm^2$	$4mm^2$	$25.8mm^2$	$9mm^2$	$1.68\,mm^2$
Electrode Count	576	48	100	100	40	16	64
Channel							
Channel Count	24	16	100	100	40	16	16
Type Of	2D	2D	2D	2D	—	Off	2D
Electrodes	Polymer	Gold	Gold	Gold	—	Chip	Gold
Power	—	10mW	$6\mu W$	0.84mW	—	$4.3\mu W$	$42\mu W$
Dynamic Range	—	60dB	50dB	97dB	80dB	—	140dB (3-mode)
Conversion Rate	10Hz	10kHz	10kHz	—	1Hz	10Hz	10kHz
Sensitivity(LSB)	97pA	240pA	—	330pA	$25\mu V$	—	320fA
ENOB	11 bits	9 bits	8 bits	No ADC	12 bits	8 bits	9.3 bits
Waveform Generator	—	—	Yes	Yes	—	—	Yes
Type	—	—	Square Wave	Square Wave	—	—	8-bit Programmable
Frequency	—	—	10KHz	50MHz	—	—	10kHz
Power	—	—	—	—	—	—	1.1mW (5nF Load)

the FRA implementations in which a square waveform is utilized for multiplication and integration. The stepwise approximation of the interrogation waveform and multiplication coefficients significantly reduces the systematic error caused by higher order harmonics present in the rectangular waveforms, thus eliminating the need for excessive averaging that is time consuming at the lower frequency range. This enables real-time monitoring and analysis of DNA hybridization.

VII. CONCLUSION

A 16-channel, mixed-signal CMOS impedance spectroscopy DNA analyzer is presented. It consists of a programable waveform generator, on-chip memory and multiple impedance extraction units. Multiplication and integration, two operations required for frequency response analysis (FRA) algorithm, are efficiently performed by the in-channel current-mode input dual-slope multiplying ADC with negligible resources overhead. The ADC combines impedance extraction and analog-to-digital conversion into a single conversion cycle. The impedance spectroscopy microsystem was implemented in a CMOS 0.13 μm technology. Each channel occupies an area of 0.06 mm^2 and consumes 42 μW of power from a 1.2 V supply.

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