spurious signals. The level of the spurious signals was analyzed, and the relative mismatch errors should be smaller than $10^{-\mathrm{SFDR}/20}$, where SFDR is the required dynamic range. In practice, this easily limits the dynamic range to -40–50 dBc unless the incompletely cancelled images are hidden underneath the fundamental signals by choosing a carrier frequency of $fs/4$.

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Dynamic MOS Sigmoid Array Folding Analog-to-Digital Conversion

Roman Genov and Gert Cauwenberghs

***Abstract*—A dynamic, saturating difference circuit for large-scale parallel folding analog-to-digital conversion is presented. The circuit comprises a subthreshold nMOS transistor source-coupled to a capacitor, implementing a log-domain integrator. The output current is a logistic sigmoidal function of the change in voltage on the gate. Offset and gain of the differential sigmoid are controlled by timing of global clock signals and are independent of transistor mismatch. Folding operation for analog-to-digital conversion is obtained by differentially combining and integrating currents from a bank of sigmoid units. A 128-channel parallel bank of 4-bit Gray-code folding analog-to-digital converters measures 0.75 mm $\times$ 2 mm in 0.5 μm CMOS and delivers 768 Msps at 82-mW power dissipation.**

***Index Terms*—Charge-mode comparator, correlated double sampling, diode integrator, folding analog-to-digital converter (ADC), interpolating ADC, sigmoid.**

I. INTRODUCTION

High-performance data conversion can be achieved either by expending power and area to achieve high precision in a single analog architecture or by distributing the architecture over multiple low-resolution quantization tasks, each implemented with relatively imprecise analog circuits, and combined in the digital domain. Delta-sigma modulation has proven to be superior in attaining very high precision by distributing the quantization process over time [1]. Both high speed and high resolution can be achieved by distributing the quantization process in space [2].

The highest speeds in analog-to-digital conversion are obtained with flash and folding converter architectures. A folding analog-to-digital converter (ADC) compared to a flash ADC offers fewer comparators and reduced decoding logic, thus allowing higher speed at lower power [3]. A folding interpolating ADC further interpolates the folded output signals to increase resolution or reduce folding rate in a multistage conversion architecture.

Fig. 1(a) depicts an example 3-bit folding ADC [4], [5]. Each of the three folding circuits comprises identical saturating difference units at linearly spaced inflection voltages, whose outputs are combined in alternating fashion. The folded output signals are zero-thresholded by high-gain comparators, producing Gray-code outputs illustrated in Fig. 1(b). The comparator outputs are latched and digitally postprocessed to generate binary-coded outputs.

Conventionally, the saturating difference unit (σ) of a folding circuit is implemented as a bipolar junction transistor (BJT) or MOS differential pair. The differential output current is a saturating monotonic smooth (sigmoid) function of the differential input voltage. For instance, in the case of a MOS differential pair shown in Fig. 2(a) and

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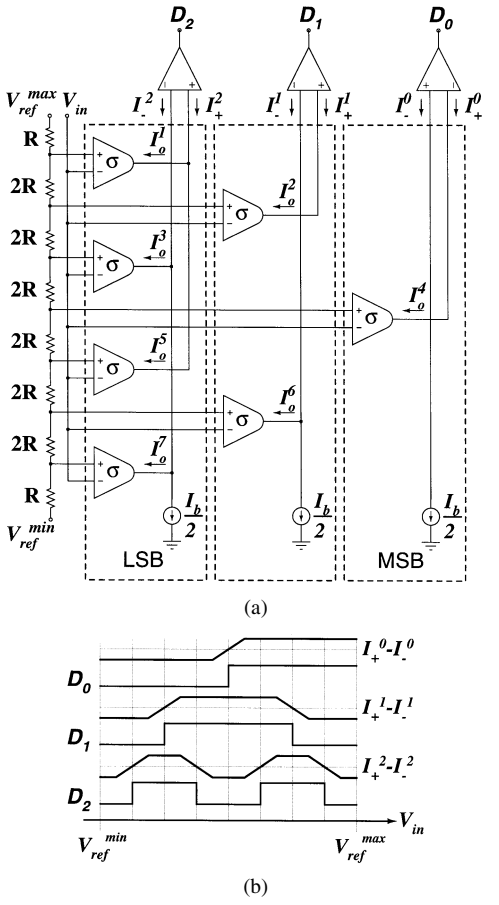

Fig. 1. A 3-bit Gray-code folding ADC. (a) Architecture. (b) Folding currents and thresholded Gray-code output.

biased in the subthreshold region, one of the complementary output currents can be expressed as [6], [7]

$$I_o = I_b\,\sigma\Big(A(V_{\rm ref} - V_{\rm in})\Big) \tag{1}$$

where I_b is the bias tail current, $A = \kappa/V_t$ is a voltage range factor set by the Boltzmann thermal voltage $V_t = kT/q$ and gate coupling coefficient κ, and

$$\sigma(x) = \frac{1}{1+e^{-x}} \tag{2}$$

is the canonical logistic sigmoid function.

The complementary output currents are differentially combined, with alternating polarity, to construct the folded output current illustrated in Fig. 1(b). Proper folding operation relies on precise addition and subtraction of sigmoid functions with identical saturation level I_b and with linearly spaced points of inflection $V_{\rm ref}$. MOS transistor mismatch in the differential pair and tail current supply contribute variability in the amplitude and offset of the implemented sigmoids, illustrated in Fig. 2(b). To maintain linearity in the ADC characteristic, relative variations in amplitude and offset cannot exceed the least significant bit (LSB) level (2^{-n} for n-bit conversion). Offset and amplitude mismatch can be reduced through enlarged sizing of components, contributing power dissipation. Adaptive autozeroing techniques can compensate for offset [8], but not amplitude mismatch.

We present a compact, offset and amplitude-compensated folding circuit utilizing dynamic differential sigmoid (σ) units, each implemented with one capacitor and four nMOS transistors. Section II describes the sigmoid difference unit, and Section III presents the folding

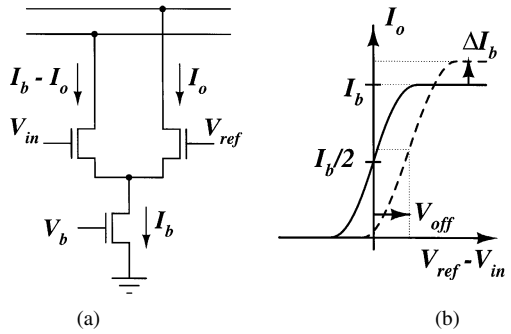

Fig. 2. (a) Conventional folding unit using a MOS differential pair. (b) Sigmoid differencing characteristic.

circuit comprising these units. Section IV summarizes measured results from a densely integrated bank of 128 parallel 4-bit folding Gray-code ADCs fabricated in a 0.5-μm CMOS process.

II. Correlated Double-Sampling Sigmoid Unit

A. MOS-C Diode-Integrator

This section demonstrates that a σ differencing and folding unit can be implemented using a single active element, with precisely controlled sigmoid amplitude and offset. The circuit consists of a capacitor and an exponential element, such as a diode [9] or a MOS transistor operating in the subthreshold regime [10], where the differential voltage is presented as a step in input voltage on the MOS gate. Offset compensation is achieved in the charge domain, similar to the CMOS charge-transfer comparator described in [11].

In the circuit of Fig. 3(a), the nMOS transistor is source-coupled to a capacitor. In the subthreshold and saturation regions, the drain current is exponential in gate and source voltage, and the large-signal dynamics of the integrator are described by

$$C\frac{dV_s}{dt} = I_o(t) = \frac{W}{L}I_0' e^{(\kappa V_g - V_s)/V_t} \tag{3}$$

which, by integrating over t and V_s, yields

$$CV_t e^{V_s/V_t} = \frac{W}{L}I_0' e^{\kappa V_g/V_t}\; t + c_1 \tag{4}$$

with integration constant c_1 as determined by initial conditions. Direct substitution yields

$$I_o(t) = \frac{CV_t}{t + \frac{c_1}{\frac{W}{L}I_0' e^{\kappa V_g/V_t}}}. \tag{5}$$

At time $t = 0$, the input voltage is switched from $V_g(0^-)$ to $V_g(0^+)$ while the capacitor instantly retains the source voltage $V_s(0)$. The source current therefore switches from $I_o(0^-)$ to $I_o(0^+)$ over the transition at the gate as

$$I_o(0^+) = I_o(0^-)e^{\kappa \triangle V_g/V_t} \tag{6}$$

where $\triangle V_g = V_g(0^+) - V_g(0^-)$. The output current (5) can thus be expressed in terms of initial conditions as

$$I_o(t) = \frac{I_o(0^+)}{\frac{I_o(0^+)}{CV_t}t + 1} = \frac{I_o(0^-)}{\frac{I_o(0^-)}{CV_t}t + e^{-\kappa \triangle V_g/V_t}}. \tag{7}$$

Interestingly, for $t \gg CV_t/I_o(0^+)$, $I_o(t)$ becomes independent of initial conditions [9]

$$I_o(t) \approx \frac{CV_t}{t}. \tag{8}$$

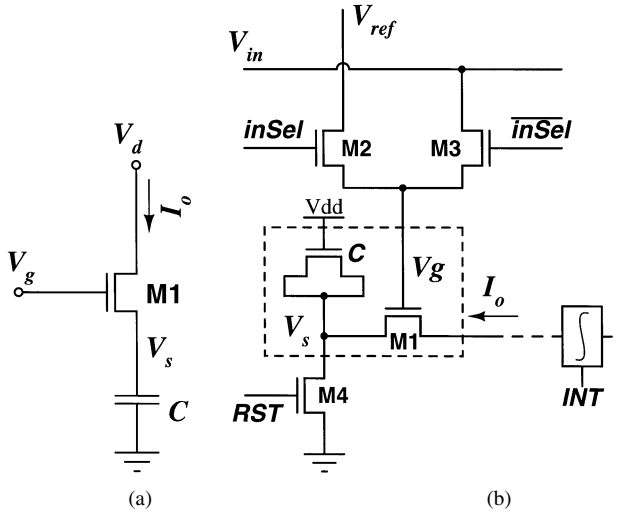

Fig. 3. (a) MOS-capacitor diode-integrator. (b) Dynamic sigmoid (σ) difference folding unit.

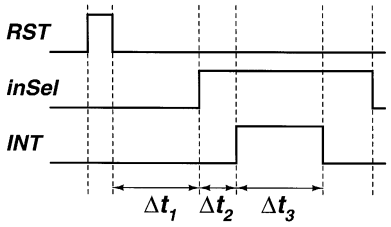

Fig. 4. Control signal timing diagram for the sigmoid (σ) difference unit circuit in Fig. 3(b).

B. Differential Sigmoid Unit

Saturation of the output current of the circuit in Fig. 3(a) as a function of a change in the input voltage V_g is utilized in the design of the sigmoid difference unit as shown in Fig. 3(b). The nMOS capacitor is initially charged by pulsing reset (*RST*), as shown in Fig. 4. Over the time interval $\triangle t_1$, the capacitor discharges to raise V_s until $M1$ reaches well into the subthreshold region. The end of the interval defines the initial condition for the source current $I_o(0^-)$. The differential input voltage is presented as a transient on the gate, $\triangle V_g = V_{\rm ref} - V_{\rm in}$, implemented using an analog multiplexer $M2 - M3$ and controlled by $inSel$ and $\overline{inSel}$ timing signals in Fig. 4. In subthreshold,[1] this gate voltage transition produces a change in source current according to (7). By combining (6) and (7), the input–output characteristic of the sigmoid difference unit is expressed as

$$I_o(t) = I_{\rm sat}(t)\ \sigma\Big(A(\triangle V_g - V_{\rm off}(t))\Big) \tag{9}$$

with the same logistic sigmoid function $\sigma(.)$ and scale factor A as for the MOS differential pair in subthreshold (1), but with time-varying voltage offset and current amplitude

$$V_{\rm off}(t) = -\frac{V_t}{\kappa}\log\frac{I_o(0^-)\,t}{CV_t} \approx -\frac{V_t}{\kappa}\log\frac{t}{\triangle t_1} \tag{10}$$

$$I_{\rm sat}(t) = \frac{CV_t}{t} \tag{11}$$

where the time origin $t = 0$ is taken at the onset of $inSel$ (Fig. 4).

The time dependence of offset and amplitude is inconsequential to the folding characteristic, as time is in common to all σ-cells, and all currents are collected and integrated over the same time window, $\triangle t_3$ (*INT*) in Fig. 4. Note that, by virtue of correlated double sampling in the differential transient $\triangle V_g$ by switching $M2 - M3$, the offset $V_{\rm off}(t)$ is independent of $M1$ threshold variations and, to first order, $1/f$ noise. If desired, the residual uniform (systematic) offset can be eliminated by controlling the timing of $\triangle t_2$ and $\triangle t_3$ relative to $\triangle t_1$. In particular, at the onset of the *INT* integration interval ($t = \triangle t_2$), the voltage offset (10) reduces to zero when $\triangle t_2$ equals $\triangle t_1$.[2]

Fig. 5 illustrates the theoretical and simulated input–output characteristics of the σ-unit for different time intervals $\triangle t_2$ after switching the inputs. Fig. 6 depicts transients in output current I_o for different values of $\triangle V_g$.

[1]For large values of $\triangle V_g$, the nMOS may initially enter the strong inversion region. This affects the timing but not the operation of the circuit, since once V_s has raised to reach the subthreshold the asymptotic relationship (8) holds again.

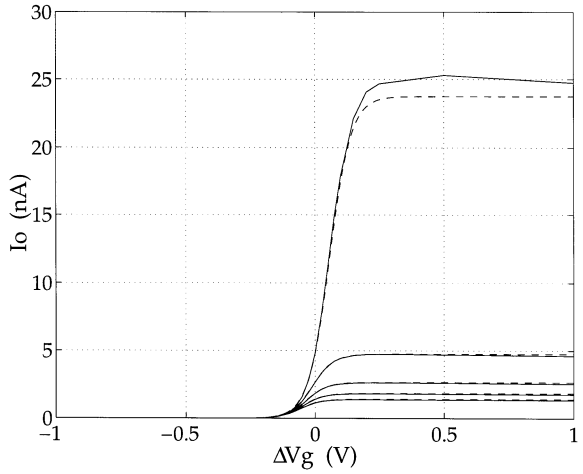

Fig. 5. The input–output characteristics of the MOS-C σ-unit at different fixed time intervals $\triangle t_2$ after onset of *inSel*, calculated using (9) (dashed line) and simulated using SpectreS for a 0.5-μm CMOS process (solid line). Top to bottom: $\triangle t_2$ =50, 250, 450, 650, and 850 ns.

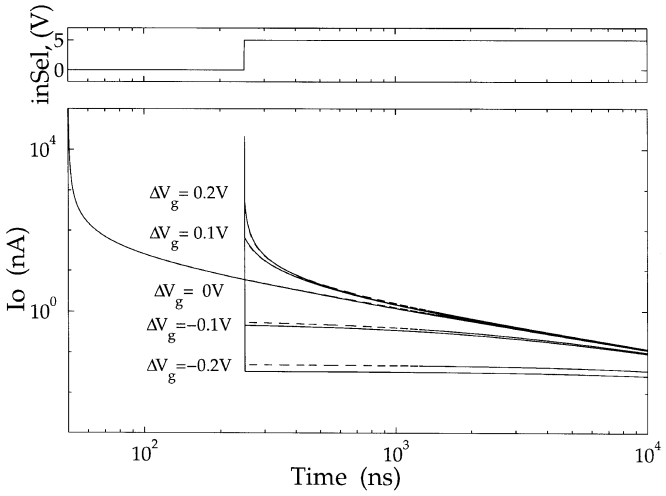

Fig. 6. Differential sigmoid output current transients for different values of $\triangle V_g$. The solid line shows the SpectreS simulation results for a 0.5-μm CMOS process; the dashed line was obtained using (9). The initial current $I_o(0^-)$ = 6 nA. The effective nMOS capacitor value is 45 fF.

[2]This choice results in zero offset for folding ADC operation, assuming that the thresholding comparison of the folding output takes place primarily at the onset of the *INT* interval through a regenerative amplification process as described in Section III-B. In the interpolative mode of folding ADC operation, the folding current is integrated over the entire $\triangle t_3$ interval of *INT* resulting in a broadened sigmoid with input-referred voltage offset $V_{\rm off} = -V_t/\kappa \log(\triangle t_2/\triangle t_1\ \sqrt{1 + \triangle t_3/\triangle t_2})$, which reduces to zero for $\triangle t_3 = \triangle t_1{}^2/\triangle t_2 - \triangle t_2$.

III. MOS-C Folding Circuit and Gray-Coded Folding ADC

A dynamic Gray-coded folding ADC is realized by constructing folding circuits consisting of σ units just described. Folding circuits and comparators in the architecture of Fig. 1(a) combine to produce the Gray-coded output bits shown in Fig. 1(b). The folding currents could, in principle, be integrated for continued interpolating conversion to further increase resolution. For brevity in the present exposition, the interpolating functionality of the folding architecture for multistage ADC operation will not be elaborated on in what follows.

In general, an n-bit folding ADC comprises $2^n - 1$ sigmoid units, arranged in n folding circuits, each folding circuit feeding into a single comparator to generate the Gray-coded bits D_j, $j = 0, \ldots n-1$. An additional sigmoid unit, supplying half the tail current $I_{\rm sat}/2$, is needed in each folding circuit (n total) as a reference bias in the comparison.

A. MOS-C Folding Circuit

The σ-units produce output currents

$$I_o^i = I_{\rm sat}(t)\ \sigma\Big(A(V_{\rm ref}^i - V_{\rm in} - V_{\rm off}(t))\Big) \tag{12}$$

with inflection points ${V_{\rm ref}}^i$ equally spaced between ${V_{\rm ref}}^{\rm min}$ and ${V_{\rm ref}}^{\rm max}$, obtained by linearly tapping a resistive line. The reference sigmoid supplying the current $I_{\rm sat}(t)/2$ is identical to the other σ-units but with half the capacitance, $C/2$, and saturated by applying a step in voltage given by the conversion range ${V_{\rm ref}}^{\rm max} - {V_{\rm ref}}^{\rm min}$.

For instance, in a 4-bit ($n = 4$) Gray-code ADC, the LSB ($j = 3$) differential folding output currents contain the following eight sigmoid contributions:

$$I_+^3 = I_{\rm sat} \sum_{i=0}^{3} \sigma\Big(A(V_{\rm ref}^{4i+1} - V_{\rm in} - V_{\rm off})\Big) \tag{13}$$

$$I_-^3 = I_{\rm sat} \sum_{i=0}^{3} \sigma\Big(A(V_{\rm ref}^{4i+3} - V_{\rm in} - V_{\rm off})\Big) + \frac{I_{\rm sat}}{2}. \tag{14}$$

Theoretical and simulated output currents of a 4-bit LSB folding circuit are plotted in Fig. 7 as a function of input voltage. In the actual implementation, two additional σ-cells are used to avoid side effects visible at the lower and higher ends of the conversion interval.

B. Integrating Sense-Amplifying Comparator

Bit decisions are made on integrated, differentially folded σ-unit currents using a correlated double sampling sense-amplifying comparator. As discussed in Section II-B, synchronous and properly chosen timing of control signals eliminates the offset $V_{\rm off}(t)$.

The integrating and latching sense-amplifying comparator is shown in Fig. 8. A cascode stage $M9 - M10$, controlled by the bias voltage $V_{\rm casc}$, provides low impedance input to the sense amplifier to improve the conversion speed and reduce the effect of the output conductance of the σ-cells. Current-domain correlated double sampling is achieved by swapping differential current inputs to the comparator at start of integration using multiplexers $M5-M6$ and $M7-M8$, from precharge to evaluate mode. In precharge mode (time interval $\triangle t_2$ in Fig. 4) capacitors C are precharged through transistors $M3$ and $M4$ to the difference in gate voltages of transistors $M1$ and $M2$ set by currents I_- and I_+ (including mismatch in threshold voltage). In evaluate mode (time interval $\triangle t_3$ in Fig. 4), the multiplexers $M5-M6$ and $M7-M8$ switch the input currents. Positive feedback amplifies the difference in input currents, producing bistable voltage output. The correlated double sampling scheme compensates for comparator input-referred offset and doubles its input dynamic range. An additional comparator stage, not shown, further amplifies the difference $V_{o+} - V_{o-}$ and latches the result.

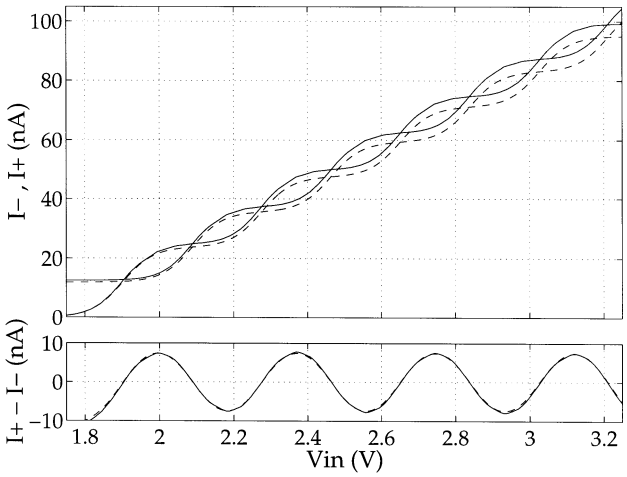

Fig. 7. Output currents of the LSB folding circuit for a 4-bit Gray-code ADC. The solid line represents the SpectreS simulation results for a 0.5-μm CMOS process; the dashed line corresponds to (14) and (13). The time interval $\triangle t_2 =$ 50 ns.

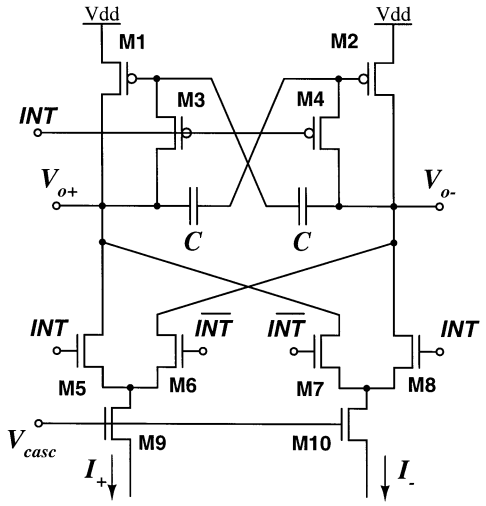

Fig. 8. Integrating sense-amplifying comparator.

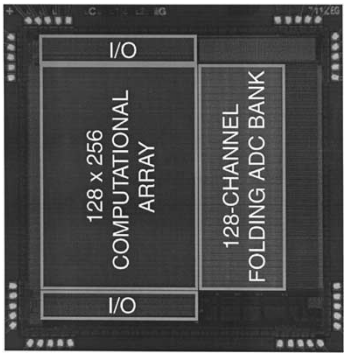

Fig. 9. Micrograph of a mixed-signal processor containing a computational array and a 128-channel parallel bank of 4-bit Gray-code folding ADCs. Die size is 3 mm $\times$ 3 mm in 0.5 μm CMOS technology.

IV. Experimental Results

A prototype 128-channel bank of 4-bit dynamic Gray-codes folding ADCs was fabricated in a 0.5-μm CMOS process. The die micrograph is shown in Fig. 9. The parallel bank of folding ADCs serves to quantize analog outputs from a massively parallel mixed-signal matrix–vector

TABLE I
FOLDING ADC ARRAY CHARACTERISTICS

Technology	0.5 μm 2P3M CMOS
Size	0.7 mm $\times$ 2 mm
Channels	128
Resolution	4 bit
INL / DNL	0.5 LSB / 0.4 LSB
Conversion speed	768 Msps (128 $\times$ 6 Msps)
Power dissipation	82 mW at 5 V

multiplying (MVM) computational array [13]. The ADC bank measures 0.75 mm $\times$ 2 mm, and dissipates 82 mW of power at 6-MHz clock, for a combined conversion rate of 768 Msps (7.68×10^8 samples per second). The portion of the power consumed by the folding circuits (excluding sense amplifiers and output drivers) is 15 mW. The resistor string contributes 1 mW to total power. The measured characteristics are summarized in Table I.

In mixed-signal MVM array processing, multiple results from array-parallel low-resolution folding ADCs are combined in the digital domain to digitize a single output vector component. Parallel use of multiple quantizers allows to boost overall quantization resolution by almost 2 bits beyond the resolution limits of each ADC channel [13], [14] to approximately 6 bits.

V. CONCLUSION

A compact, offset and amplitude-compensated sigmoid differencing and folding circuit has been reported. Each sigmoid difference unit performs correlated double sampling of the inputs to avoid mismatch errors. The circuit operates in weak inversion and offers both high speed and low power. The design is suited for parallel data conversion on mixed-signal computational arrays, active pixel imagers, and other distributed charge or voltage mode circuits. A 128-channel parallel bank of 4-bit Gray-code folding ADCs converters has been implemented in a 0.5-μm CMOS process, delivering 128 $\times$ 6 Msps at 82-mW power dissipation.

The results are meant to illustrate the principle and not to indicate performance limits of the approach. Resolution can be enhanced using interpolation by integrating the folding currents onto capacitors and presenting the resulting differential voltage to subsequent folding stages. Speed is limited mainly by the time required for the MOS-C diode-integrators to enter the subthreshold region. It is straightforward to extend the circuit with BJTs, which attain exponential I–V characteristics at elevated current levels, for higher speed ADCs.

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A Layout Structure for Matching Many Integrated Resistors

J. Paul A. van der Wagt, Gordon G. Chu, and Christine L. Conrad

***Abstract*—A proposed mirrored shuffle layout pattern cancels systematic resistor gradient variations up to second order and allows monolithic integration of hundreds of matched resistors for precision analog circuits. A test circuit uses 15 000 subresistors and three levels of interconnect to form 150 main resistors in a 2.85 $\times$ 0.83 mm^2 area. It demonstrates better than 11-b matching. The dominant remaining error is related to a layout artifact external to the core resistor array, and after separation the resistor array itself achieves over 13-b matching. Wafer maps show significant first- and second-order resistor value gradients that are cancelled to within the measurement error.**

***Index Terms*—Analog-to-digital conversion (ADC), analog integrated circuits, digital-to-analog conversion (DAC), integrated circuit (IC) layout, passive circuits, resistors.**

I. INTRODUCTION

Current steering segmented digital-to-analog converters (DACs) often drive unary digital-to-analog subconverters (DASCs) with thermometer decoded MSB inputs. High-speed bipolar transistor pipelined ADCs use current-mode unary DASCs to reconstruct the MSB subquantizer output. These applications often require more than

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