CMOS Impedance Spectrum Analyzer with Dual-Slope Multiplying ADC

Hamed Mazhab Jafari, Roman Genov
Department of Electrical and Computer Engineering, University of Toronto, Email: {hamed, roman}@eecg.utoronto.ca

***Abstract*—We present a multi-channel, mixed-signal VLSI architecture that utilizes frequency response analysis (FRA) to extract the real and imaginary components of a biosensor impedance. Two computationally intensive operations, the multiplication and integration required by the FRA algorithm, are efficiently performed by an in-channel dual-slope multiplying ADC with minimal resources overhead. Multiplication of the input current by a digital coefficient is implemented by modulating the counter-controlled duration of the charging phase of the ADC. Integration is implemented by accumulating output digital bits in the ADC counter over multiple input samples. The 1.2mm×1.6mm prototype fabricated in a 0.13μm standard CMOS technology has been validated in DNA catalytic reporter detection. Each channel occupies an area of only 0.06mm^2 and consumes 42μW of power from a 1.2V supply.**

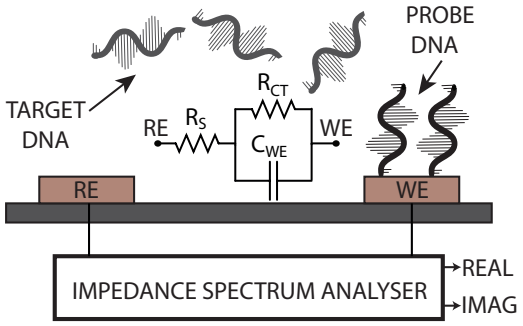


Fig. 1. Conceptual view of a biosensor impedance spectroscopy system.

I. Introduction

Impedance spectroscopy is a popular method of quantitative and qualitative monitoring of the thermodynamics and kinetics of chemical reactions in many biosensors. A wide range of biosensors have been developed which rely on impedance spectroscopy, including sensors based on enzymes, antibodies and DNA [1-4]. Fig. 1 shows the basic principle of electrochemical impedance spectroscopy sensing. An electrochemical cell consists of a working electrode (WE) and a reference electrode (RE). In biochemical sensors, biologically active compounds such as antibodies, enzymes or DNA probes are integrated with the working electrode. The integration process involves the immobilization and stabilization of biological molecules on the electrode surface. For example, in DNA sensing applications, the surface of the working electrode is functionalized with the probe DNA. Binding of the probe DNA with the target DNA results in changes in the working electrode surface properties such as an impedance or a surface charge. An impedance spectrum analyzer extracts the real and imaginary components of the biosensor impedance.

A number of integrated impedance spectroscopy microsystems have been reported [5]-[7]. The design in [5] is a single-channel impedance extractor based on a lock-in amplifier that extracts the sensor impedance from 1Hz to 10kHz. The implementation in [6] is a 100-channel impedance-to-digital converter based on a delta-sigma modulator capable of extracting sensor impedance from 1mHz to 10kHz at the cost of a long conversion cycle. A direct conversion receiver without an on-chip ADC [7] extracts the electrode impedance from 10Hz to 50MHz at the cost of consuming 104mW of power.

This paper presents a scalable, multi-channel, compact and low-power impedance spectroscopy VLSI architecture for biochemical sensing applications. Frequency response analysis (FRA) algorithm is utilized to extract the real and imaginary components of the biosensor impedance [5]. The proposed microsystem consists of a programable on-chip signal generator and 16 impedance extraction channels. Each channel includes a current-mode input dual-slope multiplying ADC. It efficiently performs multiplication and integration, two computationally intensive operations required to implement the FRA algorithm. Multiplication of the input current by a digital coefficient is implemented by modulating the counter-controlled duration of the charging phase of the ADC by that coefficient. Integration is implemented by accumulating the output digital bits in the ADC counter. The dual-slope multiplying ADC utilizes mostly the same circuits as a conventional dual-slope ADC, and the multiplication and integration are achieved by modifying the ADC algorithm.

II. Impedance Spectroscopy Implementation

A small-signal model of the electrode-electrolyte interface in an electrochemical cell is shown in the center of Fig. 1. In this model R_S represents the resistance between the working and reference electrodes, C_{WE} represents the interfacial double-layer capacitance at the WE-electrolyte interface and R_{CT} models the charge transfer resistance at the WE-electrolyte interface [3]. Fast fourier transform (FFT) and frequency-response analyzer (FRA) are two methods widely used for characterizing the electrode impedance [8]. Compared to the FFT, the FRA method requires simple circuitry and can be implemented on a small silicon area, making it suitable for sensory array microsystems. A functional block diagram of the FRA algorithm is shown in Fig. 2. The sensor is interrogated with a sinusoidal voltage. Multiplication of the

978-1-4577-1470-2/11/$26.00 ©2011 IEEE

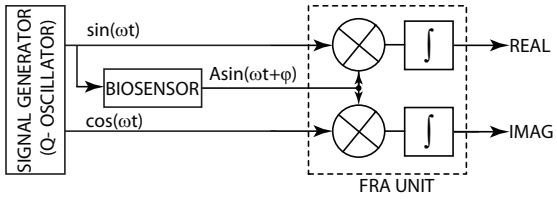


Fig. 2. Block diagram of a frequency-response analyzer (FRA) system for biosensor impedance spectroscopy.

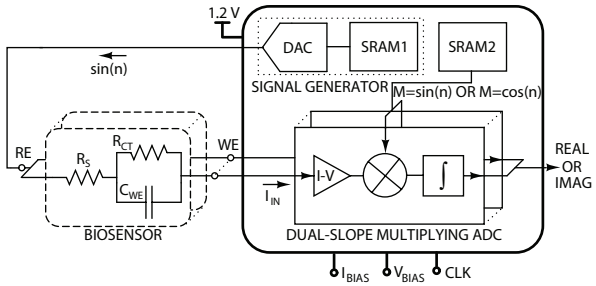


Fig. 3. Impedance spectroscopy microsytem functional block diagram.

sensor response *Asin(ωt+φ)* with *sin(ωt)* or *cos(ωt)* results in separation of real and imaginary components of the sensor impedance and additional high frequency components which are removed using an integrator [5].

In this work the FRA algorithm has been chosen to implement a sensory array impedance spectroscopy microsystem. The two key components in this system are the multiplier and the integrator. Both of these operations are implemented with an in-channel multiplying dual-slope ADC that reuses the circuits of a conventional dual-slope ADC.

III. VLSI Architecture

A. Multi-channel System-Level Architecture

The functional block diagram of the impedance spectroscopy microsystem based on the FRA algorithm is shown in Fig. 3. The microsystem is comprised of a signal generator, an extra SRAM2 block and an array of impedance extraction units. The signal generator produces the interrogation waveform *sin(ωt)* and drives the reference electrode with it. The signal generator coefficients are stored in an on-chip SRAM1. Each impedance extraction unit consists of a dual-slope multiplying ADC (DS-MADC). It acquires an input current at the low-impedance input node set to a controlled potential. The DS-MADC multiplies the biosensor response I_{IN} with the digital coefficient *M* representing *sin(ωt)* or *cos(ωt)* that are synchronized with the interrogation voltage on the reference electrode. Next the DS-MADC integrates the results over one period of the interrogation signal, thus extracting the real or the imaginary components of the biosensor impedance.

The frequency response analysis implementation is the simplest when rectangular waveforms are used instead of sine wave for both the interrogation and the multiplication signals. The problem is that severe systematic errors appear due to the higher order harmonics existing in the rectangular waveforms. Stepwise approximation of the interrogation waveform and the multiplication signals reduces the effect of higher order harmonics and increases the measurement accuracy. It has been shown [5] that representing both the interrogation signal and the multiplication signals by a coarsely quantized approximation can significantly reduces the error due to the higher order harmonics and reduce the measurement inaccuracy to below 0.1 percent.

In this work an 8-bit R-2R DAC is utilized to generate the stepwise approximation of the interrogation signal. The DAC occupies an area of 0.012mm^2 and dissipates 1.1mW of power from a 1.2V supply when driving a load of 5nF at 50KS/s. At low frequencies the interrogation sine wave is represented by 64 samples. The DAC coefficients for the first 16 samples of the signal generator waveform and for the corresponding sin/cos multiplication coefficients are stored in two on-chip global SRAM banks. The SRAMs occupy an area of 0.028mm^2 and dissipates 0.9μW of power when clocked at 50kHz. By symmetry, 64 data points in one period are generated from the 16 samples stored on-chip. As the interrogation frequency increases, the number of samples representing the interrogation and multiplication signals decreases and at 10kHz both signals are represented by three samples. This greatly reduces the ADC speed requirement while the error caused by the reduction in number of samples is kept low by averaging the results over multiple cycles.

B. Dual-slope Multiplying ADC Channel

The VLSI architecture of one channel of the integrated spectrum analyzer is depicted Fig. 4. Each channel consists of an integrating amplifier with an on-chip 10pF capacitor C_F, a high-speed latched comparator and digital blocks. The integrator switches are implemented with low-leakage switches as shown.

The conventional dual-slope ADC operates in two phases as depicted in Fig. 4(b). In phase I the integrating capacitor C_F is charged for a predetermined period of time T_1. Next, during the second phase of the operation, the capacitor is discharged to zero by a DC reference current. By counting the time T_2, a digital representation of I_{IN} can thus be obtained as $(T_2/T_1)\times I_{REF}$. To implement multiplication of the input current by a digital sin/cos coefficient as needed by the FRA algorithm, the duration of phase I is scaled with a constant coefficient $M<1$ as shown in Fig. 4(b). In this case by counting the time MT_2, a digital representation of MI_{IN} can be obtained as $M\times(T_2/T_1)\times I_{REF}$. To extract the real and imaginary components of the biosensor impedance, the input current I_{IN} is multiplied by the reference sine or cosine coefficient denoted as *M* (stored in SRAM2) and the results are integrated over one period by a 16-bit counter.

The timing diagram of the ADC for a typical conversion cycle is shown in Fig. 4(c). First, the integrating counter is reset. At the same time, the sin/cos multiplication coefficient, *M*, is loaded into the in-channel input latch (time A). Next, the in-channel counter counts up from zero to time MT_1

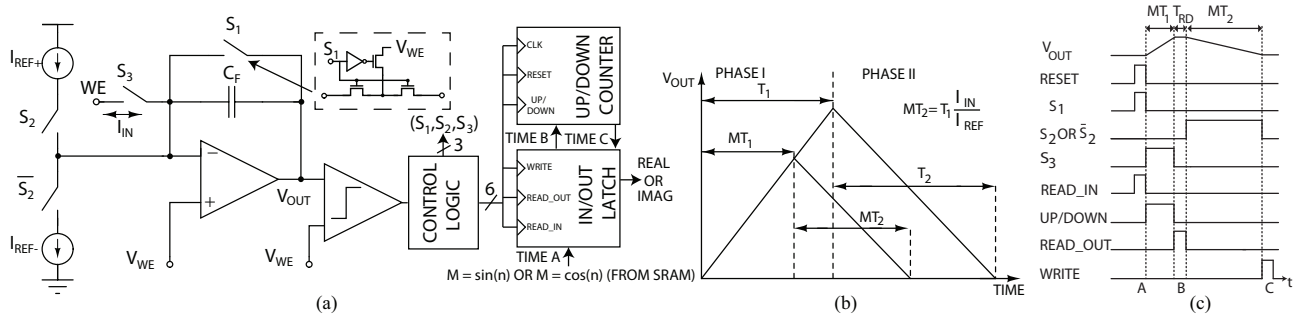
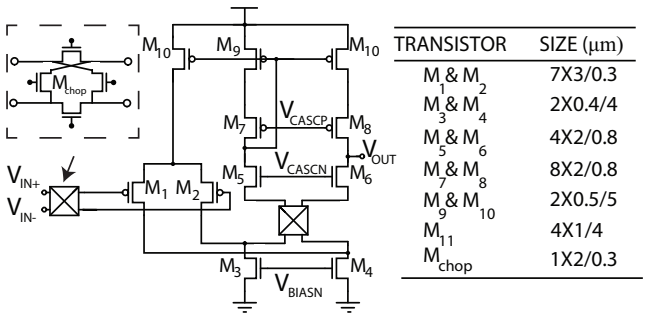


Fig. 4. (a) Dual-slope multiplying ADC VLSI architecture, (b) timing diagram illustrating the multiplication function, and (c) timing diagram of all relevant signals.



TRANSISTOR	SIZE (μm)
M_1 & M_2	7X3/0.3
M_3 & M_4	2X0.4/4
M_5 & M_6	4X2/0.8
M_7 & M_8	8X2/0.8
M_9 & M_{10}	2X0.5/5
M_{11}	4X1/4
M_{chop}	1X2/0.3

Fig. 5. Folded-cascode OTA in the analog integrator.

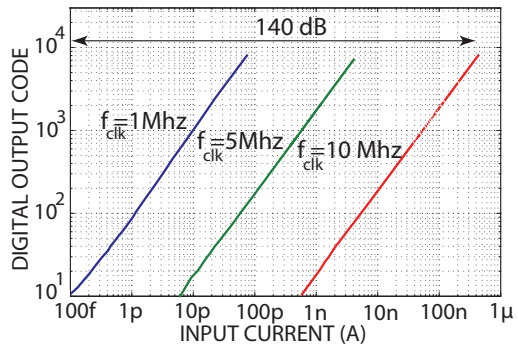


Fig. 6. Experimentally measured transfer characteristics of the impedance spectrum analyzer channel for three sampling frequencies.

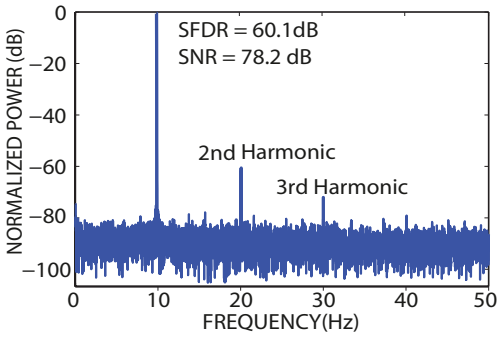


Fig. 7. Output spectrum of the ADC for a 10Hz sinusoidal input.

and the input current is integrated onto capacitor C_F. After time MT_1, the voltage on the capacitor is held constant for a fixed time interval T_{RD}. During this time the content of the output latch (zero for the first conversion cycle) is loaded into the counter (time B). During time MT_2, depending on the comparator output, the integrating capacitor is discharged using the appropriate current source, I_{REF+} or I_{REF-}. During time MT_2 the counter counts up or down depending on the sign of the input current in phase I and the final value of the counter is written into the output latch (time C). This part of the ADC conversion cycle performs the summation which implements integration required by the FRA algorithm. This process is repeated for one full cycle of the sinusoidal stimulation waveform and the final value stored in the output latch corresponds to the real or imaginary component of the biosensor impedance, for sin and cos multipliers respectively.

The analog integrator amplifier is a folded-cascode transconductance amplifier consuming 6μW from a 1.2V supply as shown in Fig. 5. Since the impedance spectroscopy frequency range is typically from 1Hz to a few kHz, the amplifier utilizes input PMOS devices with a wide aspect ratio and internal chopping to reduce the effect of the flicker noise. The comparator is implemented with three pre-amplifier stages, with a total gain of 60dB, and a high-speed output latch. The comparator is verified in simulation to operate correctly up to 40MHz. The channel consumes 42μW of power from a 1.2V power supply when clocked at 10MHz.

IV. EXPERIMENTAL RESULTS

The 16-channel 1.2×1.6 mm^2 integrated impedance spectrum analyzer prototype was implemented in a 0.13μm CMOS process with a 1.2 V supply. Each channel consists of a square electrolessly plated Au WE with side length of 55μm. Each column of four working electrodes shares a 45μm-wide Au RE electrode driven by the on-chip signal generator.

The digital output of one channel for the input current swept between 100fA and 400nA is shown in Fig. 6. The input dynamic range is 140dB cumulatively for the three sampling frequency settings, or 65.9dB at 1MHz clock. Dynamic per-

TABLE I
EXPERIMENTALLY MEASURED CHARACTERISTICS

Technology	0.13μm CMOS
Supply Voltage	1.2V
Area	1.2mm×1.6mm
Array Dimensions	4×4 channels
Channel Size	300μm×200μm
Sensitivity	100fA
Channel SNR (fclk=1MHz)	78.2 dB
Channel SFDR (fclk=1MHz)	60.1 dB
Power Consumption	
DAC	1.1 mW
SRAM	1.3μW
Current conveyer	8μW
Comparator	19μW
Biasing	4μW
Digital	11μW
Total (channel)	42μW

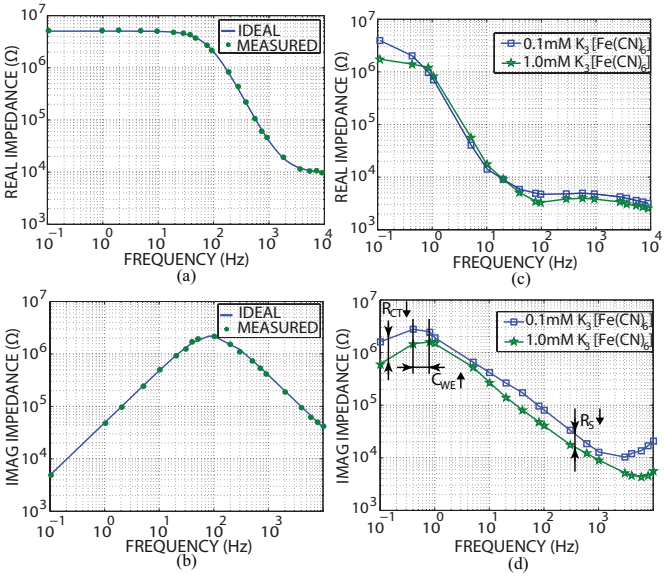


Fig. 8. Biosensor impedance as a function of frequency experimentally measured by the impedance spectroscopy microsystem: (a) real, and (b) imaginary component of the off-chip biosensor model; (c) real, and (d) imaginary component of the potassium ferricyanide solution.

formance of an entire channel was measured by applying a 10Hz full scale (300nA) sinusoidal input current with the ADC clocked at 10MHz. Fig. 7 shows the 65536-point FFT of the measured ADC output. The strong second harmonic is due to the single-ended architecture of the ADC. The resulting effective number of bits (ENOB) is 9.3. Table I provides a summary of experimentally measured characteristics of the integrated impedance spectroscopy microsystem.

The electrode model shown in Fig. 1 was used to emulate the biosensor. R_S value was set to 10kΩ, C_{WE} was set to 400pF and R_{CT} was set to 4.4MΩ. To verify the impedance extraction capability of the microsystem, a sinusoidal voltage stimulus (generated by the on-chip DAC) with the frequency swept from 0.1Hz to 10kHz was applied to the biosensor model. Fig. 8 (a) and (b) demonstrate that the fabricated prototype tracks the theoretical model well over the full range of frequencies.

Potassium ferricyanide $K_3[Fe(CN)_6]$ is widely used in electrochemical DNA detection systems. Impedance spectroscopy recordings of 0.1mM and 1mM potassium ferricyanide in 1 M potassium phosphate buffer (pH 7.3) have been carried out. A 9mV 0.1 to 10kHz sin wave was applied between the WEs and an off-chip Ag-AgCl reference electrode. The real and imaginary impedance results obtained from the two concentrations of the potassium ferricyanide solution are shown in Fig. 8 (c) and (d). An increase in the concentration of the potassium ferricyanide results in a decrease in value of R_S and R_{CT} and increase in value of C_{WE}. The measurement of potassium ferricyanide validate impedance spectroscopy microsystem in DNA sensing applications.

V. CONCLUSIONS

A multi-channel, mixed-signal CMOS impedance spectroscopy VLSI architecture is presented. It consists of a programable signal generator, on-chip memory and multiple impedance extraction units. Multiplication and integration, two operations required for frequency response analysis (FRA) algorithm, are efficiently performed by the in-channel current-mode input dual-slope multiplying ADC with negligible resource overhead. The ADC combines impedance extraction and analog-to-digital conversion into a single conversion cycle. The impedance spectroscopy microsystem with 16 channels was implemented in a CMOS 0.13μm technology. Each channel occupies an area of 0.06mm^2 and consumes 42μW of power from a 1.2V supply.

REFERENCES

[1] F. Heer, M. Keller, G. Yu, J. Janata, M. Josowicz, A. Hierlemann, "CMOS Electro-Chemical DNA-Detection Array with On-Chip ADC," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, pp. 168-169, 2008.

[2] M. Schienle, C. Paulus, A. Frey, F. Hofmann, B. Holzapfl, P. S. Bauer, and R. Thewes, "A fully electronic DNA sensor with 128 positions and in-pixel A/D conversion," *IEEE J. Solid-State Circuits,* vol. 39, no.12, pp. 2438-2445, 2004.

[3] P. M. Levine, P. Gong, R. Levicky, K.L. Shepard, "Active CMOS Sensor Array for Electrochemical Biomolecular Detection," *IEEE J. Solid-State Circuits,* vol. 43, no. 8, pp. 1859-1871, 2008.

[4] A. Hassibi and T. H. Lee, "A Programmable 0.18μm CMOS Electrochemical Sensor Microarray for Bimolecular Detection," *IEEE Sensors Journal*, vol. 6, pp. 1380-1388, 2006.

[5] M. Min and T. Parve, "Improvement of lock-in bio-impedance analyzer for implantable medical devices," *IEEE Trans. Instrum. Meas*., vol. 56, pp. 968-974, 2007.

[6] A. Yang, S. R. Jadhav, R. M. Worden, and A. J. Mason, "Compact low-power impedance-to-digital converter for sensor array microsystems," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2844-2855, 2009.

[7] A. Manickam, A. Chevalier, M. McDermortt, A. D. Ellington, A. Hassibi, "A CMOS Electrochemical Impedance Spectroscopy Biosensor Array for Label-Free Biomolecular Detection," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, pp. 130-131, 2010.

[8] E. Barsoukov, J. R. Macdonald, Impedance Spectroscopy: Theory, Experiment, and Applications, 2nd ed., John Wiley, Hoboken, NJ, 2005.