Compact Chopper-Stabilized Neural Amplifier with Low-Distortion High-Pass Filter in 0.13μm CMOS

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***Abstract*— A compact and low-distortion neural recording amplifier is presented. The amplifier consists of two stages of amplification using capacitive feedback to set a gain of 54dB. To minimize flicker noise in the 1st stage, internal chopping is utilized at the folded node of the OTA, resulting in flicker noise contribution from the input differential pair only. A low-distortion constant-V_{GS} feedback circuit to set a low frequency high-pass pole is introduced. It is less sensitive to the output swing than the conventional sub-threshold MOS circuit. The amplifier fabricated in a standard 1.2V 0.13μm CMOS technology occupies 125x175μm^2 and achieves an NEF of 4.4, an input-referred noise of 4.7μV over a 5kHz bandwidth, a CMRR of 75dB and a THD of -50dB for a 0.6V output swing.**

I. Introduction

The highly dense organization of neurons in biological tissue requires a large number of electrodes to obtain an accurate representation of neural activity. State-of-the-art implantable electrode arrays consist of 64 or more electrodes, either implantable multielectrode arrays (MEA) or electrocorticography (ECoG) grids. To interface with such electrode arrays while enabling simultaneous recording from all channels requires a large number of low-noise neural recording front-end amplifiers. This drives up the area and power budget of a neural recording system-on-chip (SoC). Thus, for dense, high channel count implantable SoC implementations with on-chip signal processing and RF circuitry a fully differential architecture with minimized area and power dissipation is critical.

State-of-the-art neural recording amplifiers utilizing chopper stabilization to reduce flicker noise have been demonstrated for scalpf EEG applications [1], [2], [3]. These designs require large capacitors and DC-servo loops to enable chopping while maintaining a low-frequency high-pass pole resulting in large silicon area or large off-chip passives. These designs also do not cover higher frequencies required to record neural spikes. Neural recording amplifiers without chopper stabilization for dense neural recording arrays have been demonstrated [4], [5], [6] and [7]. These designs require large devices in the OTA to minimize flicker noise. As well, these capacitive feedback designs utilize a high resistance device to create a low-frequency high-pass pole that is sensitive to the output swing resulting in distortion at low frequencies as well as variations due to fabrication process.

Two techniques for improving the area and linearity of compact neural recording amplifiers are demonstrated in this paper. The first is to introduce chopping inside the front-end OTA to reduce the overall flicker noise without enlarging the area of all transistors except for the input pair. The second is to use a modified feedback element which helps ensure high linearity at low frequencies for large output swings. Adding tunability to the high-pass pole enables calibration for process variation or adjusting the bandwidth for filtering of different neural signals. We present a neural recording design that minimizes the integration area allowing for a large-scale multi-channel low-power neural recording array VLSI implementation. The rest of the paper is organized as follows. Section II discusses the neural recording architecture. Section III discusses the VLSI implementation. Section IV contains results of experimental characterization of the presented neural recording amplifier.

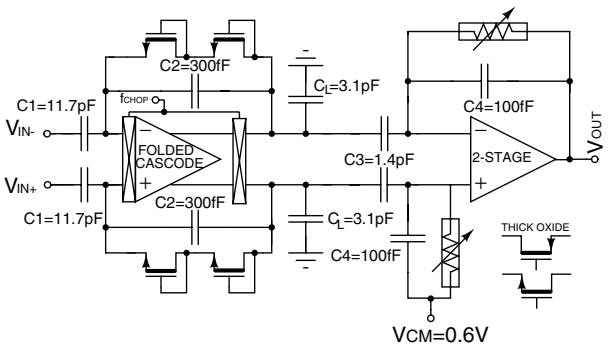

Fig. 1. Architecture of neural recording amplifier.

II. Neural Recording VLSI Architecture

The neural recording amplifier operates from a 1.2V supply and is implemented in a standard 0.13μm CMOS technology. The architecture is shown in Figure 1. With neural signal levels between 10μV and 1.2mV and a frequency range between 1Hz and 5kHz, an output swing of 0.6V and an input-referred noise of below 5μV were targeted. The 1st stage requires high CMRR, low noise and low power dissipation. The 2nd stage requires low power dissipation and high linearity. A gain of 500V/V is set by the two stages of capacitive feedback amplifiers utilizing dense dual MIM capacitors. The 1st stage has a maximum output swing of below 50mV and thus, utilizes a fully differential chopper-stabilized folded-cascode OTA with two MOS-bipolar pseudo-resistive feedback devices in series to set the low-frequency high-pass pole. The 2nd

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stage requires output swings of up to 0.6V and uses a 2-stage OTA and an improved tuneable feedback element to achieve a constant resistance and tunability of the high-pass pole.

III. VLSI IMPLEMENTATION

The main novel components of the neural recording amplifier are the 1st stage fully-differential chopper-stabilized folded-cascode OTA and the 2nd stage tunable feedback element.

A. Chopper-stabilized OTA

The first stage utilizes a fully differential folded-cascode OTA with 60dB gain as shown in Figure 2(a). To minimize flicker noise of devices M3/M4 and M5/M6 chopping was placed at the folded node. Placing chopping in front of the input pair as is done conventionally would have resulted in noise multiplication due to a switched capacitor created by the parasitic capacitance of the input pair. This can be alleviated by using very large input capacitors (>100pF) at the expense of area. The low impedance at the folded-cascode node, allows for high frequency chopping (>100kHz) which is filtered out by the bandpass filter of the 2nd stage. To minimize flicker noise of the input pair (M1/M2), large PMOS devices were selected. To minimize thermal noise transistors they were biased in sub-threshold to maximize their g_m. Transistors M3/M4 and M5/M6 were biased in saturation to minimize their g_m. Common-mode feedback (CMFB) is implemented by modulating the tail current of the 1st stage of folded-casocode OTA using a continuous-time CMFB amplifier. The OTA requires a total of 2.4μA which includes 1.6μA into the input pair, and 0.8μA into the cascode transistors. Transistor sizing for the chopper-stabilized OTA is shown in Table I with all transistors utilizing standard thin oxide.

When chopping is disabled, 30 percent of the total input-referred integrated noise from 10Hz to 5kHz is contributed from the flicker noise of M3 and M4 as shown in Table II. With chopping enabled, the majority of the total input-referred integrated noise is contributed from thermal noise with all flicker noise contributed from the input-pair. This design allocates 25 percent of the total noise contribution to the flicker noise of the input-pair noise and can further be reduced by increasing the area of the input devices at the expense of silicon area. At low frequencies (below 10Hz) the thermal noise contribution from the feedback resistor begins to dominate.

The 2nd stage OTA requires high output swing and thus is implemented using a 2-stage OTA. The singled-ended OTA has 60dB of gain and utilizes PMOS input devices. A total of 350nA is utilized by the OTA, with 100nA in the input stage and 250nA in the 2nd stage.

B. High-pass Feedback Element

The 1st stage utilizes two diode connected MOSFETs which implement two MOS-bipolar pseudo-resistive devices [5]. At low-output swings this resistance is relatively constant. To make this device tuneable, the gate can be connected to a bias voltage and its $|V_{GS}|$ can be modified to adjust the resistance

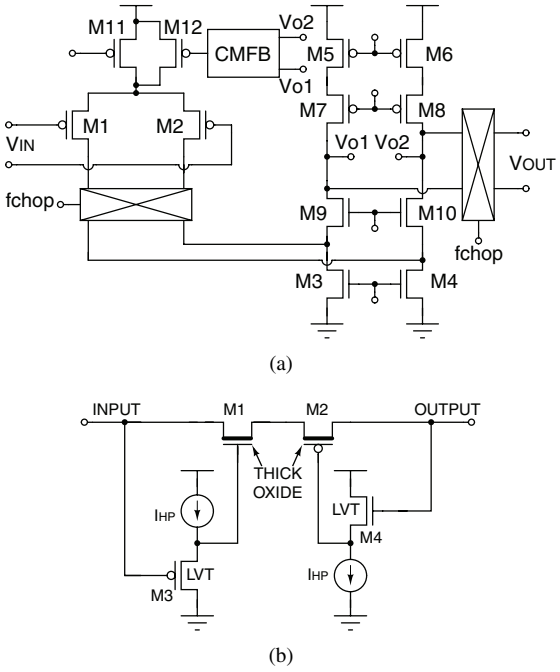

Fig. 2. (a) Schematic diagram of the internally chopper-stabilized folded-cascode OTA. (b) Schematic diagram of the low-distortion high-resistance feedback element.

TABLE I
OTA TRANSISTOR SIZES.

Transistor	W/L (μm)
$M_{1,2}$	$25 \times 2/1.5$
$M_{3,4}$	$4 \times 0.5/15$
$M_{5,6}$	$4 \times 1/10$
$M_{7,8}$	$4 \times 0.6/1$
$M_{9,10}$	$4 \times 0.6/1$
M_{11}	$4 \times 1/2$
M_{12}	$1 \times 1/2$

[6]. At large output swings, the $|V_{GS}|$ of the feedback element changes resulting in a varying resistance leading to non-linearities at low frequencies. Also, setting the $|V_{GS}|$ too low results in DC bias drifts.

In the 2nd stage, to ensure a more constant $|V_{GS}|$ as the output swings and to allow for tunability, two source followers act as floating DC voltage sources to track the changing output as shown in Figure 2(b). The resistance can be reduced by increasing the current in the source followers and thus increasing the $|V_{GS}|$ of the MOS devices. To minimize area, low-threshold devices were used to ensure $|V_{GS}|$ tunability between approximately below 0.1 and 0.3V. Utilizing both NMOS and PMOS ensures at least one device has the proper $|V_{GS}|$ to implement a large resistance at the extreme output levels (0.3 and 0.9V). Additionally, comparing to the conventional approach, this feedback resistance achieves more accurate biasing by ensuring a controlled resistance in the feedback.

Transistor sizing for the tuneable resistor are shown in

TABLE II

SUMMARY OF SIMULATED NOISE

DEVICE (CHOPPER OFF)	NOISE SOURCE	CONTRIBUTION (%)
M3/M4	Flicker	30.4
M1/M2	Thermal	25.2
M1/M2	Flicker	16.2
M3/M4	Thermal	8.1
M5/M6	Thermal	6
DEVICE (CHOPPER ON)	**NOISE SOURCE**	**CONTRIBUTION (%)**
M1/M2	Thermal	38.6
M1/M2	Flicker	24.6
M3/M4	Thermal	19.0
M5/M6	Thermal	9.0

TABLE III

TRANSISTOR SIZES OF THE FEEDBACK ELEMENT.

Transistor	W/L (μm)
M_1	$1 \times 0.5/15$
M_2	$1 \times 0.5/15$
M_3	$2 \times 2.5/0.5$
M_4	$3 \times 1.0/0.5$

Table III. The NMOS and PMOS feedback devices are implemented using thick oxide and the source followers are implemented using low-threshold thin-oxide devices. The high leakage of thin oxide devices in this process yields a resistance that is too low to obtain a sub-Hz high-pass frequency pole.

IV. EXPERIMENTAL RESULTS

The neural recording amplifier was fabricated in a standard 1-poly, 8-metal, 1.2V, 0.13μm CMOS process. The micrograph of the amplifier is shown in Figure 3. It occupies an area of 175μm $\times$ 125μm. The majority of the area is utilized by the 1st stage closed-loop amplifier.

A. Gain and Noise

The experimentally measured frequency response and input-referred noise are shown in Figure 4. The gain is approximately 54dB between sub-1Hz to 5kHz. The input-referred noise between 10Hz and 5kHz is 4.7μV_{rms}, and between 1Hz and 100Hz is 3.7μV_{rms}. The NEF of the fully differential neural recording amplifier for a 5kHz bandwidth is 4.4.

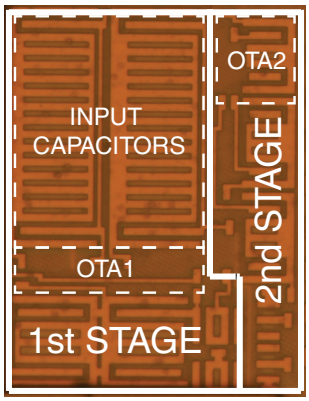

Fig. 3. Micrograph of the neural recording amplifier with dimensions of 175μm by 125μm in 0.13μm CMOS.

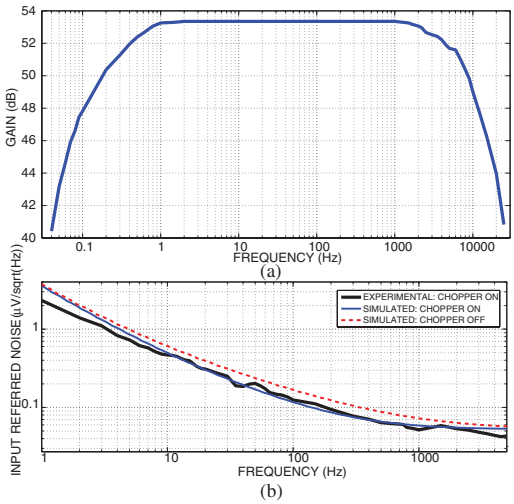

Fig. 4. (a) Experimentally measured frequency response. (b) Experimentally measured noise.

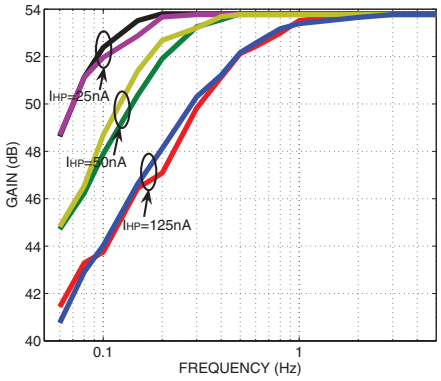

Fig. 5. Experimentally measured high-pass filter frequency response for three different values of I_{HP} on two different channels on the chip.

Tunability of the high-pass pole is shown in Figure 5 for two different neural recording amplifiers on the chip. The source follower current, I_{HP}, was set to 25nA, 50nA and 125nA. The 3dB high-pass cutoff frequencies between the two channels are close to each other. Setting the source follower current to 25nA and 1μA yields a highpass pole of 0.05Hz and 10Hz, respectively. The low-pass pole can also be tuned by changing the bias current in the OTAs. The experimentally measured CMRR at 10Hz and 1kHz is 75.4dB and 71.5dB, respectively.

The output waveforms for a 1mV$_{pk-pk}$ 20Hz sinusoid and a 20μV_{pk-pk} 20Hz sinusoid input are shown in Figures 6(a) and (b), respectively. For the 1mV$_{pk-pk}$ input (0.5V output), the distortion is not visible with the THD being -50dB. Figures 6(b) displays the output for a low-SNR signal of 20μV_{pk-pk}. It depicts the amplifier noise and high frequency ripple due to the chopper switching.

B. Linearity

The THD at full output swing was measured for the proposed feedback element and for the conventional feedback

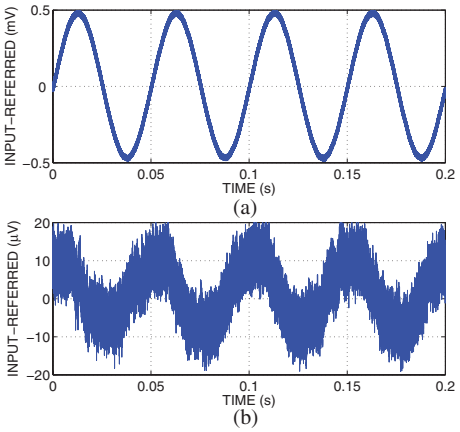

Fig. 6. Experimentally measured output waveforms for (a) a 20Hz 1mV$_{pk-pk}$ input and (b) a 20Hz 20μV_{pk-pk} input.

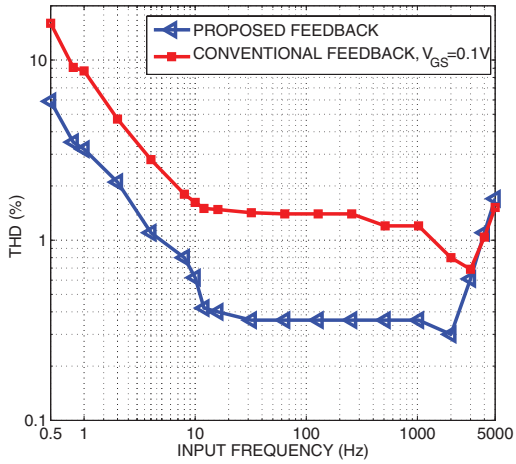

Fig. 7. Experimentally measured THD in percent at full output swing (0.6V) comparing the proposed and conventional tuneable feedback elements.

element with V_{GS} set to 0.1V as needed to obtain the same AC high-pass pole frequency. A comparison between the conventional and proposed feedback element at 0.6V output swing is shown in Figure 7. The proposed feedback element yielded up to 14dB improvement in linearity. This linearity improvement is also visible in the time domain as shown in Figure 8. Figure 8(a) shows the distorted output of the conventional circuit at 1Hz. The less distorted output of the neural amplifier with the proposed feedback element is shown in Figure 8(b). A comparison to recently reported neural recording amplifiers is given in Table IV.

V. Conclusions

A 0.13μm CMOS compact neural recording amplifier with low noise and high linearity is demonstrated. Experimental measurements yield an NEF, CMRR and power dissipation of 4.4, 75dB and 3.8μW, respectively, for the fully differential amplifier operating from a 1.2V supply. The amplifier utilizes 0.022mm^2 of silicon area making it suitable for dense neural recording SoCs.

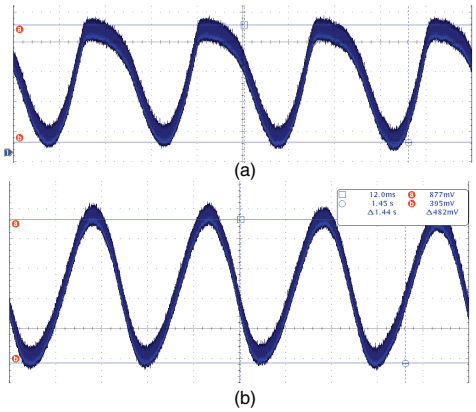

Fig. 8. Experimentally measured output waveforms for a 1mV$_{pk-pk}$ 1Hz sinusoid input comparing (a) conventional and (b) proposed feedback elements performance.

TABLE IV
Comparison Neural Recording Amplifiers

Spec.	[5]	[6]	[8]	[9]	THIS WORK
Power Diss.	42.2μW	43μW	15μW	5.04μW	3.8μW
Tech.	0.5μm	0.13μm	0.35μm	0.065μm	0.13μm
Supply (V)	3.3	1.2	3.3	0.5	1.2
Area (mm^2)	0.16	0.2	0.04	0.013	0.022
CMRR (dB)	-	-	-	75	75.4
Noise (LFP)	5.1	14μV	7μV	4.3μV	3.7μV
Noise (Spike)	-	2.2μV	-	4.9μV	4.7μV
NEF	5.1	5.0	4.6	6	4.4
Fully Integrated	YES	YES	YES	NO	YES

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