

CMOS Tunable-Color Image Sensor With Dual-ADC Shot-Noise-Aware Dynamic Range Extension

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Abstract—A wide dynamic range CMOS tunable-color image sensor is presented. The sensor integrates an 8x8 array of tunable-color photogates which exploit the wavelength-dependent optical absorption properties of the polysilicon gate structure. An analysis is presented for the wide dynamic range asynchronous self-reset with residue readout architecture where photon shot noise is taken into consideration. An implementation of this architecture is presented where the (coarse) asynchronous self-reset operation and (fine) residue analog-to-digital conversions are performed with separate in-pixel and off-pixel circuits, respectively, for a noise-optimized design. A prototype was fabricated in a standard 0.35 μm CMOS process and is validated in color light sensing which achieves SNRs of 24.3 dB and 28.5 dB in green and red light measurements, respectively, under a moderate input light intensity of 300 $\mu\text{W}/\text{cm}^2$. The readout circuit achieves a measured dynamic range of 82 dB with a peak SNR of 46.2 dB under broadband illumination. The prototype has been integrated with a microfluidic device and experimentally validated in fluorescence contact imaging.

Index Terms—CMOS image sensor, fluorescence imaging, lab-on-a-chip, microfluidics, quantum dot, self-reset, subranging architecture, two-step ADC, wide dynamic range.

I. INTRODUCTION

FLUORESCENCE-BASED transduction is an established technology and finds a multitude of applications in the life sciences. For many analytes, it provides the highest sensitivity and selectivity from common transduction methods [1]. In particular, laser-induced fluorescence is a prominent sensory method for lab-on-a-chip devices, depicted in Fig. 1 [2]. Several groups have focused on the development of integrated fluorescence-based sensing platforms for applications ranging from cancer research [3], [4] to nucleic acid detection [1], [5].

One of the advantages of fluorescence-based sensing is its suitability for spectral multiplexing. To concurrently analyze multiple biological processes (e.g., hybridization in DNA analysis [6] or biological structures (e.g., internal organs in small animal imaging [7]), multiple fluorescent markers can be used,

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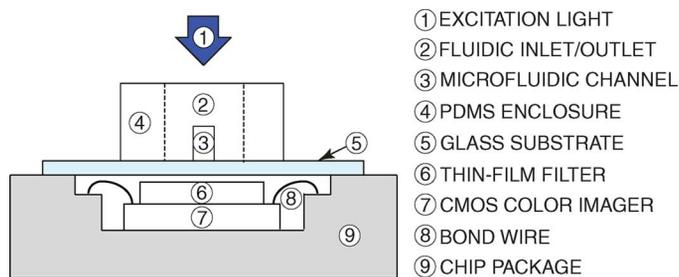


Fig. 1. Schematic cross-section of a CMOS fluorescence contact imaging microsystem.

which can be distinguished by their emission wavelengths (i.e., color).

Fluorescent markers, such as the green-emitting and red-emitting quantum dots (QDs) [8], absorb narrow-band excitation light and emit at longer wavelengths. Emission wavelengths are typically between 500 nm to 700 nm and well-separated (e.g., 50–100 nm) amongst each other. Unlike other spectroscopic applications where continuous fine resolution spectroscopy techniques (e.g., Raman spectroscopy) are required, fluorescence imaging requires spectral differentiation among only a small number of discrete wavelengths. Therefore, a tunable-color light sensor that can detect a finite number of well-separated wavelengths can be used to sense and differentiate the emission wavelengths of various fluorophores.

In fluorescence imaging, fluorophore-labeled biological samples can vary widely in the amount of light they output. For example, in hybridization assays, target analyte concentrations in the order of nano- to milli-molar are typical [2], [9]. In addition, the fluorescence excitation light intensity is typically orders-of-magnitude higher than that of the fluorescence emission. Coupled with the fact that it is difficult to fabricate ultra-thin yet high-performance optical filters, the detection of fluorescence in a contact imaging microsystem may have to be performed in the presence of inadequately-rejected stray excitation light [5]. Therefore, employing a wide dynamic range (WDR) imager is advantageous as it allows for sensing of the low target specimen concentrations superimposed on a substantial background [10].

The choices of the photodetector for fluorescence imaging systems have conventionally been the photo multiplier tube (PMT) and the charge-coupled device (CCD). PMTs are amongst the most sensitive photodetectors, but are bulky, expensive and require high operation voltage making them unattractive to be integrated into a miniaturized system. The throughput of PMT-based detection systems is relatively low due to the lack of parallelism in a single photodetector based

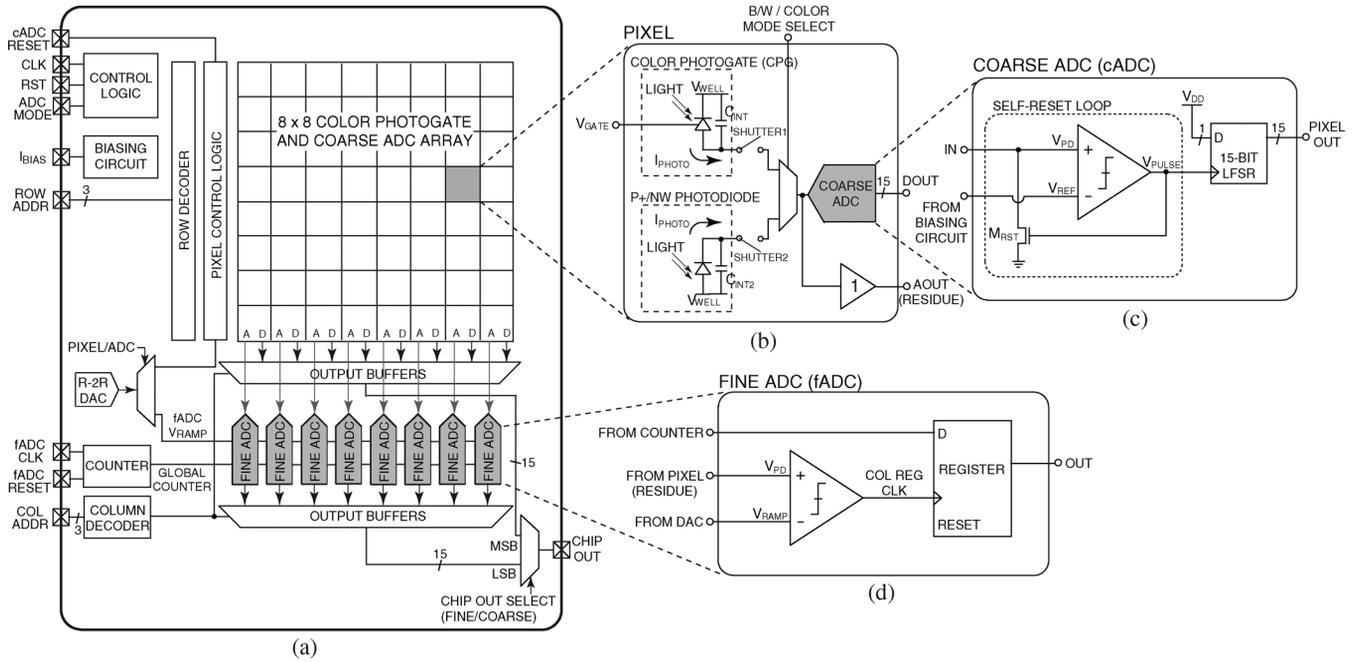


Fig. 2. VLSI architecture of WDR tunable-color digital pixel sensor prototype.

PMT. In contrast, CCDs can be employed in an arrayed implementation, but do not allow for on-chip integration of peripheral circuits such as for signal conditioning. This increases cost and limits miniaturization. CMOS technology, on the other hand, has the advantages of low cost, high integration density, and signal processing versatility, as for example demonstrated in a time-resolved fluorescence imager [11] and a lab-on-chip fluorometer [12].

Numerous dynamic range (DR) enhancement circuit techniques for CMOS image sensors have been reported. The logarithmic sensor provides a wide DR with a simple circuit implementation but achieves a low overall linearity and poor sensitivity under high illumination [13]. The multiple-capture sensor provides a wide DR and maintains high linearity but results in SNR drops at the high illumination range [14]. The asynchronous self-reset technique, albeit requiring a large pixel area, extends the DR and simultaneously achieves high linearity, SNR, and a sensitivity comparable to that of the active pixel sensor [15], [16]. Combined high SNR, DR, and linearity are often primary design requirements for biosensors.

Early asynchronous self-reset based prototypes [17] output only the self-reset count but neglected the charge that remains in the integration capacitor, commonly referred to as the well. This residue charge is not read out and introduces an error. To mitigate this shortcoming, residue quantization is introduced to the asynchronous self-reset technique [15], analogous to a two-step subranging analog-to-digital converter (ADC). The subranging ADC consists of a self-reset ADC, referred to as a coarse ADC (cADC), which produces the most significant bits (MSBs), followed by a residue ADC, referred to as a fine ADC (fADC), which produces the least significant bits (LSBs). The method of residue quantization in [15] is by reusing the in-pixel ADC to also process a signal beyond the full well capacity. Since the fADC and cADC have different input ranges, using the same

ADC circuit in the presence of input-dependent shot noise does not lead to an overall noise-optimized design.

We present a CMOS tunable-color wide dynamic range image sensor prototyped in a standard $0.35\ \mu\text{m}$ CMOS technology. The sensor integrates an 8×8 array of pixels utilizing the CMOS tunable-color photogate (CPG), with the earlier-generation single-pixel prototypes reported by us in [10], [18], [19]. The CPG employs the polysilicon gate as an optical filter, thus requiring no additional optical color filter. We also present an analysis that accounts for photon shot noise for the architectural design of a two-step ADC for image sensors. Based on this analysis, the sensor implements a WDR asynchronous self-reset readout architecture that places the residue ADC at the column level. The sensor is experimentally validated through the measurement of color light intensities and through 2D color imaging. It is also integrated into a contact imaging microsystem for sensing fluorescent samples in a microfluidic channel.

The rest of the paper is organized as follows. Section II discusses the overall VLSI architecture. Section III reviews the tunable-color photogate device. Section IV quantitatively analyzes the two-step ADC VLSI architecture in the presence of shot-noise. Sections V and VI discuss the circuit implementation of the prototype and reports experimental results, respectively. Section VII describes the experimental validation in fluorescence imaging of samples in a microfluidic channel. Section VIII highlights key observations.

II. VLSI ARCHITECTURE

Fig. 2 depicts the chip-level VLSI architecture of the imager. The pixel is schematically depicted in Fig. 2(b). Each pixel integrates a $50\ \mu\text{m} \times 50\ \mu\text{m}$ tunable-color photogate (CPG) [19] for color sensing and a p^+/n -body photodiode to provide monochromatic sensing.

The sensor implements the asynchronous self-reset with the residue readout technique. In this scheme, the photocurrent is first estimated by a coarse ADC and the estimation error is subsequently quantized by a fine ADC and used to improve the accuracy of the final result. In the presented implementation, the asynchronous self-reset cADC is located in the pixel but the fADC is implemented as a column-parallel single-slope ADC. This enables the decoupling of specifications for the two sub-ADCs for noise-optimization described in Section IV. The error that results from coarse analog-to-digital conversion, i.e., the residue charge, is buffered by an in-pixel source follower before it is fed into the column-level fADC.

Fig. 3 depicts key signals within the imager. Analog-to-digital conversion is divided into two phases. Phase 1 is a global operation which begins at the start of the integration time, when the ‘cADC RESET’ signal is asserted to reset the integration node and in-pixel counters. The shutter then closes, feeding the photocurrent into the readout circuit, and the photodiode output voltage V_{PD} raises. If illumination is large enough to exceed the well capacity, the comparator generates a pulse at the node V_{PULSE} , which turns on the reset transistor to reset V_{PD} . Each reset increments the in-pixel counter by one. The number of resets corresponds to the MSBs of the overall two-step ADC output. At the end of integration time, phase 2 begins. In phase 2, the ‘fADC RESET’ signal is asserted to indicate the start of the residue digitization using single-slope operation. For each conversion, a voltage ramp V_{RAMP} is fed into each column-parallel comparator to be compared against the residue voltage, V_{PD} . As V_{RAMP} reaches V_{PD} , the fADC counter latches in the current value of the global counter. The result of this phase produces the LSBs of the final output. Since the fADC is implemented as a column-parallel ADC, it goes through the sampled residues in the pixels within a column and digitizes them sequentially. In other words, light exposure and phase 1 conversion are global operations whereas the phase 2 conversion of residues is performed sequentially.

An on-chip R-2R digital-to-analog converter (DAC) is used to successively generate multiple control voltages for the CPGs (described in Section III) and generate the voltage ramp for the column-parallel single-slope ADCs (described in Section V).

III. CMOS TUNABLE-COLOR PHOTOGATE

Conventional filterless color sensing techniques that solely rely on integrated circuit process technology are based on sensing at specific depths in the bulk silicon. As a result, these techniques tend not to scale well with technology [20], [21]. The color (e.g., RGB Bayer mosaic) filter array used in commercial color cameras does not offer the flexibility to tune detection wavelengths. The CMOS tunable-color photogate (CPG) has been developed to mitigate these difficulties by employing the polysilicon gate as an optical filter. Thus, the CPG does not require an additional optical color filter. An earlier generation single-pixel prototype has been reported in [10], [18] with detailed analysis reported in [19]. A concise description of the CPG principle of operation is given in this section.

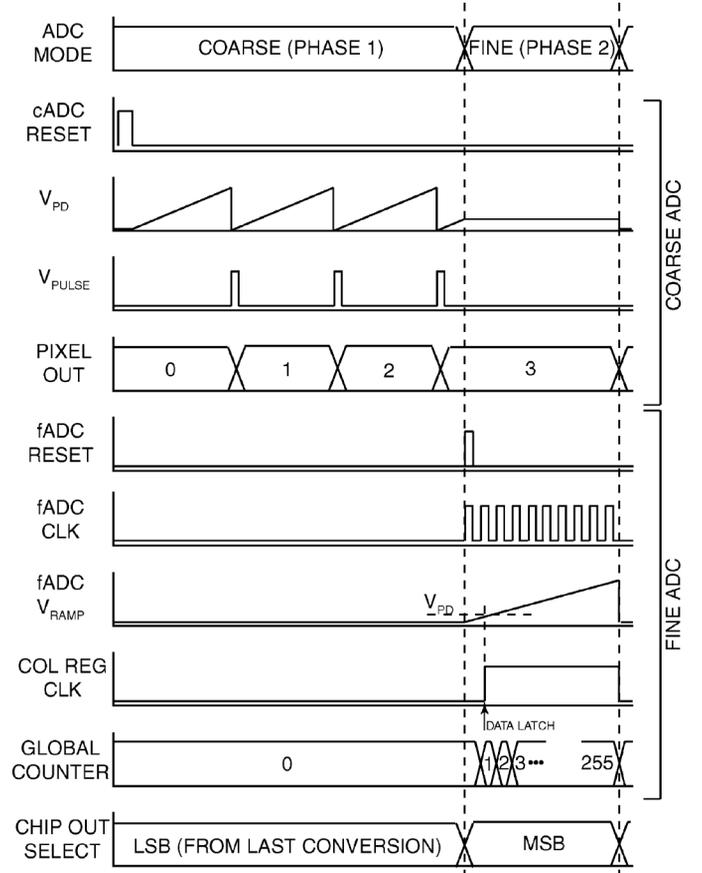


Fig. 3. Transient of key signals in the imager prototype.

A. Principle of Operation

When the CPG is illuminated, the absorption of light is described by the Beer–Lambert law [22]. The absorbed photons generate electron-hole pairs, giving rise to a photocurrent for a single wavelength input that is given by

$$I = \frac{qS\lambda}{hc}(1 - e^{-\alpha(\lambda)\omega(p)})A(\lambda)\phi \quad (1)$$

where ϕ is the radiation intensity, q is the elementary charge, S is the area of the detector, λ is the wavelength, h is Planck’s constant, c is the speed of light in vacuum, α is the absorption coefficient, ω is the effective depth of the sensing region, and $A(\lambda)$ is the light absorption from the various layers between the light source and the detection volume. α is a function of λ and the control parameter p determines the value of ω . For a given detector size, (1) can be rewritten as

$$I = k(p, \lambda)\phi. \quad (2)$$

When multiple wavelengths of light are incident simultaneously, the intensities at these wavelengths can be determined by measurements from multiple photo detectors [23]. For example, for a two-wavelength input, the photo currents I_1 and I_2 measured by two photo detectors can be related to the input intensities ϕ_1 and ϕ_2 (at λ_1 and λ_2 , respectively) by

$$I_1 = k_{11}\phi_1 + k_{12}\phi_2 \quad (3)$$

$$I_2 = k_{21}\phi_1 + k_{22}\phi_2 \quad (4)$$

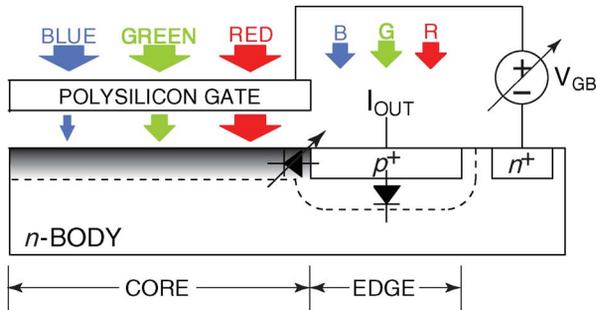


Fig. 4. Cross-sectional view of the CMOS tunable-color photogate (CPG). The poly-gate provides wavelength-dependent light absorption.

where the k -coefficients describe the transfer function of the detectors and can be obtained empirically. Specifically, k_{xy} is the detector sensitivity at λ_x with control input y . The input intensities ϕ_1 and ϕ_2 can be obtained by solving the system of equations, provided that the detectors have unique spectral responses (i.e., (3) and (4) are linearly independent). This model can be extended to a finite set of N wavelengths. To determine the intensity of an input spectrum to a resolution of N distinct wavelengths, N measurements are required from N detectors. Provided that the wavelengths are well-separated, this method offers the flexibility to tune to any arbitrary set of wavelengths within the sensitive range of the silicon photodiode. However, the major limitation of this approach is that it requires the complete set of wavelengths to be sensed be known *a priori* so that the appropriate k -coefficient model can be developed. As a counterexample, the sensor would report incorrect intensities if three wavelengths are present at the input but only a two-wavelength model is used for reconstruction.

B. CPG VLSI Implementation

To create the equivalent of multiple photo detectors with unique spectral responses, the CPG depicted in Fig. 4 has been developed, comprising core and edge regions. The core region of the CPG is covered by a polysilicon gate. A p^+ -diffusion, referred to as the edge region, forms the device output. A n^+ -diffusion fabricated in an n -body forms the body bias ohmic contact.

The gate performs two key functions for color sensing. First, it functions as an optical filter to provide wavelength-dependent absorption as described above. Second, it is a terminal for the induction of an electric field to modulate the extent of photo-generated carrier collection in the core region, the area under the gate. When V_{GB} is applied such that no depletion region is formed under the gate, photo detection only takes place near the p^+/n -body depletion region. When another V_{GB} is applied to form a depletion region at the CPG core, it also participates in photo detection. But the light experiences wavelength-dependent absorption as it travels through the gate. Since the gate provides greater attenuation at shorter wavelengths, the core region provides additional long-wavelength (e.g., red) responsivity to the CPG. Since the edge and core of the CPG have different spectral properties, when different gate-to-body voltages are applied, an equivalent of multiple detectors with unique spectral

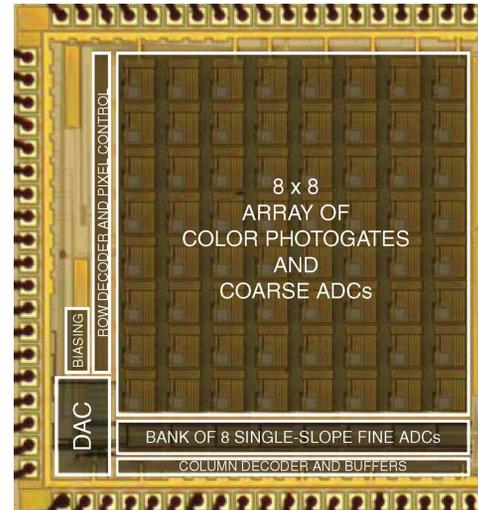


Fig. 5. Micrograph of the $0.35 \mu\text{m}$ standard CMOS $2 \text{ mm} \times 2 \text{ mm}$ color sensor die with a $175 \mu\text{m} \times 175 \mu\text{m}$ pixels.

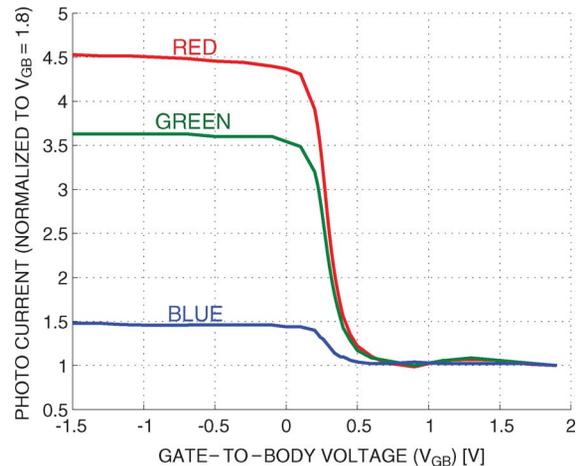


Fig. 6. Measured $50 \mu\text{m} \times 50 \mu\text{m}$ CPG photocurrent for monochromatic light at 620 nm (red), 520 nm (green), and 450 nm (blue).

responses is created, e.g., for two colors, (3) and (4) are implemented by a single device.

It is worth noting that, in a $0.35 \mu\text{m}$ standard CMOS technology, the thickness of the polysilicon gate is approximately 300 nm [24], leading to an approximate attenuation of 65% for blue light (450 nm), 30% for green light (520 nm), and 15% for red light (620 nm), based on the wavelength-dependent polysilicon absorption coefficients of 3.56 , 1.35 , and $0.45 \mu\text{m}^{-1}$ for blue, green, and red light, respectively. The overall image chip micrograph is depicted in Fig. 5. The photocurrent of a $50 \mu\text{m} \times 50 \mu\text{m}$ CPG is depicted in Fig. 6, where the photocurrent is measured across V_{GB} for three monochromatic illuminations using a semiconductor parameter analyser. To highlight the relative change in the current, the results are normalized to one at $V_{GB} = 1.8 \text{ V}$. For $0 \text{ V} < V_{GB} < 0.6 \text{ V}$, the ratio of the currents corresponding to each color changes significantly across V_{GB} . Therefore, $V_{GB} = 0 \text{ V}$ and $V_{GB} = 0.6 \text{ V}$ are utilized for the multiple measurements as required in (3) and (4). The generation of multiple values of V_{GB} is automated by the on-chip DAC. Multiple CPG responses at different values of

V_{GB} are passed through the ADC for digitization. The reconstruction algorithm that solves for the input spectrum ϕ in (3) and (4) is implemented in software.

IV. SHOT NOISE-AWARE WDR TWO-STEP IMAGER ADC

The exploitation of photon shot noise to reduce the noise requirement of a multi-ramp single-slope imager ADC has been demonstrated [25]. In this section, shot noise exploitation for the asynchronous self-reset with residue readout WDR architecture is described qualitatively first. A quantitative analysis is then presented for a general two-step imager ADC.

A. Qualitative Analysis

In Fig. 7, the transfer characteristic of the image sensor is plotted on a logarithmic scale. Under the customary assumption that one input photon results in one output electron, the input-referred and output-referred quantities are equivalent and are interchangeable for the purpose of the following analysis. Noise sources depicted in Fig. 7 are the photon shot noise and read noise, which consists of thermal and flicker noise of the photodiode and readout circuit. In a conventional active pixel sensor (APS), the sensor output increases linearly with the light intensity until the full well capacity N_{FW} is reached. For an imager with extended DR, the output reaches a higher value, N_{SAT} , typically limited by mechanisms that are specific to implementation, e.g., in-pixel memory depth for certain self-reset schemes.

The photon shot noise has a standard deviation equal to the square root of the input light signal, in units of electrons. Because photon shot noise increases with the input, as opposed to the input-independent read noise, it becomes the dominant noise source at higher light intensities. In this part of the input range, the conventional ADC has a better noise performance than is required, i.e., its quantization and thermal noise can be increased without decreasing the overall noise performance.

Fig. 8 also illustrates the above idea for the asynchronous self-reset cADC and residue fADC architecture depicted in Fig. 2. In this architecture, the cADC is only active when the input signal exceeds the full well capacity, N_{FW} , at which point, the shot noise is σ_{FW} . Therefore, since the irreducible shot noise component is already substantial, a cADC noise floor much below σ_{FW} is over designed in terms of keeping the combined shot noise and read noise at a reasonable level. Unlike the cADC, the fADC operates from the dark condition to N_{FW} . Therefore, the fADC noise floor is ideally minimized. Since the area constraint limits the performance of in-pixel ADCs and that a high performance is required from the fADC, it is implemented in the periphery as a column-level circuit.

B. Quantitative Analysis

This section presents an analysis that can be used as a guideline for the architectural design of the two-step ADC. In order to keep the analysis general to any two-step imager ADC architecture, the formulation is not specific to particular fADC and cADC implementations. Therefore, it is assumed that the noise floors of the ADCs are independent of the input amplitude, as most types of ADC exhibits this characteristic.

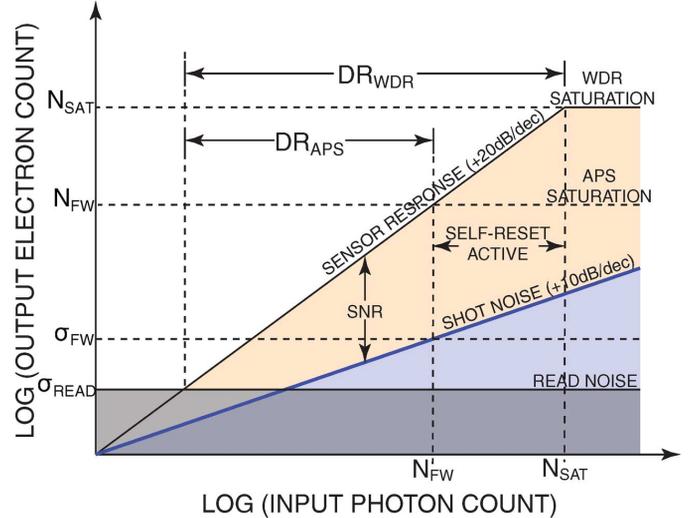


Fig. 7. Imager transfer curve illustrating the concept of shot noise as an input-dependent noise source.

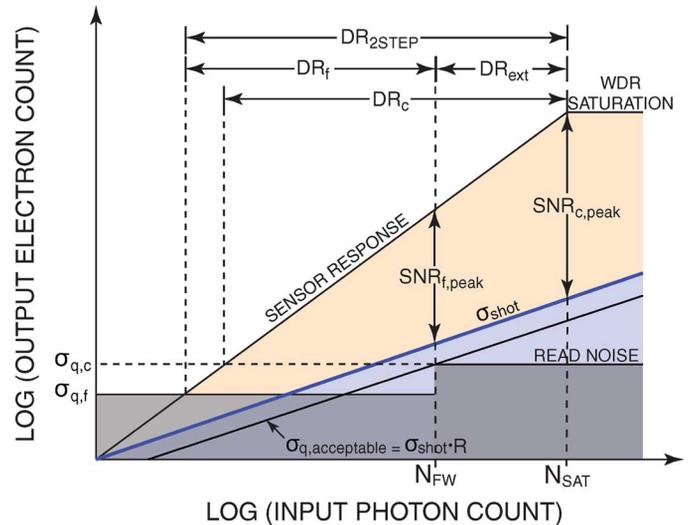


Fig. 8. Imager transfer curve illustrating shot-noise-aware design.

The analysis begins with the well capacity, which is the amount of charge that a pixel can hold in a single photocurrent integration, given by

$$N_{FW} = \frac{C_{int} V_{int}}{q} \quad (5)$$

where C_{int} and V_{int} are the integration capacitance and integration voltage, respectively, and q is the elementary charge. It is worth noting that C_{int} is in most cases the parasitic capacitance of the photodiode. Since C_{int} is process dependent and V_{int} depends primarily on the supply voltage, N_{FW} is largely determined by the process technology.

The asynchronous self-reset with residue readout scheme can be regarded as a conventional active pixel sensor with dynamic range extension at high illumination via self-reset operation. Since imager ADCs are usually designed such that their quantization noise does not exceed the read noise [25], in this analysis, the fADC root-mean-square (RMS) quantization noise, $\sigma_{q,f}$, is chosen to be equal to the read noise, σ_{read} , i.e.,

$$\sigma_{q,f} = \sigma_{read}. \quad (6)$$

It is well established that, for an input that follows a uniform probability distribution function, the RMS quantization noise of an ADC, σ_q , can be related to the quantization step size, N_{LSB} , as follows [26]

$$\sigma_q = \frac{N_{LSB}}{\sqrt{12}}. \quad (7)$$

Therefore, the fADC quantization step size is given by

$$N_{LSB,f} = \sqrt{12}\sigma_{q,f}. \quad (8)$$

From the ratio of the largest to the smallest signal, the resolution of the fADC and cADC can be readily formulated. The number of bits for the fADC, N , is given by

$$\frac{N_{FW}}{N_{LSB,f}} = 2^N \Rightarrow N = \log_2 \frac{N_{FW}}{N_{LSB,f}}. \quad (9)$$

The saturation signal of the entire two-step DR, N_{SAT} , is determined by the maximum input light intensity specification. The number of bits for the cADC, M , is given by

$$\frac{N_{SAT}}{N_{FW}} = 2^M \Rightarrow M = \log_2 \frac{N_{SAT}}{N_{FW}}. \quad (10)$$

The resolution of the two-step ADC is therefore $M + N$ bits.

The analysis next proceeds to obtain an expression for the RMS quantization noise of the cADC, $\sigma_{q,c}$. The standard deviation of shot noise is given by

$$\sigma_{shot}(N_{sig}) = \sqrt{N_{sig}} \quad (11)$$

where N_{sig} is the input photon count. Referring to Fig. 8, in order to constraint the cADC quantization noise to an acceptable level, $\sigma_{q,acceptable}$, a quality ratio R is defined to relate the cADC noise to shot noise, given by

$$R = \frac{\sigma_{q,acceptable}}{\sigma_{shot}(N_{sig})}. \quad (12)$$

If $R = 1$, then $\sigma_{q,acceptable} = \sigma_{shot}$. Therefore, to ensure that $\sigma_{q,c}$ is below shot noise, R is chosen to be less than unity.

As depicted in Fig. 8, since $\sigma_{q,acceptable}$ has its minimum at N_{FW} within the range that the cADC self-resets (i.e., N_{FW} to N_{SAT}) and since $\sigma_{q,c}$ must be smaller or equal to $\sigma_{q,acceptable}$, $\sigma_{q,c}$ is chosen to be equal to the acceptable noise level evaluated at the full well level, i.e.,

$$\sigma_{q,c} = \sigma_{q,acceptable}(N_{FW}). \quad (13)$$

This guarantees that $\sigma_{q,c}$ is below shot noise for $N_{sig} \geq N_{FW}$. At full well, using (11) and (12), $\sigma_{q,c}$ is given by

$$\sigma_{q,c} = R \cdot \sigma_{shot}(N_{FW}) = R \cdot \sqrt{N_{FW}}. \quad (14)$$

Using (7) and (14), the quantization step size for the cADC is given by

$$N_{LSB,c} = \sqrt{12}\sigma_{q,c} = R\sqrt{12N_{FW}}. \quad (15)$$

As a measure of the noise increase, or equivalently the reduction of the noise requirement of the cADC, the factor F is defined, given by

$$F = \frac{\sigma_{q,c}}{\sigma_{q,f}} = \frac{N_{LSB,c}}{N_{LSB,f}} = \frac{R\sqrt{12N_{FW}}}{N_{LSB,f}} \quad (16)$$

which is interestingly proportional to the square root of the well capacity. Also, combining (9) and (16), F can be expressed as

$$F = \frac{R\sqrt{12}}{\sqrt{N_{FW}}}2^N \quad (17)$$

which states that once the fine ADC resolution, N , is fixed, the factor F is inversely proportional to $\sqrt{N_{FW}}$.

Key performance metrics of the fADC and cADC can then be computed. The dynamic range is defined as the ratio of the largest signal to the smallest detectable signal. The DRs, in dB, for the fADC and cADC are, respectively

$$DR_f = 20 \log_{10} \frac{N_{FW}}{\sigma_{q,f}} \quad (18)$$

and

$$DR_c = 20 \log_{10} \frac{N_{SAT}}{\sigma_{q,c}}. \quad (19)$$

But as shown in Fig. 8, the DR of the overall two-step ADC is not merely DR_c as is the case for a conventional two-step ADC. Rather, the extended DR is involved, given by

$$DR_{ext} = 20 \log_{10} \frac{N_{SAT}}{N_{FW}}. \quad (20)$$

The DR of the overall two-step ADC is given by

$$DR_{2STEP} = 20 \log_{10} \frac{N_{SAT}}{\sigma_{q,f}} = DR_f + DR_{ext}. \quad (21)$$

This DR analysis reveals an important property of the two-step WDR ADC. When shot noise is considered, as in this analysis, the cADC noise floor can be raised, which relaxes the DR requirement of the cADC. However, as illustrated in Fig. 8, $\sigma_{q,c}$ still has to be designed to a level below the cADC LSB step size, namely, the full well level. Therefore, the cADC effective number of bits (ENOB) exceeds its actual number of bits. As mentioned previously, if $\sigma_{q,c}$ is designed to be in the neighborhood of $\sigma_{q,f}$, the cADC has better noise performance than is required. But, if $\sigma_{q,c}$ is equal to the full well level, then the final result of the entire two-step ADC is only accurate to the cADC LSB and renders the entire N bits of the fADC inaccurate.

The signal-to-noise ratios (SNRs) in dB for the fADC in the read noise dominant (low signal) and shot noise dominant (high signal) regimes are, respectively

$$\text{SNR}_{f,low} = 20 \log_{10} \frac{N_{sig}}{\sigma_{q,f}} = 20 \log_{10} \frac{\sqrt{12}N_{sig}}{N_{LSB,f}} \quad (22)$$

and

$$\text{SNR}_{f,high} = 20 \log_{10} \frac{N_{sig}}{\sigma_{shot}} = 20 \log_{10} \sqrt{N_{sig}}. \quad (23)$$

The peak SNR in dB of the fADC is obtained by evaluating $\text{SNR}_{f,high}$ at the highest fADC input, given by

$$\text{SNR}_{f,peak} = 20 \log_{10} \frac{N_{FW}}{\sigma_{shot}(N_{FW})} = 20 \log_{10} \sqrt{N_{FW}} \quad (24)$$

assuming, as it is typical of imagers, that shot noise dominates at the full well level. Analogously, since $\sigma_{q,c}$ is designed (from (13)) to be below shot noise in the extended dynamic range, the imager is shot noise dominant within this range. Hence the SNR in dB in the extended DR is given by

$$\text{SNR}_{ext} = 20 \log_{10} \frac{N_{sig}}{\sigma_{shot}} = 20 \log_{10} \sqrt{N_{sig}} \quad (25)$$

which has the same expression as $\text{SNR}_{f,high}$. Analogously, the cADC peak SNR in dB is given by

$$\text{SNR}_{c,peak} = 20 \log_{10} \frac{N_{SAT}}{\sigma_{shot}(N_{SAT})} = 20 \log_{10} \sqrt{N_{SAT}}. \quad (26)$$

Lastly, the peak SNR of the overall two-step ADC is given by

$$\text{SNR}_{2STEP,peak} = 20 \log_{10} \frac{N_{SAT}}{\sigma_{shot}(N_{SAT})} = \text{SNR}_{c,peak} \quad (27)$$

which is different from the ratio of the maximum input to the noise at the zero signal level, as is often the case for most types of ADCs. This difference is a direct result of the presence of shot noise. Strictly speaking, the above peak SNR expressions are approximations, as read noise has not been included. But since the peak SNRs are evaluated at the illumination level where shot noise dominates over read noise, the approximations are nonetheless accurate.

As a numerical example of the above quantitative analysis, the following parameters with values typical to CMOS imagers are assumed [27]: $\sigma_{read} = 5 e^-$, $N_{FW} = 10,000 e^-$, and $N_{SAT} = 1 \times 10^6 e^-$. Assume that the fADC quantization noise is designed to be equal to the read noise, i.e., $\sigma_{q,f} = \sigma_{read} = 5 e^-$. From (8), $N_{LSB,f} = 17.3 e^-$. From (9) and (10), the number of bits for the fADC and cADC are $N = 9.2$ bits and $M = 6.6$ bits, respectively. Suppose the cADC is designed to have a quantization noise comparable to shot noise at the full well input, i.e., $R = 1$. Therefore, based on (14) and (15), it can be computed that $\sigma_{q,c} = 100 e^-$ and $N_{LSB,c} = 346 e^-$, respectively. From (16), the cADC noise floor can be raised 20 times ($F = 20$) while not incurring a severe noise degradation. This translates to a power and/or area saving. From (24) and (26), the peak SNRs for the fADC and cADC are estimated to be 40 dB and 60 dB, respectively. From (27), the peak SNR of the two-step ADC is 60 dB. From (18)–(20), DR_f , DR_c , and DR_{ext} are 66 dB, 80 dB, and 40 dB, respectively. Since the overall DR is $DR_f + DR_{ext} = 106$ dB, the fact that shot noise is taken into account relaxed the cADC noise requirement by 26 dB. An important benefit of this is a much reduced pixel area for an in-pixel cADC implementation (an asynchronous self-reset ADC is required to be implemented in-pixel). It is

also worth noting that since the shot noise magnitude is equal to the square root of the signal magnitude, in this example, after 10,000 resets, the equivalent signal is $10,000^2 e^-$. This results in a shot noise of 10,000 e^- , which is equal to the full well capacity. Therefore, the entire residue or the entire fADC output consists of noise.

V. CIRCUIT IMPLEMENTATION

The design of Fig. 2 has been fabricated in a 0.35 μm standard digital CMOS technology. The 175 $\mu\text{m} \times 175 \mu\text{m}$ pixels with a 10% fill factor are tiled to form a 8×8 array for imaging.

A. Pixel Circuit Implementation

The pixel readout circuit consists of an electronic shutter, a reset block, and ADC block that implements asynchronous self-reset, the coarse part of the two-step ADC operation. The reset block includes a comparator and a reset transistor. The ADC has a 15-bit linear feedback shift register (LFSR) counter which dominates the pixel area. The choice of 15-bit is to provide a wide dynamic range even without the use of the fADC. This enables the imager to support a high frame rate mode with pixel-parallel A/D conversion.

Referring to the circuit in Fig. 2(c) and timing diagram in Fig. 3, in the beginning of each integration period, the counter is cleared and the photodiode output V_{PD} is charged to the reset voltage $V_{RST} = 0$ V. The n -body is biased at the voltage $V_{BODY} = 1.5$ V. The photocurrent causes V_{PD} to rise, charging the integration capacitor C_{INT} . When V_{PD} reaches the comparator reference voltage $V_{REF} = 1$ V, the comparator changes state, causing the reset transistor M_{RST} to turn on, resetting V_{PD} to V_{RST} . After reset, the comparator output toggles back to the original state. The combination of two toggles generate a pulse with a width that equals the time it takes to reset C_{INT} . In the absence of circuit nonidealities and ignoring the residue, the resulting pulse train has a pulse frequency proportional to the incident light intensity. The asynchronous self-reset ADC is less sensitive to supply voltage scaling as it effectively represents the light signal by a digital count, rather than a voltage across a capacitor.

The voltage comparator is a two-stage design with large PMOS input transistors to lower thermal and flicker noise. Fig. 9 depicts the voltage comparator. The first stage employs cross-coupling to increase the output resistance of the load transistors M_1 through M_4 . The second stage provides an additional gain. The first stage and the second stage consume 18 μA and 10 μA for the 3.3 V supply, respectively. The comparator has a 66 dB simulated DC gain for resolving ≈ 1 mV for a maximum input swing of 2 V. It has a 3-dB bandwidth of 10 MHz.

B. Column-Parallel Analog-to-Digital Converters

The column-parallel single-slope ADC of Fig. 2(d) digitizes the residue voltage V_{PD} . It consists of a voltage comparator with the same topology as the in-pixel comparator of Fig. 9 and a 15-bit binary counter. A global counter is connected to both the on-chip DAC and the column-parallel ADC sub-circuits as shown in Fig. 2(a). During analog-to-digital conversion, it increments in order to have the DAC output a ramp voltage V_{RAMP}

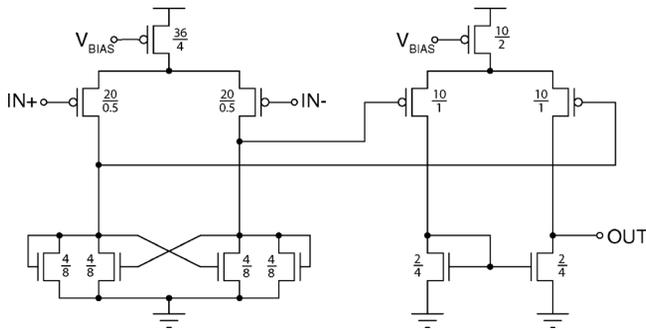


Fig. 9. Schematic of the voltage comparator.

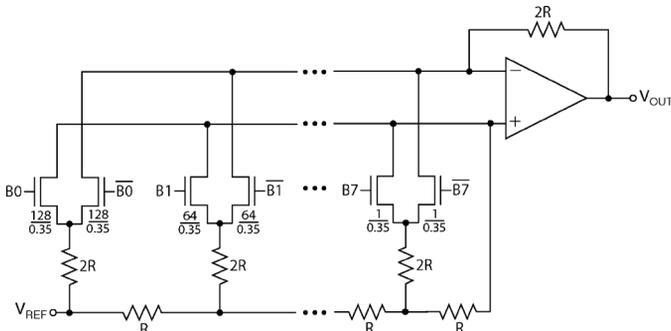


Fig. 10. Schematic of the on-chip R-2R DAC.

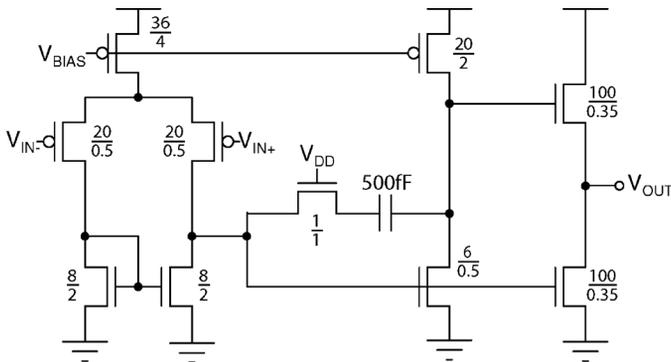


Fig. 11. Schematic of the operational amplifier within the DAC.

to the column-parallel ADCs. As depicted in Fig. 3, V_{RAMP} is compared to the residue voltage V_{PD} . When V_{RAMP} reaches V_{PD} , the comparator clocks the register to latch in the present global counter value, which is the digital representation of V_{PD} .

C. Digital-to-Analog Converter

The schematic of the on-chip DAC is shown in Fig. 10. The DAC is based on the R-2R architecture [26], due to the availability of high-precision resistors in the CMOS process used. Unlike the conventional resistance-ratio ladder converter [26], the R-2R converter realizes binary-weighted currents with a smaller number of components and with a resistance ratio of only two, independent of the number of bits.

Switches are sized proportionately to accommodate the binary increase in the current level through each branch. The unit resistors R_{unit} are 5 k Ω non-silicided polysilicon resistors, each occupying an area of 24 $\mu\text{m} \times 1.1 \mu\text{m}$. The opamp is based on the two-stage opamp architecture, depicted in Fig. 11. PMOS

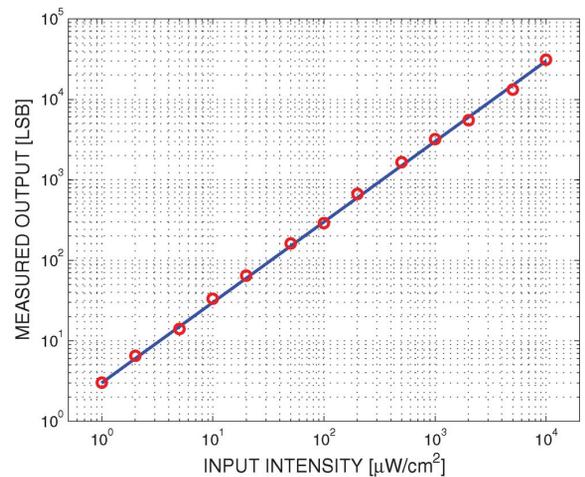


Fig. 12. Experimentally measured imager output as a function of input intensity.

input transistors are used to lower the flicker noise. The DAC occupies an area of 300 $\mu\text{m} \times 120 \mu\text{m}$.

VI. EXPERIMENTAL RESULTS

A. Pixel Readout Circuit

The experimentally measured transfer characteristic is depicted in Fig. 12, obtained from illumination provided by a halogen lamp onto a pixel. The input light intensity is measured by an optical power meter (with a detector calibrated for broadband sensing) and is varied by over four orders of magnitude using neutral density (ND) filters. ND filters used are from Thorlabs with optical densities (OD) of 0.3, 0.7, 1.0, 2.0, 3.0, and 4.0 and are combined to provide various degrees of attenuation. Measurements are collected using the 50 $\mu\text{m} \times 50 \mu\text{m}$ CPG which is set to the highest photo sensitivity, i.e., $V_{GB} = 0 \text{ V}$. At each intensity, 32 measurements are obtained to calculate the average and standard deviation σ of the imager output. The experimentally measured transfer characteristic is depicted in Fig. 12, obtained from illumination provided by a halogen lamp onto a pixel. The input light intensity is measured by an optical power meter (with a detector calibrated for broadband sensing) and is varied by over four orders of magnitude using neutral density (ND) filters. ND filters used are from Thorlabs with optical densities (OD) of 0.3, 0.7, 1.0, 2.0, 3.0, and 4.0 and are combined to provide various degrees of attenuation. Measurements are collected using the 50 $\mu\text{m} \times 50 \mu\text{m}$ CPG which is set to the highest photo sensitivity, i.e., $V_{GB} = 0 \text{ V}$. At each intensity, 32 measurements are obtained to calculate the average and standard deviation σ of the imager output.

The experimentally measured SNR of the imager output, depicted in Fig. 13, is calculated as mean over standard deviation of the output. The input-referred dynamic range is defined as the maximum output over the RMS value of the readout noise σ , i.e., the standard deviation of the imager output under dark condition [27]. Therefore, the DR is the range between SNR = 0 and the highest signal level in Fig. 13 and is measured to be 82 dB, limited by the maximum light intensity achievable by

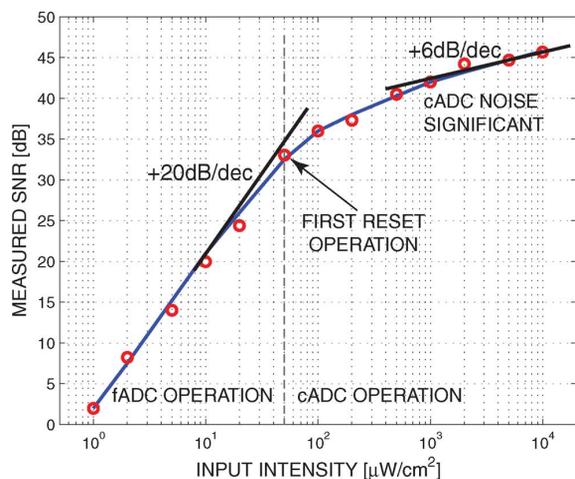


Fig. 13. Experimentally measured imager SNR as a function of input intensity.

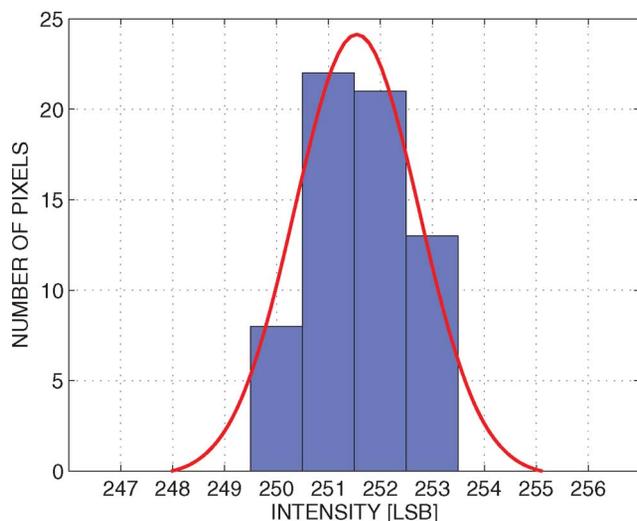


Fig. 14. Histogram of the sensor output under uniform illumination.

the light source in the high end and the read noise in the low end. In Fig. 13, as the input signal increases, the SNR improves at 20 dB/dec at low illumination where the total noise is dominated by the input-independent noise of the fADC readout circuit. As the number of reset operations increases, the noise in the self-reset loop (e.g., reset noise) accumulates, which reduces the rate of increase of the SNR to approximately 6 dB/dec at very high illumination levels. This increase in cADC noise has also been reported in [15] and must be minimized. As depicted in Fig. 13, the peak SNR of 46.2 dB has been measured at the highest input intensity. Fig. 13 also depicts a measured number of reset pulses of 200, which is equivalent to a DR increase of 46 dB over the same CMOS image sensor without any DR enhancement, i.e., with the cADC disabled.

To evaluate the fixed pattern noise (FPN) of the imager, uniform illumination is applied to the entire pixel array. Fig. 14 depicts the histogram of image intensities resulting from uniform illumination. The average intensity is 251.1 counts with a FPN (1σ) of 0.38%.

B. Digital-to-Analog Converter

The DAC consumes 1.24 mW and achieves 8-bit accuracy with INL and DNL shown in Fig. 15(a) and (b), respectively.

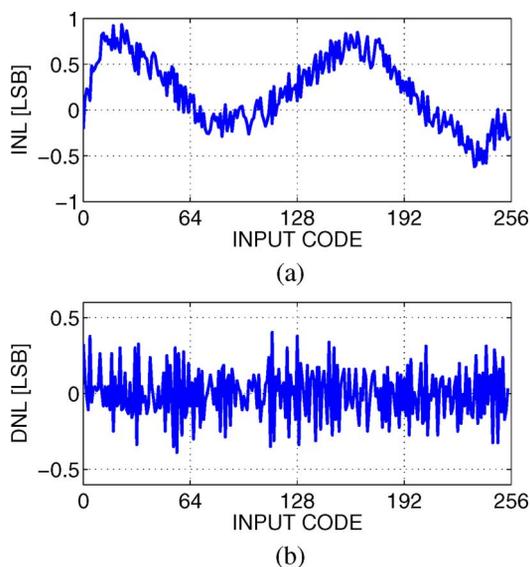


Fig. 15. Experimentally measured on-chip DAC performance: (a) INL, and (b) DNL.

The opamp within the DAC achieves a simulated DC gain of 69 dB and a 3-dB bandwidth of 20 kHz.

C. System-Level Validation in Color Light Measurements

The 0.35 μm CMOS prototype in Fig. 5 has been tested in light intensity measurements at the green (520 nm) and red (620 nm) wavelengths using two current-controlled light-emitting diodes (LEDs) for input illumination.

In order to measure the intensity at two known wavelengths, according to (3) and (4), an empirical model with four k -coefficients is required. The extraction of k -coefficients can be performed as follows. For example, in (3), to extract k_{11} , a known light intensity ϕ_1 serves as the input of the measurement I_1 (at V_{GB1}). Similarly, for k_{12} , a known light intensity ϕ_2 is applied as an input for another measurement at V_{GB1} . This process is then repeated for V_{GB2} . Following the above procedure, only N measurements are required to determine all N k -coefficients. Additionally, it has been found that modeling accuracy can be improved by simultaneously utilizing multiple combinations of input colored light intensities to solve for the average k -coefficients. The k -coefficients are obtained only once, and are stored for subsequent reconstruction calculations.

To resolve the input to two wavelengths, each input light is measured two times using $V_{GB1} = 0$ V and $V_{GB2} = 0.6$ V. The raw measurements and the previously obtained model are combined to reconstruct the input using (3) and (4). Fig. 16 depicts measured intensities after reconstruction for an illumination that simultaneously contains green (520 nm) and red (620 nm) light. For each of the two wavelengths, intensities of 0, 60, 120, 180, 240, and 300 $\mu\text{W}/\text{cm}^2$ have been used. Fig. 16(a) depicts measured tunable-color photogate response across the illumination range for two gate-to-body voltages. These data are used to determine the k -coefficients to create a linear model (depicted as a mesh). In order to evaluate the crosstalk between color channels, for each intensity step, the intensity of the other color is swept. For example, in Fig. 16(b), for each of the six green intensities, the red intensity is varied in six levels. Therefore, based on six

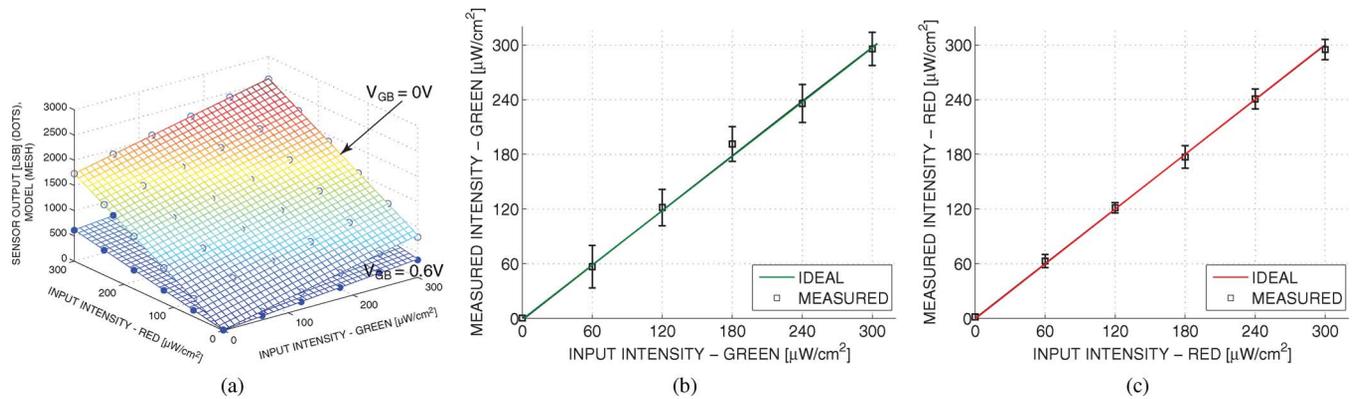


Fig. 16. Simultaneous two-color light-emitting diode (LED) illumination measurements: (a) measured tunable-color photogate response for two gate-to-body voltages across illumination (circles). A linear model based on k -coefficients is superimposed (mesh). (b) Reconstructed intensity of the green (520 nm) input component. (c) Reconstructed intensity of the red (620 nm) input component.

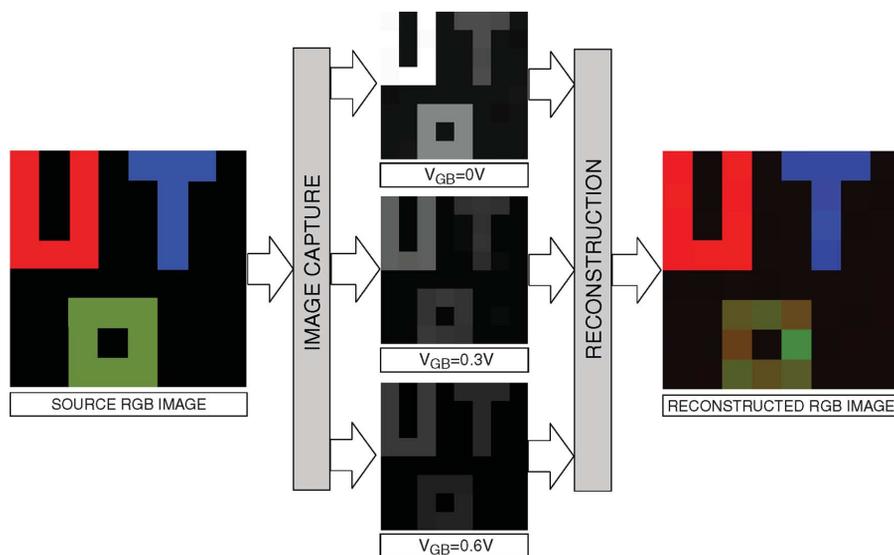


Fig. 17. Color imaging: RGB image reconstructed from input images captured at $V_{GB} = 0\text{ V}$, 0.3 V , and 0.6 V , from top to bottom, respectively. $V_{BODY} = 1.5\text{ V}$.

intensity steps, each against six intensities of the other color, a total of 36 measurements have been performed. Each error bar contains a sweep across all intensities of the other color and depicts one standard deviation from the mean value. Fig. 16(c) is analogous to Fig. 16(b) but for the red component of the input light.

The SNR is commonly defined for imagers as $\text{SNR} = \mu/\sigma$, where μ and σ are the mean and standard deviation of the output calculated over temporal measurements for all pixels [28]. As shown in Fig. 16(b) and (c), the peak SNRs measured at the intensity of $300\ \mu\text{W}/\text{cm}^2$ are 24.3 dB and 28.5 dB for the green and red components, respectively. In a separate high input intensity test (result not shown), the imager achieves a peak SNR of 29.2 dB and 34.8 dB for green and red light at the intensity of $1500\ \mu\text{W}/\text{cm}^2$ (limited by maximum LED output).

D. System-Level Validation in 2D Color Imaging

Although the imager has been designed for fluorescence sensing application rather than for the photographic application, its ability to reproduce an image is evaluated via capturing of a still photographic image. It is an image abbreviating the

string ‘University of Toronto’ by the characters ‘U’, ‘o’, and ‘T’, on a black background. The approximately $10\text{ cm} \times 10\text{ cm}$ image is held approximately 0.9 m from the lens, which focuses the light onto the pixel array. The lens aperture is at $F/16$ and the integration time is 1 sec under $\approx 200\ \mu\text{W}/\text{cm}^2$ of illumination. The image captured by the proposed sensor is depicted in Fig. 17. The entire array of pixels use a global color model or k -coefficient matrix. One key advantage of the proposed approach to color sensing is that each pixel produces the entire set of RGB values. Therefore, color interpolation, a process that approximates missing color information from neighboring pixels commonly performed in cameras with a color filter mosaic array, is not required. This eliminates the associated color artifacts.

Table I summarizes the experimentally measured electrical characteristics of the image sensor prototype depicted in Fig. 5.

VII. VALIDATION IN FLUORESCENCE IMAGING

The tunable-color sensor prototype has been evaluated as a part of a fluorescence imaging microsystem to validate its suitability for point-of-care (POC) diagnostic applications. POC

TABLE I
EXPERIMENTAL CHARACTERISTICS

Technology	0.35 μ m standard CMOS
Supply Voltage	3.3V
Chip Power Consumption (30fps)	8mW
Pixel Power Consumption (30fps)	100 μ W
Pixel Size	175 μ m \times 175 μ m
Photodetector Type	p^+ -FD/ n -body photogate
Core Area	1.6mm \times 1.6mm
Array Pixel Count	8 \times 8
Integration Capacitance	250fF
Counter Size	15-bit (33k count)
Max. Effective Well Capacity	156ke ⁻ \times 33k (at $V_{REF}=1V$)
Optical Sensitivity	3.3 μ W/cm ² /level
Max. Photocurrent	2.5 μ A
Dark Current	0.25 count/sec
Max. Pulse Frequency	10MHz
Frames Per Second	0.1-100
FPN (1σ)	0.38%
Peak SNR	46dB
Dynamic Range	82dB
DAC Power Consumption	1.24mW
DAC Maximum INL	+0.9/-0.6 LSB
DAC Maximum DNL	+0.4/-0.4 LSB

devices are becoming increasingly popular as they promise to bring diagnostic technology from the standard laboratory setting to the patient residence to facilitate early diagnosis [29]. Although miniaturization is a key for the development of such devices, for optical transduction such as fluorescence-based detection, a fluorescence microscope is commonly employed. Despite the high sensitivity and selectivity offered by this transduction method and its widespread applications ranging from the detection of nucleic acids, proteins and small molecules, its incorporation into POC devices has been limited due to the limited portability and the high cost of the instrumentation. One emerging technique with a potential to overcome the limitations of a fluorescence microscope is contact imaging [30]. Unlike the conventional fluorescence microscope, in contact imaging as depicted in Fig. 1, the object to be imaged is placed in close proximity to the focal plane, eliminating the need for bulky and expensive optics such as a system of lenses and mirrors, which enables miniaturization to realize lab-on-a-chip platforms.

Microfluidic networks offer many advantages for chemical and biological sensing. First, reaction time is greatly shortened, in some cases from hours to minutes [31], as active delivery by electrokinetic flow can be used to accelerate interactions between molecules over an otherwise slow diffusion-limited process. Secondly, small sample volumes in the nano-liter range can be readily transported and processed by means of microfluidic networks. Thirdly, sensing of samples within a microfluidic channel where the chemical reaction occurs facilitates real-time detection.

Integrating an imager with microfluidics can serve a variety of applications. Spatial imaging of a fluidic channel, for example, can be a method to analyze the result of electrophoresis experiments where the outcome is determined by detecting the distance traveled by dispersed particles relative to a fluid under the influence of an electric field [32].

Quantum dots (QDs) as fluorescent markers exhibit a number of unique optical properties that render them superior than organic fluorescent dyes. These unique properties include: narrow, symmetric and size-tunable emission spectra (full width at half maximum, FWHM of 25–35 nm); strong and broad absorption spectra; high quantum yield (>20%) and long life time (> 10 ns) [8]. As compared to organic fluorophores, QDs have greater resistance to photobleaching that enables long-term monitoring. The broad absorption spectra of QDs allows for multiple colors of QDs to be excited efficiently with a single excitation source which is generally not possible with organic dyes. These properties make QDs ideal as fluorescent biomarkers.

A. Microsystem Prototype Design

The microsystem prototype consists of a blue LED for fluorescence excitation, an optical filter for excitation rejection, a fluidic structure for holding the sample solution, and the CMOS CPG imager for photo detection. A 100- μ m-thick, 1.5 mm \times 1.5 mm optical interference filter is used to attenuate the 450 nm (FWHM = 20 nm) excitation light from the Philips Luxeon K2 450 nm (FWHM = 20 nm) blue LED. The filter is fabricated using 60 layers of Nb₂O₅ and SiO₂ (by Omega Optical) to the required specification, and optically tested prior to integration with the CMOS die. This approach is chosen over the direct deposition of thin-film layers over the CMOS die to ensure that well-established methods for coating planar substrates can be used during filter fabrication. The filter is a long-pass design with a cut-off wavelength of 510 \pm 2 nm. The filter has been tested to provide an optical density (OD) of six (i.e., 10⁶ attenuation) at the excitation wavelength of 450 nm, with a transmission rate greater than 90% at 520 nm and on average greater than 85% from 520 nm to 700 nm.

The microfluidic device consists of a hybrid of top polydimethylsiloxane (PDMS) cover and bottom glass substrate. The channels are fabricated in PDMS using a soft-lithography (rapid prototyping and replica molding) technique. PDMS base and curing agent are thoroughly mixed in a 10:1 ratio, the mixture has been degassed under vacuum, and then 3 g of the mixture are poured onto the microfluidic template and cured in an oven at 120°C for 30 min. The cured PDMS cover is peeled off and the inlets and outlets at the ends of each channel are punched out using a 2 mm diameter metal bore. The PDMS cover is then air plasma oxidized for 30 s at 10.5 W and is immediately sealed to a plasma oxidized glass coverslip.

Fig. 1 depicts a simplified cross-sectional view of the resulting microfluidic device. It has 1 cm (length) \times 250 μ m (width) \times 11 μ m (height) channels, terminated by an inlet and an outlet on each end. The microfluidic device is subsequently integrated with the CMOS sensor as shown in Fig. 18(a). Fig. 18(b) depicts an enlarged view of the microfluidic channel passing over the sensor pixel array.

TABLE II
CMOS FLUORESCENCE MICROSYSTEMS COMPARATIVE ANALYSIS

	This Work	[5]	[33]	[34]	[28]
CMOS Technology	0.35 μm	0.35 μm	5 μm	0.18 μm	0.5 μm
Supply Voltage	3.3V	3.3V	5V	1.8V	3.3V
Array Pixel Count	8 \times 8	128 \times 128	10 \times 10	128 \times 128	132 \times 124
Pixel Size	175 μm \times 175 μm	15 μm \times 15 μm	300 μm \times 300 μm	7 μm \times 7 μm	20 μm \times 20 μm
Photodetector Type	CMOS photogate	n ⁺ /p-sub	p ⁺ /n-well	n ⁺ /p-sub	n-well/p-sub
Excitation Wavelength	450nm	532nm	470nm	345nm	532nm
Emission Wavelength	620nm	575nm	530nm	447nm	575nm
Peak SNR	46dB	N/A	N/A	46dB	44dB
Dynamic Range	82dB	46dB	40dB	\approx 50dB	\approx 53dB
Chip Power Consumption	8mW	26.2mW	N/A	N/A	2.37mW
Chip Output	Digital	Analog	Analog	Analog	Digital
Integrated Fluidics	PDMS	No	No	PDMS	No

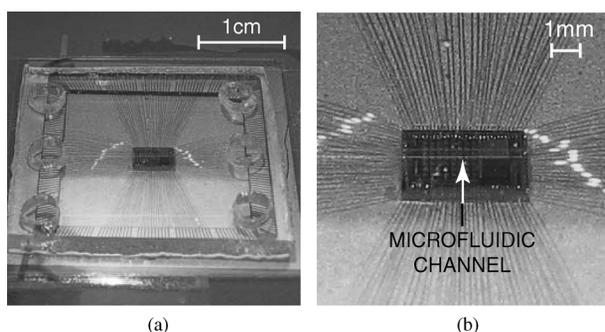


Fig. 18. Photograph of the microfluidic device placed over the CMOS sensor die: (a) overall configuration showing entire package cavity, and (b) close-up view of fluidic channel running across the CMOS die.

B. Fluorescence Contact Imaging Experimental Results

To evaluate the applicability to fluorescence imaging, the proposed microsystem is utilized to image QDs in a microfluidic device. Fig. 19 show measured results from fluorescence imaging as captured by the presented CMOS image sensor. Fig. 19(a) captures the fluorescence of 2 μm red QDs (peak emission wavelength at 620 nm) in a microfluidic channel. Since only a single color of emission is to be sensed, the CPG functions as a monochromatic detector (i.e., reconstruction is not necessary) and is set to $V_{GB} = 0$ V to maximize sensitivity. The samples have been imaged under an excitation power of approximately 0.5 mW/mm² and an exposure time of 10 sec. The presence of the fluidic network introduces light scattering, which combined with the stray LED output in the filter pass-band, resulted in a background signal of approximately 250 sensor output codes. To remove the background signal component, the background signal is subtracted from the original image to produce the result in Fig. 19(a). Fig. 19(b) depicts a background subtracted image of a spot (diameter 1 mm) of 2 μm solution of red QDs. The sample solution is directly spotted on the thin-film filter, and as a result, the sample spot is approximately 100 μm away from the detector due to the thickness of the filter. To highlight the features in the captured images, Fig. 19(a) and (b) are intensity-thresholded to produce Fig. 19(c) and (d), respectively. Fig. 19(c) highlights the fact

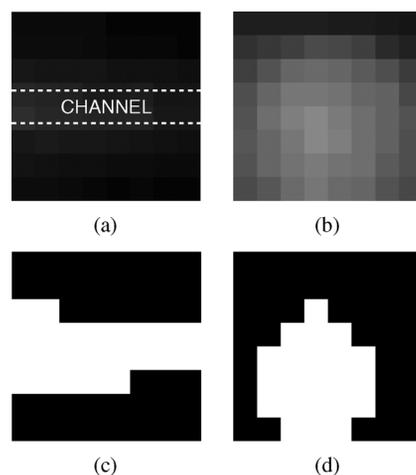


Fig. 19. Fluorescence imaging of 2 μm red quantum dot in solution phase: (a) background subtracted image of sample in a 250 μm -wide microfluidic channel, and (b) background subtracted image of 1 mm-diameter rQD spot deposited directly on the thin-film filter. (c) and (d) are intensity-thresholded images of (a) and (b), respectively.

that the fluorescence intensity is higher on the left hand side of the image. This is due to a concentration gradient of the quantum dot solution, which has been injected into the channel from the inlet located on the left of the image. Thresholding has been performed in software but can be readily implemented on-chip [5]. Table II compares the proposed work to recently reported CMOS fluorescence imaging microsystems.

It is often meaningful to characterize the detection limit by the required sample size, rather than solely by the analyte concentration [35]. Since 25 nL of sample volume has been injected into the channel with a 2 μm concentration, the microsystem is able to detect 50 fmol of rQD fluorophore. This is advantageous as fewer time-consuming polymerase chain reaction (PCR) cycles are needed to bring the concentration of the target DNA to a level that can be detected.

VIII. DISCUSSION

Spatial resolution is often traded off for SNR and DR in scientific imagers. For example, in a DNA detection biosensor,

the pixel is designed to be pitch-matched to an individual spot on a microarray [1]. The presented pixel has a large area of $175\ \mu\text{m} \times 175\ \mu\text{m}$. The rather low fill-factor of 10% is due to the inclusion of a digital counter for asynchronous self-reset operation. To improve fill factor, one approach is to implement the comparator and counter on the column level to perform synchronous reset operation, at the expense of lowered SNR due to delayed reset [36].

The requirement that the input spectra be known *a priori* as discussed in Section III-A is not a serious limitation when the sensor is applied to fluorescence sensing as the spectrum typically consists of only the emission wavelengths and these wavelengths can be made well-separated by an appropriate choice of fluorophores. The tunability of the sensor is a key advantage as this allows the detection of specific emission wavelengths from various fluorophores.

The CMOS die is housed inside a $400\text{-}\mu\text{m}$ -deep cavity within an integrated circuit package. The microfluidic network is suspended on top of the cavity, as depicted in Fig. 18(a). The total distance from the sample to the detector, including the thickness of the reservoir bottom, is approximately $300\ \mu\text{m}$. This distance leads to a reduced photon collection efficiency compared to depositing the fluorophores on the thin-film filter, which is placed directly on the CMOS die surface. This is the reason for the higher intensity in Fig. 19(b) as compared to Fig. 19(a). The distance also leads to blurring of the images. Aside from introducing optics such as microlenses to focus the image onto the photo detectors, a possible solution is to design the microfluidic device with an additional lower layer that can be extended down into the chip package cavity [37]. Thus, channels can be routed to this layer to bring the sample solution closer to the pixel array.

IX. CONCLUSION

A wide dynamic range CMOS tunable-color image sensor is presented. The sensor integrates an 8×8 array of tunable-color photogates. It exploits the wavelength-dependent optical absorption properties of the polysilicon gate to yield color discrimination on a standard digital CMOS process without an external color filter array. An analysis is presented for the asynchronous self-reset with residue readout ADC architecture where photon shot noise is taken into consideration. An implementation of this architecture is described where the coarse asynchronous self-reset operation and fine residue quantization are performed with separate circuits, on and off the array, respectively, to yield a noise-optimized design. A prototype is fabricated in a standard $0.35\ \mu\text{m}$ CMOS process and is validated in color light measurements. Contact imaging of quantum dot nanoparticles within a microfluidic channel validates the prototype in fluorescence-based analyte detection. The prototype demonstrates technologies that enable miniaturized, low-cost bio-sensing for medical diagnostics applications.

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