Roman Genov

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RESEARCH INTERESTS

Analog and digital VLSI circuits, systems and algorithms for parallel signal processing and high-performance adaptive computing with application to pattern recognition, focal-plane imaging, communications, autonomous system design, and low-power biomedical instrumentation.

EDUCATION

The Johns Hopkins University, Ph.D., Electrical and Computer Engineering, Baltimore, MD, 08/2002.
Dissertation: Massively Parallel Mixed-Signal VLSI Kernel Machines.
Advisor: Gert Cauwenberghs

Massachusetts Institute of Technology, Visiting Student, AI Lab/CBCL, Cambridge, MA, 1/99-8/99.

The Johns Hopkins University, M.S.E., Electrical and Computer Engineering, Baltimore, MD, 1998.
GPA 4.00/4.00

Rochester Institute of Technology, B.S., Electrical Engineering, Rochester, NY, 1996.
GPA 4.00/4.00, Highest Honors, Rank in class – 1/316

PROFESSIONAL EXPERIENCE

University of Toronto, Toronto, ON, 9/2002-Present
Assistant Professor, Electronics Group, Department of Electrical and Computer Engineering.

The Johns Hopkins University, Baltimore, MD, 9/96-8/2002
Research Assistant, Adaptive Microsystems Lab, Electrical and Computer Engineering Department.
Designed low-power massively parallel mixed-signal array processor chips providing 1,000 GOPS/Watt (first Support Vector Machine in silicon).
Developed multi-chip PCI parallel processing card achieving ultra-fast real-time performance in data classification (sound) and pattern recognition (image, video) tasks.
Designed and tested novel high-performance algorithmic A/D converters (with Northrop Grumman Corporation), low-power charge-mode flash converters, and parallel delta-sigma converters.
Supervised B.S. and M.S. level students in algorithm development and microchip design.

Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, 6/98-7/98.
Visiting Researcher, Autonomous Systems Lab.
Developed learning algorithms and VLSI architectures for mobile mini-robot navigation.
Investigated sensor-processor interfaces.

Xerox Corporation, Webster, NY, 3/96-8/96.
Design Engineer CO-OP, Advanced Development Team in the Color Imaging Systems Division.
Developed and designed electrical and computer systems for new generation color copiers.
Responsible for hardware-software co-design with Verilog and Xilinx FPGA tools.

Atmel Corporation, Columbia, MD, 6/95-12/95.
Design Engineer Intern, Chesapeake Design Center.
Designed, simulated and laid out digital VLSI cells. Developed a Perl extraction tool to automate creation of Verilog ASIC models from HSPICE output.

AWARDS AND HONORS

New Opportunities Award, Canadian Foundation for Innovation (CFI), 2004.
Discovery Award, Natural Sciences and Engineering Research Council of Canada (NSERC), 2002.
Best Student Paper Award, 3rd place, IEEE Midwest Symposium on Circuits and Systems (MWSCAS'2000), 2000.
Best Presentation Award, IEEE International Joint Conference on Neural Networks (IJCNN'99), 1999.
Best Student Paper Contest Finalist, IEEE International Symposium on Circuits and Systems (ISCAS'99), 1999.
American Councils for International Education Fellowship, 1994-95.

RESEARCH GRANTS AND CONTRACTS

"Intelligent Sensory Integrated Systems," R. Genov (PI), New Opportunities Award, Canadian Foundation for Innovation (CFI), Ministry of Economic Development and Trade (MEDT), and industrial sponsors, $252,000, 06/2004-05/2009.
"Real-time Human Gate Recognition for Automated Surveillance," D. Hatzinakos, K. Plataniotis, R. Genov (Co-PI), P. Klentrou, Communications and Information Technology Ontario (CITO), $226,422, 6/2004-5/2006.
"Autonomous Integrated Vision Systems," R. Genov (PI), Natural Sciences and Engineering Council of Canada (NSERC), Discovery Award, $83,400, 05/2003-04/2007.
"Mixed-Signal VLSI Circuits and Systems," R. Genov (PI), Connaught Foundation, $10,000, 10/2002.
"Mixed-Signal VLSI Circuits and Systems," R. Genov (PI), University of Toronto, ECE Dept., $100,000, 10/2002.

GRADUATE RESEARCH ADVISEES

Rafal Karakiewicz, Candidate for M.A.Sc. Degree.
Ashkan Olyaei, Candidate for M.A.Sc. Degree.
Joseph Aziz, Candidate for M.A.Sc. Degree.
Quincy Fung, Candidate for M.A.Sc. Degree.

TEACHING

"VLSI Design Methodology," ECE1388 9/2004-12/2004, 9/2005-12/2005 (26 graduate students).
"Analog Electronics," ECE530 1/2004-4/2004, 1/2005-4/2005, 1/2006-4/2006 (55-65 students).
"Introductory Electronics," ECE231 1/2003-4/2003, 1/2004-4/2004, 1/2005-4/2005, 1/2006-4/2006 (80-100 students).
"Selected Topics in Circuits and Systems – VLSI Circuits and Systems for Pattern Recognition," ECE1390 9/2003-12/2003 (5 graduate students).

INVITED PRESENTATIONS AND SHORT COURSES

"CMOS Wavelet Compression Imager Architecture," *IEEE CAS Emerging Technologies Workshop*, St. Petersburg, Russia, June 23-24, 2005.
"Kerneltron: Massively Parallel Mixed-Signal VLSI Pattern Recognition Processor," Centre for Vision Research, Toronto, ON, March 11, 2005.
"Pattern Recognition at 1GOPS/mW and Beyond: Massively Parallel Mixed-Signal VLSI Storage, Computing and Data Conversion," Microelectronics Strategic Alliance of Quebec (ReSMiQ), half-day intensive course, Montreal, QC, March 4, 2005.
"Kerneltron: Massively Parallel Mixed-Signal VLSI Pattern Recognition Processor," IEEE EDS/CAS Western New York Conference, Invited Plenary Talk, Rochester, NY, Nov. 3, 2004.
"A 1GMACS/mW Mixed-Signal Differential-Charge CID/DRAM Processor," IEEE Int. Conf. on Circuits and Systems for Communications (ICCSC'04), Invited Plenary Talk, Moscow, Russia, June 30 - July 2, 2004.
"Kerneltron: Massively Parallel Mixed-Signal VLSI Pattern Recognition Processor," Invited Seminar,

Rochester Institute of Technology, Rochester, NY, Apr. 30, 2004.

"Silicon Support Vector Machine," Neural Information Processing Systems Conference (NIPS'2003), Demonstrations track presentation, Vancouver, BC, Dec. 10, 2003.

"Kerneltron: Support Vector 'Machine' in Silicon," VLSI Seminar Series, School of Electrical and Computer Engineering, Cornell University, Ithaca, NY, Nov.13, 2003.

"Massively Parallel Mixed-Signal VLSI Kernel Machines," Seminar Series, Division of Engineering, Brown University, Providence, RI, Feb.25, 2002.

"Massively Parallel Mixed-Signal VLSI Kernel Machines," Seminar Series, Department of Electrical and Computer Engineering, McGill University, Montreal, QC, Feb.19, 2002.

"Massively Parallel Mixed-Signal VLSI Kernel Machines," Seminar Series, Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Feb.11, 2002.

"VLSI Array for Massively Parallel Kernel Computation," Workshop on Neuromorphic Engineering, Telluride, CO, July 2001.

"Q-Learning: Experiments on Microrobots," Neural Information Processing Systems (NIPS'1999) workshop "Learning Chips and Neurobots," Breckenridge, CO, Dec. 1998.

PROFESSIONAL ACTIVITIES

Society Membership: IEEE (Institute of Electrical and Electronic Engineers), Circuits and Systems (CAS) Society, Solid-State Circuits (SSC) Society, Engineering in Medicine and Biology (EMB) Society.

Technical Committee Membership: Neural Systems and Applications of IEEE CAS Society, Biomedical Circuits and Systems of IEEE CAS Society, Sensory Systems of IEEE CAS Society.

Conference Program Committees:

Review Committee Member, IEEE Int. Symp. Circuits and Systems (ISCAS'2003, 2004, 2005).
Technical Program Committee Member, Great Lakes Symposium on VLSI (GLSVLSI'2003).
Program Committee Member, SPIE Bioengineered and Bioinspired Systems Conference (Bio'2003, 2005).

Conference Session Chair/Co-chair:

IEEE Int. Symp. Circuits and Systems, "Self-Correcting ADC," (ISCAS'2002); "VLSI Implementation of Neural Networks and Systems," (ISCAS'2003, cancelled); "Neural Systems and Applications," (ISCAS'2004).

SPIE Int. Symp. Microtechnologies, Bioengineered and Bioinspired Systems 2003, "Biosensors."

External Advisory Committee Member, Department of Electrical Engineering, Rochester Institute of Technology, 2004-current.

Journal and Conference Reviews:

IEEE Transactions on Circuits and Systems II (TCAS-II); IEEE Transactions on Neural Networks (TNN); IEEE Int. Symp. on Circuits and Systems (ISCAS); Great Lakes Symposium on VLSI (GLSVLSI); Applied Soft Computing Journal.

High-Technology Entrepreneurship Interactive Program, The Johns Hopkins University, 1999.

Tau Beta Pi Engineering Future, Leadership and Technical Management Interactive Workshop, 1998.

IEEE Johns Hopkins University Chapter Treasurer, 1997.

REFEREED JOURNAL PUBLICATIONS

"Dynamic MOS Sigmoid Array Folding Analog-to-Digital Conversion," R. Genov and G. Cauwenberghs, *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 51 (1), pp. 182-186, 2004.

"Silicon Support Vector Machine with On-Line Learning," R. Genov, S. Chakrabartty, G. Cauwenberghs, *Int. Journal of Pattern Recognition and Artificial Intelligence*, vol. 17 (3), pp. 385-404, 2003.

"Kerneltron: Support Vector 'Machine' in Silicon," R. Genov, G. Cauwenberghs, *IEEE Trans. on Neural Networks*, vol. 14 (5), pp. 1426-1434, Sept. 2003.

"Charge-Mode Parallel Architecture for Matrix-Vector Multiplication," R. Genov, G. Cauwenberghs,

IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing, vol. 48 (10), pp. 930-936, Oct. 2001.

REFEREED CONFERENCE PUBLICATIONS

"CMOS Haar Wavelet Sensory Parallel Processor Architecture," A. Olyaei, R. Genov, *SPIE Photonics North*, Toronto, Canada, Sept. 12-14, 2005.

"Multi-Channel Integrated Neural Interfaces for Distributed Electro-Chemical Sensing," J. Aziz, R. Genov, *Midwest Symposium on Circuits and Systems (MWSCAS'05)*, Cincinnati, Ohio, Aug. 7-10, 2005.

"Mixed-Signal CMOS Haar Wavelet Compression Imager Architecture," A. Olyaei, R. Genov, *Midwest Symposium on Circuits and Systems (MWSCAS'05)*, Cincinnati, Ohio, Aug. 7-10, 2005.

"CMOS Wavelet Compression Imager Architecture," A. Olyaei, R. Genov, *IEEE CAS Emerging Technologies Workshop*, St. Petersburg, Russia, , June 23-24, 2005 (invited).

"Minimal Activity Mixed-Signal VLSI Architecture for Real-Time Linear Transforms in Video," R. Karakiewicz and R. Genov, *IEEE Int. Symp. on Circuits and Systems (ISCAS'2005)*, Kobe, Japan, May 23-26, 2005.

"A 1GMACS/mW Mixed-Signal Differential-Charge CID/DRAM Processor," R. Genov, *IEEE Int. Conf. on Circuits and Systems for Communications (ICCSC'2004)*, Moscow, Russia, June 30 - July 2, 2004 (invited).

"Integrated Multi-Electrode Fluidic Nitric-Oxide Sensor and VLSI Potentiostat Array," M. Naware, A. Rege, R. Genov, M. Stanacevic, G. Cauwenberghs, N. Thakor, *IEEE Int. Symp. on Circuits and Systems (ISCAS'2004)*, Vancouver, Canada, May26-29, 2004.

"VLSI Multi-Channel Track-and-Hold Potentiostat," R. Genov, M. Stanacevic, M. Naware, G. Cauwenberghs, N. Thakor, in *Microtechnologies for the New Millennium, Bioengineered and Bioinspired Systems 2003*, Proc. SPIE vol. 5119, May 2003.

"Algorithmic Partial Analog-to-Digital Conversion in Mixed-Signal Array Processors," R. Genov, G. Cauwenberghs, *Proc. IEEE Int. Symp. on Circuits and Systems (ISCAS'2003)*, Bangkok, Thailand, May 25-28, 2003.

"A 5.9mW 6.5GMACS CID/DRAM Array Processor," R. Genov, G. Cauwenberghs, G. Mulliken, and F. Adil, *Proc. European Solid-State Circuits Conference (ESSCIRC'2002)*, Florence, Italy, Sept. 24-26, 2002.

"Kerneltron: Support Vector 'Machine' in Silicon," R. Genov, G. Cauwenberghs, *Proc. SVM'2002*, Lecture Notes in Computer Science, Niagara Falls, ON, Aug. 10, 2002.

"Delta-Sigma Algorithmic Analog-to-Digital Conversion," G. Mulliken, F. Adil, G. Cauwenberghs, and R. Genov, *Proc. IEEE Int. Symp. on Circuits and Systems (ISCAS'2002)*, Phoenix, AZ, May 26-29, 2002.

"Charge-Based MOS Correlated Double Sampling Comparator and Folding Circuit," R. Genov and G. Cauwenberghs, *Proc. IEEE Int. Symp. on Circuits and Systems (ISCAS'2002)*, Phoenix, AZ, May 26-29, 2002.

"Neuromorphic Processor for Real-Time Biosonar Object Detection ," G. Cauwenberghs, R. T. Edwards, Y. Deng, R. Genov, and D. Lemonds, *Proc. IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP'2002)*, Orlando, FL, May 13-17, 2002.

"Stochastic Mixed-Signal VLSI Architecture for High-Dimensional Kernel Machines," R. Genov, G. Cauwenberghs, *Advances in Neural Information Processing Systems (NIPS'2001)*, Cambridge, MA: MIT Press, vol. 14, 2002.

"CID/DRAM Mixed-Signal Parallel Distributed Array Processor," R. Genov, G. Cauwenberghs, *14th International IEEE ASIC/SOC Conference (ASIC/SOC'2001)*, Washington, DC, Sept. 12-15, 2001.

"Embedded Dynamic Memory and Charge-Mode Logic for Parallel Array Processing," R. Genov, G. Cauwenberghs, *Proc. of the 5th World Multi-Conference on Systemics, Cybernetics and Informatics (SCI'2001)*, Orlando, FL, July 22-25, 2001. (*Best Paper Award*.)

"Massively Parallel Inner-Product Array Processor," R. Genov, G. Cauwenberghs, *Proc. of Int. Joint Conference on Neural Networks (IJCNN'2001)*, Washington, DC, July 15-19, 2001.

"Analog Array Processor with Digital Resolution Enhancement and Offset Compensation," R. Genov, G. Cauwenberghs, *Proc. of Conference on Information Sciences and Systems (CISS'2001)*, Baltimore, MD, March 21-23, 2001.

"Charge-Mode Parallel Architecture for Matrix-Vector Multiplication," R. Genov and G. Cauwenberghs, *Proc. of 43rd IEEE Midwest Symposium on Circuits and Systems (MWSCAS'2000)*, Lansing, MI, Aug. 8-11, 2000. (*Best Student Paper Award*, 3rd place.)

"Learning to Navigate from Limited Sensory Input: Experiments with the Khepera Microrobot," R. Genov, S. Madhavapeddi and G. Cauwenberghs, *Proc. of International Joint Conference on Neural Networks (IJCNN'99)*, Washington, DC, vol. 3, pp. 2061-2064, 1999. (*Best Presentation Award.*)

"16-Channel Single-Chip Current-Mode Track-and-Hold Acquisition System with 100 dB Dynamic Range," R. Genov and G. Cauwenberghs, *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS'99)*, Orlando, FL, vol. 6, pp. 350-353, 1999. (*Best Student Paper Contest Finalist.*)

PATENTS

"High-Precision Matrix-Vector Multiplication on a Charge-Mode Array with Embedded Dynamic Memory and Stochastic Method Thereof," R. Genov and G. Cauwenberghs, patent pending, 2003.

"Multi-Site Sensory Signal Acquisition, Processing and Classification, and Electronic Method Thereof," R. Genov, patent pending, May 2005.

"An Implantable Intelligent Neural Activity Acquisition, Processing and Stimulation System," B.L Bardakjian, R. Genov, P.L. Carlen, M. Derchansky, patent pending, June 2005.