ECE 1388 2016 VLSI Design Methodology (tentative)

Overview: VLSI circuits and systems design methodology in deep submicron CMOS technologies using advanced CAD tools.

Schedule: Tuesday 3 - 5 pm
Location: ES-B149
Home page: http://www.eecg.utoronto.ca/~roman/teaching/1388/2015/main.html
Instructor: Roman Genov Office: Bahen 5142 E-mail: roman_at_eecg.utoronto.ca
Textbook: Weste and Harris, CMOS VLSI Design: A Circuit and Systems Perspective, 4th edition, Addison Wesley, 2011.

Pre-requisites
An undergraduate course on CMOS circuit design, and basic understanding of UNIX.

Lecture topics covered:

- The lectures serve to review basic digital circuit design topics as needed to complete all projects in the course:
    1. Introduction to MOS Transistors and to Digital Circuits
    2. Layout and Fabrication
    3. CMOS Transistor Theory
    4. Non-Ideal Transistors
    5. DC & Transient Response
    6. CMOS Processing Technology
    7. Design for Optimum Speed: Logical Effort
    8. Design for Low Power
    9. Interconnect and Wire Engineering
    10. Packaging, Power and I/O

Lab topics covered:

- There are 4 take-home labs. VLSI User's Manual is the basis for the labs as follows:
    1. Introduction. Cadence: A Beginner's Guide and Schematic Entry (Ch. 1-3)
    2. Cadence: Physical Layout and Analog Simulation (Ch. 4-5)
    3. Cadence: Digital Simulation with Hardware Description Languages (Ch. 6)
    4. Synopsis and Cadence: Logic Synthesis and Optimization; Place and Route (Ch. 7-8)
- The lab sequence is intended to gradually expose students to CAD tools design environments in order to complete the projects.
- TAs will answer questions by email

Tutorial topics covered:

- The mandatory-attendance tutorials provide intensive training in the use of CAD tools:
    1. Cadence Virtuoso Schematic Editor
    2. Cadence Virtuoso Layout Editor
    3. Layout of Parameterized Cells (P-cells)
    4. Digital Design Flow, from Synthesis to Place-and-route

5. Verilog-A Language
6. Mixed-signal Simulations within Cadence Virtuoso AMS Environment

Course Projects

- The three course projects will be based on the labs, tutorials and textbook as follows:
    1. Device and Circuit Characterization and Basic Layout (Design Example: CMOS Transistor and Inverter)
    2. Digital Circuit and Layout Design for Optimum Performance (Design Example: 5-bit Register Decoder)
    3. Digital Circuit Synthesis and Layout Place-and-Route (Design Example: 4x4-bit Unsigned Array Multiplier)

Final Project

- The final project guides student teams through a simplified practical flow of a complete integrated circuit (IC) design starting from the project definition and system outline to the complete verified IC layout including a padframe. The project aims to help students apply skills learned in this course and other courses to the design of a die-level CMOS integrated circuit. The default final project topic is the Design of a CMOS Image Sensor Integrated Circuit. Some students may choose a different topic, subject to limitations.

- The final project runs in weeks 7-14 with the following weekly milestones:
    1. Group formation and project definition (Oral presentation)
    2. System outline (Written update)
    3. Circuit cells and simulations (Written update)
    4. Complete schematic (Written update)
    5. Cell layout (Written update)
    6. Complete layout within a pad frame (Oral presentation)
    7. LVS final check (Final report)

- The goal of the project is for students to develop/polish and demonstrate a number of skills including but not limited to:
    1. Understanding and mastery of the IC design flow
    2. Knowledgeable utilization of all lecture material within the final project
    3. Performing optimal circuit and layout design as part of an IC design flow
    4. Demonstrated ability to work efficiently within an IC design team
    5. Ability to communicate results effectively by way of two oral presentations
    6. Understanding all presentations and participation by asking/answering questions

- Previous years final project web reports are available here 2004 , 2006.

Grade breakdown

Course projects	30%
Final project	60%
Class participation	10%