2D Numerical Investigation of the Impact of Compositional Grading on the Performance of Submicrometer Si–SiGe MOSFET's

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Abstract—**Computer simulation is used to establish the impact of design parameters on the subthreshold characteristics, hot carrier injection, and high frequency performance of Si–SiGe FET's. The results indicate that by fully grading the Ge content in the channel of a MOSFET, short channel effects are reduced and high frequency performance is improved as compared to devices with uniform Ge channels. A cutoff frequency of 38 GHz and a maximum frequency of oscillation of 160 GHz are predicted for fully graded p-channel MOSFET's with 0.25 μm gate lengths. Energy balance simulation reveals that hot carrier injection at the Si–SiO_2 interface is considerably suppressed if a fully graded channel is employed.**

I. Introduction

CONSIDERABLE effort has been dedicated to the SiGe–Si heterostructure system as a promising vehicle to implement bandgap engineering concepts in the technologically mature silicon environment [1], [2]. Si–SiGe HBT's have already proved that the performance bounds of Si bipolar transistors can be pushed beyond the limits envisioned only a few years ago [3]. Developments over the last decade have also demonstrated that high speed FET action can be achieved with both type I and type II Si–SiGe heterostructure alignments, employing either Schottky or MOS gates [4]–[9].

Record-breaking electron and hole mobilities have so far been the exclusive domain of Schottky-gate controlled modulation-doped FET's (MODFET's) [10]–[12]. Recently reported Si–SiGe p-channel MOSFET's [13] and [14] have demonstrated hole mobilities higher than in Si devices but well below those measured in MODFET's. This discrepancy is partly due to the quality of the Si–SiO_2 interface and its proximity to the SiGe channel but is also due to the much higher Ge mole fractions, 0.8–1, typical of type II p-MODFET's. More experimental work is required to elucidate this problem. At least from the theoretical point of view, hole mobilities in buried heterojunction MOSFET channels should be comparable to those in Schottky gate devices.

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Since the performance of state of the art Si p-MOSFET's lags behind that of n-MOSFET's, upgrading the p-channel device requires more urgent attention. The focus of this study will therefore be on Si–SiGe p-FET's. Where appropriate, reference will be made to recent Si–SiGe n-MODFET results [9].

Most of the experimental work on Si–SiGe FET's has been carried out on devices with channel lengths greater than 0.25 μm. It is critical for the future prospects of Si-based heterostructure IC's that their performance edge be maintained as the dimensions shrink to 0.1 μm and beyond. In the deep submicrometer realm, nonlocal transport effects play a significant role, and a meaningful attempt to predict device behavior ultimately requires their inclusion. To date, such studies have been hindered by the complexity of the numerical modeling problem and by the scarcity of experimental data referring to the transport properties of SiGe. In the investigation of hot carrier injection in MOSFET's, the temperature of both electrons and holes must be monitored.

The purpose of this paper is to 1) propose a fully compositionally graded SiGe channel concept as leading to the best performance in deep submicrometer MOS devices, 2) quantify the high frequency performance of Si–SiGe FET's, and 3) estimate the impact of compositional channel grading on hot carrier and short channel effects.

The paper is organized as follows. The second section describes the numerical model employed in the study of submicrometer heterostructure devices. Section III discusses present Si–SiGe FET concepts and proposes an optimized structure with a fully graded SiGe channel. Section IV presents simulation results on the dc characteristics and on the high frequency performance of graded- and uniform-channel Si–SiGe p-MOSFET's. The influence of Ge compositional grading on hot carrier injection is assessed based on energy balance simulations. The scaling potential of fully graded channel Si–SiGe MOSFET's is demonstrated in Section V for channel lengths as small as 0.06 μm. Finally, in Section VI, conclusions are drawn regarding the prospect of Si–SiGe FET's for low-voltage, high-speed digital and analog applications.

II. Numerical Models

The ATLAS/BLAZE 2D heterostructure device simulator [15] is used to analyze type I and type II graded and abrupt heterostructures. Both the conventional Drift-Diffusion (DD),

and the more sophisticated Energy Balance (EB) model, which accounts for nonlocal transport effects, were employed for simulations of the dc characteristics. Frequency domain performance was simulated using the DD model. The EB model for semiconductor devices with nonuniform bandgap [16] and [17] is obtained by combining the approach proposed by Stratton for Si devices [18], with the DD heterojunction model as developed in [19] and [20]. The system of five independent semiconductor equations is solved with potential Ψ, electron and hole concentrations n and p, and electron and hole temperatures T_n and T_p, as variables.

A. Mobility and Ionization Models

In the case of DD simulations a field dependent mobility model is employed for $Si_{1-x}Ge_x$:

$$\mu_p(E) = \frac{\mu_{op}}{1 + \frac{\mu_{op}E}{v_{sp}}}$$
$$\mu_n(E) = \frac{\mu_{on}}{\left[\left(1 + \left(\frac{\mu_{on}E}{v_{sn}}\right)^2\right)\right]^{1/2}} \quad (1)$$

where E is the electric field parallel to the heterointerface, and v_{sn} and v_{sp} are the saturation velocities of electrons and holes.

In EB simulations carrier mobilities are expressed as functions of the local carrier temperatures:

$$\mu_p(T_p) = \frac{\mu_{op}}{1 + \alpha_p(T_p - T_o)}$$
$$\mu_n(T_p) = \frac{\mu_{on}}{[1 + \alpha_n^2(T_n - T_o)^2]^{1/2}} \quad (2)$$

where

$$\alpha_p = \frac{3}{2}\frac{k_B\mu_{op}}{qv_{sp}^2\tau_{mp}} \qquad \alpha_n = \frac{3}{2}\frac{k_B\mu_{on}}{qv_{sn}^2\tau_{mn}}$$

and $\tau_{mn} = \tau_{mp} = 0.4$ ps in both Si and SiGe.

The low-field mobility values in undoped SiGe are derived from experimental data [9], [13], [21]–[23]. The low-field hole mobility in undoped $Si_{0.5}Ge_{0.5}$ is assumed to be 40% higher than in $Si_{0.75}Ge_{0.25}$ [22]. The saturation velocities in SiGe are set equal to those in Si, in accordance with experimental [12], [24] and Monte Carlo simulation results [25], [26].

The temperature dependent impact ionization is calculated based on the model proposed in [27]:

$$G = A_n|J_n|\exp\left(-\frac{T_{ncr}}{T_n}\right) + A_p|J_p|\exp\left(-\frac{T_{pcr}}{T_p}\right) \quad (3)$$

where

$$T_{ncr} = \frac{2}{3}\frac{qv_{sn}\tau_{in}}{k_B}E_{ncr} \qquad T_{pcr} = \frac{2}{3}\frac{qv_{sp}\tau_{ip}}{k_B}E_{pcr}$$

and $\tau_{in} = \tau_{ip} = 0.4$ ps in both Si and SiGe.

Other Si and SiGe material parameters were taken from [28] and [29].

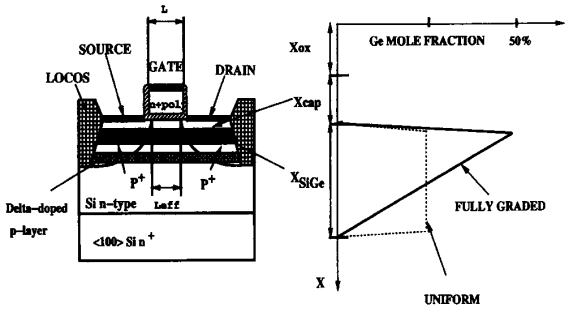

Fig. 1. Layer structure of the proposed type I graded $Si/Si_{1-x}Ge_x$ p-channel MOSFET.

III. Device Structures

The layer structure of a Si–SiGe p-MOSFET is shown in Fig. 1. Typical Type I, 2-Dimensional Hole Gas (2DHG) Si–SiGe FET's feature a thin, undoped SiGe film with uniform composition as the conductive, buried channel. The film is separated from the gate oxide by an undoped Si cap. Because the bandgap difference between Si and SiGe is almost entirely accommodated in the valence band, the thin (100–150 Å) SiGe film forms a rectangular quantum well for holes. A 50–100 Å thick p-type δ-doped region is inserted immediately below the channel, in the Si substrate, to adjust the threshold voltage[1] [1], [14]. It also helps to maximize the number of carriers in the channel over a wider range of gate voltages [30]. The effective hole velocity is determined by the parallel transport properties of the semiconductor material in which the channel is formed and by the quantum distribution of mobile charge along the direction perpendicular to the gate. In order to take full advantage of the transport properties of the quantum channel, conduction in the Si layers, especially in the cap layer, must be minimized.

Besides the ubiquitous gate length reduction, maximizing the transconductance of an FET requires that the gate-to-channel spacing be maximized and that the effective velocity of the free carriers in the channel be maximized. The reduction of the gate to channel spacing is also instrumental in suppressing short channel effects. In order to improve the cutoff frequency, the effective velocity needs to be maximized.

The gate-to-channel spacing has three components: the gate oxide thickness t_{ox}, the thickness of the silicon cap layer t_{ca}, and the gate-voltage-dependent distance between the channel/cap interface and the position of the charge centroid in the channel $\Delta t(V_{GS})$. Minimum practical limits of t_{ox} and t_{ca} are around 30 Å [32] and 50 Å, respectively. These are comparable to the value of $\Delta t(V_{GS})$, which, under normal operating conditions, varies between 10 and 80 Å, depending on the energy bands profiles in the channel.

The effective velocity of carriers in the channel can be improved by employing a large Ge mole fraction in the channel and by increasing the number of carriers in the SiGe channel. The placement of the δ-doped film or of an

[1] As shown recently [31], one can control the charge distribution also by inserting an insulating layer (such as SIMOX) immediately below the channel.

insulating layer beneath the channel has a negative impact on $\Delta t(V_{GS})$, because carriers will be accumulated at the bottom of the channel. In deep submicrometer devices, this leads to transconductance degradation and to a large subthreshold slope.

An improved solution is proposed here, whereby the δ-doped region is maintained to control the threshold voltage, but its negative impact on transconductance is eliminated by engineering the Ge mole fraction in the channel so that $\Delta t(V_{GS})$ is minimized over the entire bias range. As suggested earlier [30], full compositional grading can be employed to simultaneously maximize the velocity of holes in the channel and reduce the gate to 2DHG spacing. This is possible if the Ge concentration is linearly ramped up toward the gate, from 0% to 50% over 120 Å. As a result of the composition gradient, an electric field is induced in the channel. This field is directed from the substrate toward the gate, and pushes the holes closer to the gate, where the Ge mole fraction and mobility are highest. The energy band diagrams of the uniform, and of the proposed fully graded $Si_{1-x}Ge_x$ channels are shown in Figs. 2(a) and 2(b), respectively. In both cases the average Ge mole fraction is 0.25, but it peaks at 0.5 in the graded channel device.

Besides improving mobility, the large Ge mole fraction near the top of the channel provides a larger barrier in the path of the high energy holes that try to transfer from the SiGe channel to the Si cap layer. The expected outcome is a performance leverage over a wider range of gate voltages as compared to Si or uniform channel Si–SiGe devices, and suppressed hot carrier injection. High Ge mole fractions are typically accompanied by larger lattice mismatch and more dislocations. However, a fully graded channel device alleviates this problem by maintaining a relatively small integrated Ge dose, while offering enhanced carrier confinement and faster parallel transport. The feasibility of this graded Ge profile has recently been demonstrated in MOS capacitor experiments [33].

The 0.25 μm p-channel MOSFET Type I structures investigated in this study consist of (from substrate to the top gate oxide): an n-type Si substrate doped 6×10^{17} cm^{-3}, a 8 nm thick p-type Si layer δ-doped 2×10^{18} cm^{-3}, an undoped 5 nm thick Si buffer, an undoped 15 nm thick $Si_{1-x}Ge_x$ channel, an undoped 5 nm thick Si cap layer and a 5 nm gate oxide. The Ge concentration in the channel is either uniform at 25%, or graded from 0% at the bottom to 50% over 12 nm and then back to 0%, over 3 nm, at the top of the channel, as shown in Fig. 2(b). All abrupt heterojunctions are graded over 30 Å. In both cases the average Ge concentration is low enough (25%) to avoid strain relaxation. The lateral diffusion in the source and drain regions is assumed to be 0.05 μm. For other nominal gate lengths, the doping profile and the gate oxide thickness are scaled. The rest of the structural parameters are left unchanged.

IV. Simulation Results

In order to verify the credibility of the mobility model, simulation results are compared in Fig. 3 with recent

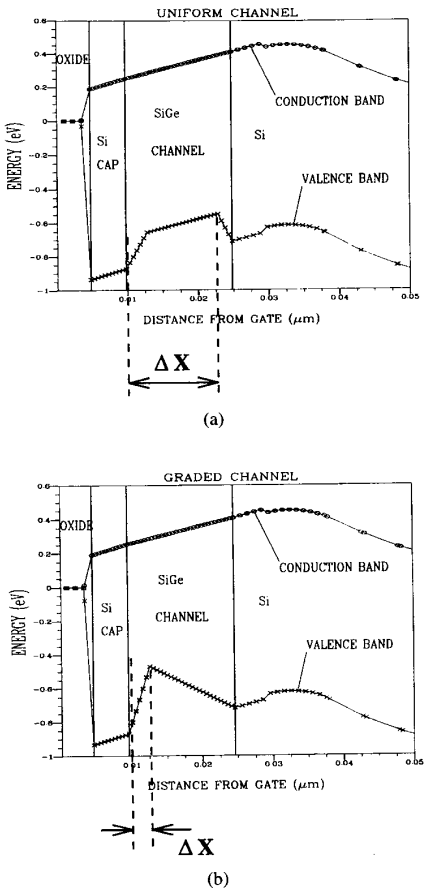

Fig. 2. Energy bands (a) of the uniform SiGe channel device, and (b) of the proposed fully graded SiGe channel $Si/Si_{1-x}Ge_x$ p-MOSFET.

transconductance data measured in long channel Si–SiGe p-MOSFET's with uniform and graded Ge channels. The validity of the Drift-Diffusion model for short channel devices was also tested on the transconductance characteristics of a submicrometer 20% Ge p-MOSFET [13], as shown in Fig. 4. These results appear to indicate that the DD model may be applied to effective channel lengths as short as 0.25 μm.

A. DC Characteristics

Fig. 5 illustrates the transfer characteristics of a fully graded SiGe channel p-MOSFET with 0.25 μm nominal gate length. Both DD and EB balance simulation results are plotted for the sake of comparison.

In the subthreshold region, since very small currents and gate voltages are involved, the DD and EB results are in very close agreement, indicating that the scaling problem can be reliably addressed with conventional modeling techniques. This situation is maintained at moderate current levels, slightly above threshold. It is only at high gate voltages that the DD model underestimates the drain current. The relatively small subthreshold slope (90 mV/decade) is an indication

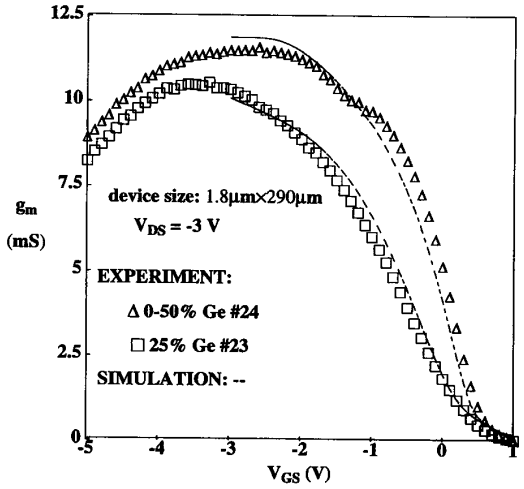

Fig. 3. Measured and simulated transconductance characteristics for uniform 25% Ge and graded 0–50% Ge channel p-MOSFET's. The low field mobility is 250 cm^2/Vs and 400 cm^2/Vs for the uniform and graded devices, respectively. The drift diffusion model was used in simulations.

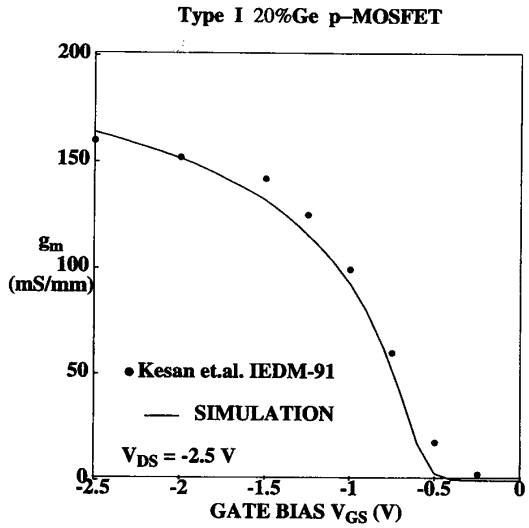

Fig. 4. Measured and simulated transconductance characteristics for 20% Ge channel p-MOSFET's. The nominal gate length is 0.4 μm. The drift diffusion model was employed in simulations.

that source-drain punch-through does not occur and that the substrate doping is suitable for this gate length. The threshold voltage shifted by 50 mV when the drain voltage was changed from -0.1 V to -2.5 V. From a qualitative point of view, the dc characteristics of the graded SiGe channel p-MOSFET are similar to those of uniform channel devices. It is in the high frequency performance that its superior performance becomes apparent.

B. High Frequency Performance

Frequency domain perturbation analysis [34] was employed to predict the small signal equivalent circuit, including the transconductance and the output conductance. The frequency dependence of the S parameters, and from it, those of the current gain h_{21} and of the unilateral power gain $GU_{\max}$ were calculated. f_T and $f_{\max}$ were determined according to their definition, without extrapolation, from the simulated $h_{21}(f)$ and $GU_{\max}(f)$ characteristics. The gate resistance R_g was modeled as a lumped resistor in series with the intrinsic gate terminal. The effect of the source resistance R_s was inherently accounted for in the 2D device structure.

Si–SiGe p-MOSFET's with uniform Ge concentration in the channel and with a fully compositionally graded channel were simulated. Transconductance versus gate voltage and cutoff frequency versus gate voltage characteristics are plotted for these devices in Figs. 6 and 7. To assess the impact of velocity saturation on transconductance and cutoff frequency, structures with 0.25 μm, 0.5 μm, 1 μm, and 2 μm gate lengths were investigated. Devices with compositional grading exhibit a sharper channel turn-on, immediately above threshold, and higher transconductance and cutoff frequency. This steep increase in transconductance and cutoff frequency is due to the higher mobility at the top of the graded channel and to the electric field induced by the compositional grading.

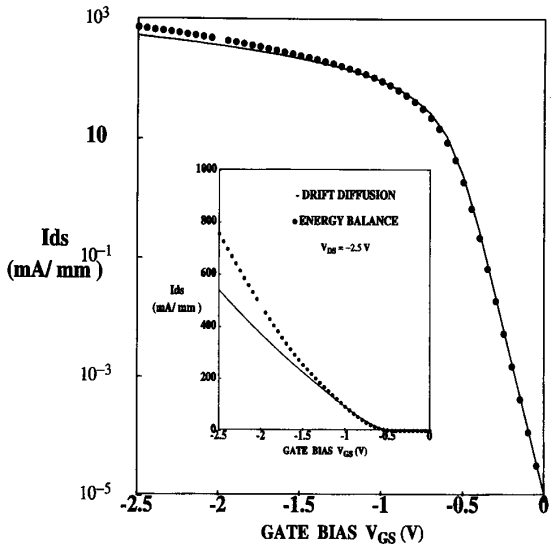

Fig. 5. Transfer and subthreshold characteristics for graded (0%–50%) Ge channel p-MOSFET's calculated with the drift diffusion (dotted line) and the energy balance (solid line) models.

For MOSFET's with 0.5 μm linewidths, the advantage of compositional grading is maintained throughout the investigated gate voltage range. The speed and gain improvements diminish as the device dimensions shrink. In the case of the 0.25 μm MOSFET's, the superiority of the graded channel is lost at gate voltages beyond -1.75 V when, regardless of the compositional profile in the channel, transconductance and cutoff frequency saturate at 350 mS/mm and 38 GHz, respectively. This is due to the fact that saturation velocity, rather than mobility, limits peak g_m and f_T. For linewidths

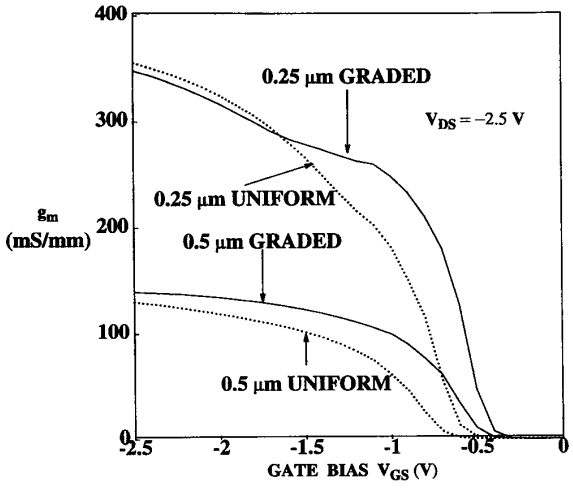

Fig. 6. Transconductance versus gate voltage for graded (0%–50%) Ge, and uniform 25% Ge channel p-MOSFET's, calculated using the drift diffusion model.

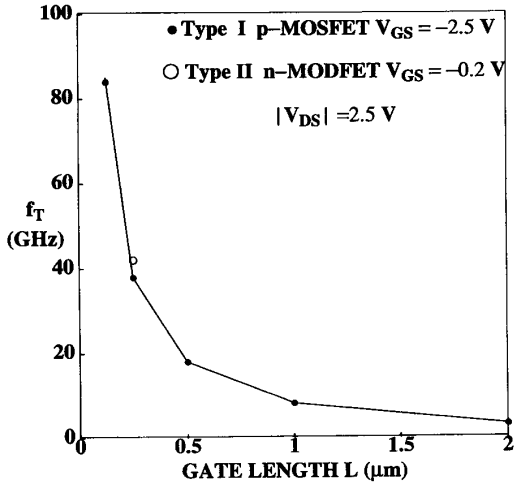

Fig. 8. Cutoff frequency versus nominal gate length for graded (0%–50%) Ge channel p-MOSFET's. Results are also shown for the type II n-MODFET of [9]. The drift diffusion model was employed in simulations.

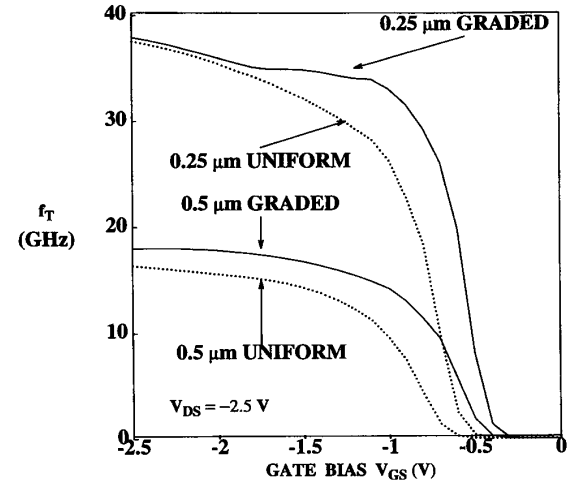

Fig. 7. Drift-Diffusion simulated cutoff frequency versus gate voltage for graded (0%–50%) Ge, and uniform (25% Ge) channel p-MOSFET's.

around or below 0.25 μm, simulation results indicate that, if mobility values are unchanged, the maximum transconductance and cutoff frequency scale linearly with the value of the saturation velocity in the SiGe channel. However, even for a 0.25 μm technology, full compositional grading, with its sharp turn-on, is beneficial in low-voltage and low-power applications.

Compositional grading was also found to reduce the output conductance in the saturation region. As a consequence, the low-frequency intrinsic voltage gain g_m/g_{ds} of the 0.5 μm device increased from 23 (uniform Ge channel) to 32 (graded Ge channel). For large gate voltages, the voltage gain of the 0.25 μm MOSFET's reduces to 25, regardless of the Ge profile in the channel. This is due to the fact that, in this bias range, most of the conduction takes place in the cap layer, which is identical in the two structures.

Fig. 8 summarizes data referring to the dependence of the cutoff frequency of graded channel MOSFET's on the gate length. For the sake of comparison, the simulated cutoff frequency of a recently reported type II n-MODFET [9] is also shown. The predicted cutoff frequency of the graded SiGe channel p-MOSFET is only slightly below that of the type II n-MODFET of identical linewidth (38 GHz as opposed to 42 GHz). This casts a favorable light on the prospect of CMOS technology in which the n and p channel devices have matched dc and ac characteristics.

Next, the impact of the gate resistance on the maximum frequency of oscillation was investigated. If the contribution of the gate resistance is neglected, $f_{\max}$ is about one order of magnitude larger than f_T. However, when a realistic gate resistance R_g is considered, the maximum frequency of oscillation is severely degraded, as illustrated in Fig. 9. The degradation is exacerbated as the device dimensions shrink and, as a result, $f_{\max}$ may become smaller than f_T,[2] for gate lengths below 0.1 μm. The reduction of R_g will be a major problem in deep submicrometer CMOS technology and metal, or metal-reinforced polysilicon gates [35] will have to used in conjunction with multiple-finger layout geometries in order to attenuate its impact on $f_{\max}$.

C. Hot Carrier Injection

Energy Balance simulations were performed in order to assess the impact of nonlocal transport effects and carrier heating on the dc characteristics of 0.25 μm Si–SiGe p-MOSFET's. It was found that, for $V_{DS} = -2.5$ V and $V_{GS} = -2.5$ V, the temperature of the hot holes at the drain end of the channel was similar in graded and uniform channel devices. However, the temperature of holes residing in the Si

[2] f_T is not affected by the gate resistance R_g.

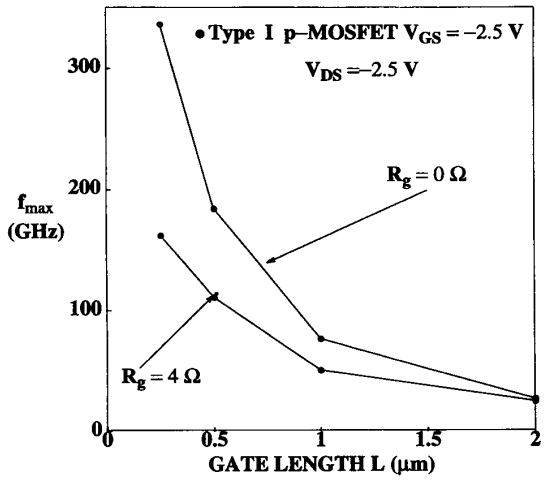

Fig. 9. Maximum frequency of oscillation versus gate length for graded (0%–50%) Ge channel p-MOSFET's with the gate resistance as variable parameter. The drift diffusion model was employed in simulations.

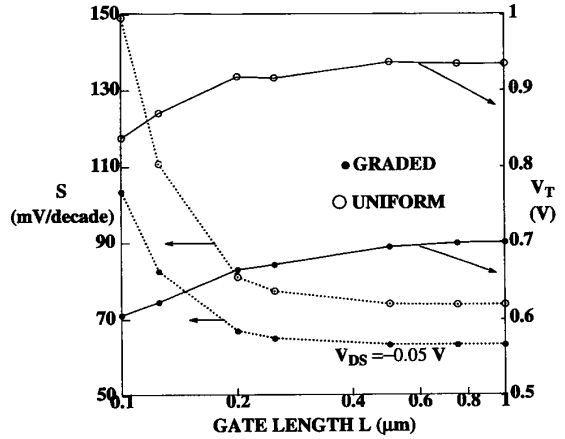

Fig. 11. Threshold voltage and subthreshold slope dependence on the feature size for graded (0%–50%) Ge, and uniform 25% Ge channel p-MOSFET's. The vertical structure was optimized for 0.125 μm gate length.

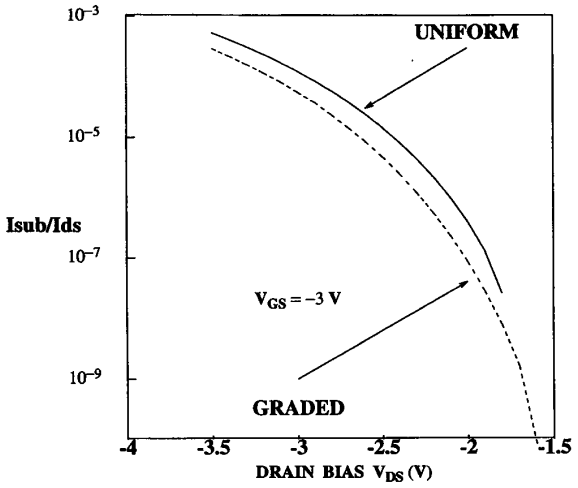

Fig. 10. The ratio of the substrate and drain currents in compositionally graded (0%–50%) Ge, and uniform 25% Ge channel p-MOSFET's with 0.25 μm linewidth. The results were obtained using energy balance simulations.

cap layer was 2500 K in the compositionally graded device and 4000 K in the uniform one. This confirms that the higher valence band energy barrier between the graded channel and the Si cap limits hot carrier injection in the cap layer and in the oxide. Additional evidence to support the suppressed hot carrier injection in the compositionally graded p-MOSFET is provided by the ratio of the substrate and drain currents. Fig. 10 shows this ratio as a function of the drain voltage. A factor of two improvement is observed for the graded device at high drain bias. The shape of the characteristics is similar to that experimentally observed in Si MOSFET's [36].

In general, a comparison between DD and EB simulation results suggests that the impact of hot carrier transport on the dc and high frequency characteristics of Si–SiGe MOSFET's is more significant than in Si–SiGe HBT's [37] and cannot be overlooked for linewidths below 0.25 μm.

V. Scaling Limits of Heterostructure Si–SiGe MOSFET's

As pointed out recently [38], the threshold voltage V_T and the subthreshold slope S are critical parameters in estimating the scaling limits of field effect transistors. Unlike predicting the cutoff frequency, which becomes problematic below 0.25 μm gate lengths due to lack of reliable transport parameters for SiGe, V_T, and S can be accurately determined from both DD and EB simulations. Therefore, it is justifiable to investigate the threshold voltage and subthreshold slope of devices scaled down below 0.25 μm.

Fig. 11 presents the threshold voltage's dependence on the gate length for a Si–SiGe p-MOSFET structure which was optimized for 0.125 μm feature size (i.e., the gate oxide thickness was reduced to 30 Å and the substrate doping was increased to 1.2×10^{18} cm^{-3}). The actual channel lengths of the 0.1 μm and 0.125 μm devices are 0.058 μm and 0.061 μm, respectively. These channel lengths are close to the envisioned limits for conventional Si MOSFET's [38]. The threshold voltage difference between the uniform and the graded channel devices is partly due to the different peak Ge composition (185 mV) and partly due to the build-in field caused by compositional grading. The threshold voltage swing at small gate lengths is slightly more pronounced for the uniform channel device.

Grading has a more significant impact on the subthreshold slope, as illustrated in Fig. 11. Graded 0.125 μm devices have a subthreshold slope of 100 mV/decade as opposed to 120 mV/decade for the corresponding uniform channel p-MOSFET. Again, this is the result of the grading induced built-in field which sharpens up the channel turn on and delays short channel effects by pushing carriers closer to the gate. It can therefore be concluded that by ramping up the Ge composition in the channel, short channel effects are reduced

and the feature size of Si–SiGe MOSFET's can be shrunk below 0.1 μm.

VI. Conclusion

The performance of submicrometer Si–SiGe MOSFET's was investigated using 2D numerical simulation. It was demonstrated that, by fully graded the Ge composition in the channel, heterostructure MOSFET's can be scaled down to channel lengths below 0.1 μm without degradation from short channel effects. Another important consequence of the fully graded SiGe channel is the increase in transconductance, voltage gain, cutoff frequency and maximum frequency of oscillation as compared to devices with uniform Ge channels. This improvement is particularly significant at small effective gate voltages. Energy balance simulations revealed that hot carrier injection at the Si–SiO_2 interface was at least 50% lower in graded than in uniform channel p-MOSFET's.

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References

[1] B. S. Meyerson, "UHV/CVD growth of Si and Si:Ge alloys: Chemistry, physics and device applications," in *Proc. IEEE*, vol. 80, pp. 1592–1608, 1992.

[2] H. Morkoç, B. Sverdlov, and G-B. Gao, "Strained layer heterostructures, and their applications to MODFET's, HBT's and lasers," in *Proc. IEEE*, vol. 81, pp. 493–556, 1993.

[3] D. L. Harame, E. F. Crabbé, J. D. Cressler, J. H. Comfort, J. Y.-C. Sun, S. R. Stiffler, E. Kobeda, J. N. Burghartz, M. M. Gilbert, J. C. Malinowski, A. J. Daly, S. Ratanaphanyrat, M. J. Saccamango, W. Rausch, J. Cotte, C. Chu, and J. M. C. Stork, "A high performance epitaxial SiGe-base ECL BiCMOS technology," in *Proc. IEDM*, pp. 19–22, 1992.

[4] T. P. Pearsall, J. C. Bean, R. People, and A. T. Fiory, "Ge_xSi_{1-x} modulation-doped p-channel field effect transistors," in *Proc. 1st. Int. Symp. Silicon Molecular Beam Epitaxy, Electrochemical Soc.*, Pennington, N.J., pp. 400–405, 1985.

[5] H. Dambkes, H.-J. Herzog, H. Jorke, H. Kibbel, and E. Kasper, "The n-channel Si/SiGe modulation-doped field-effect transistor," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 633–6638, 1986.

[6] D. K. Nayak, J. C. S. Woo, J. S. Park, K.-L. Wang, and K. P. MacWilliams, "Enhancement-mode quantum-well Ge_xSi_{1-x} PMOS," *IEEE Electron Device Lett.*, vol. 12, pp. 154–156, 1991.

[7] U. König and F. Schäffler, "Si/SiGe modulation-doped field-effect transistor with two electron channels," *Electron. Lett.*, vol. 27, pp. 1405–1407, 1991.

[8] U. König, A. J. Boers, F. Schäffler, and E. Kasper, "Enhancement mode n-channel Si/SiGe MODFET with high intrinsic transconductance," *Electron. Lett.*, vol. 28, pp. 160–162, 1992.

[9] K. Ismail, B. S. Meyerson, S. Rishton, J. Chu, S. Nelson, and J. Nocera, "High-transconductance n-type Si/SiGe modulation-doped field-effect transistors," *IEEE Electron Device Lett.*, vol. 13, pp. 229–231, 1992.

[10] U. König and F. Schäffler, "p-type Ge-channel MODFET's with high transconductance grown on Si substrates," *IEEE Electron Device Lett.*, vol. 14, pp. 205–207, 1993.

[11] G. Schüberth, F. Schäffler, M. Besson, G. Abstreiter, and E. Gornik, "High electron mobility in modulation-doped Si/SiGe quantum well structures," *Appl. Phys. Lett.*, vol. 59, pp. 3318–3320, 1991.

[12] K. Ismail, S. F. Nelson, J. O. Chu, and B. S. Meyerson, "Electron transport properties of Si/SiGe heterostructures: Measurements and device implications," *Appl. Phys. Lett.*, vol. 63, no. 5, pp. 660–662, 1993.

[13] V. P. Kesan, S. Subbanna, P. J. Restle, M. J. Tejwani, J. M. Aitken, S. S. Iyer, and J. A. Ott, "High-performance 0.25 μm p-MOSFET's with silicon-germanium channels for 300K and 77K operation," in *Proc. IEDM*, pp. 25–28, 1991.

[14] S. Verdonckt-Vanderbroek, E. F. Crabbe, B. S. Meyerson, D. L. Harame, P. J. Restle, J. M. C. Storck, A. C. Megdanis, C. L. Stanis, A. A. Bright, G. M. W. Kroesen, and A. C. Warren, "High-mobility modulation-doped graded SiGe-channel p-MOSFET's," *IEEE Electron Dev. Lett.*, vol. 12, pp. 447–449, 1991.

[15] Silvaco International, Santa Clara, CA, "ATLAS II. 2D device simulation framework," *User Manual* Edition 1, 1993.

[16] Y. Apanovich, P. Blakey, R. Cottle, E. Lyumkis, B. Polsky, A. Shur, and A Tcherniaev, "Numerical simulation of submicron devices including coupled non-local transport and non-isothermal effects," *IEEE Trans. Electron Dev.*, vol. 42, no. 5, pp. 890–898, 1995.

[17] Y. Apanovich, R. Cottle, E. Lyumkis, B. Polsky, A. Shur, and P. Blakey, "2D simulation of heterojunction devices including energy balance and lattice heating," in *ESSDERC '94 Proc. of the 24th European Solid State Device Res. Conf.*, Sept. 1994, pp. 463–466.

[18] R. Stratton, "Diffusion of hot and cold electrons in semiconductor barriers," *Phys. Rev.*, vol. 126, no. 6, pp. 2002–2013, 1962.

[19] J. Sutherland and F. Hauser, "A computer analysis of heterojunction and graded composition solar cells," *IEEE Trans. Electron. Devices*, vol. ED-24, pp. 363–373, 1977.

[20] M. Lundstrom and R. Shuelke, "Numerical analysis of heterostructure semiconductor devices," *IEEE Trans. Electron. Devices*, vol. ED-30, pp. 1151–1159, 1983.

[21] P. M. Garone, V. Venkataraman, and J. C. Sturm, "Mobility enhancement and quantum mechanical modeling in Ge_xSi_{1-x} channel MOSFET's from 90 to 300 K," *Proc. IEDM*, pp. 29–32, 1991.

[22] S. P. Voinigescu, C. A. T. Salama, J.-P. Noël, and T. I. Kamins, "Optimized Ge channel profiles for VLSI compatible Si/SiGe p-MOSFET's, in *Proc. IEDM*, 1994, pp. 369–372.

[23] M. G. Schumacher, "VLSI compatible SiGe heterojunction bipolar transistors," M.A.Sc. Thesis, University of Toronto, 1993.

[24] S. H. Li, J. M. Hinckley, J. Singh, and P. K. Bhattacharya, "Carrier velocity-field characteristics and alloy scattering potential in $Si_{1-x}Ge_x/Si$," *Appl. Phys. Lett.*, vol. 63, no. 10, pp. 1393–1395, 1993.

[25] H. Miyata, T. Yamada, and D. K. Ferry, "Electron transport properties of a strained Si layer on a relaxed $Si_{1-x}Ge_x$ substrate by Monte Carlo simulation," *Appl. Phys. Lett.*, vol. 62, no. 21, pp. 2661–2663, 1993.

[26] T. Vogelsang and K. R. Hofmann, "Electron transport in strained Si layers on $Si_{1-x}Ge_x$ substrates," *Appl. Phys. Lett.*, vol. 63, no. 2, pp. 186–188, 1993.

[27] K. Katayama and T. Toyabe, "A new hot carrier simulation method based on full 3D hydrodynamic equations," in *Proc. IEDM*, pp. 135–138, 1989.

[28] M. A. Green, "Intrinsic concentration, effective densities of states, and effective mass in silicon," *J. Appl. Phys.*, vol. 67, pp. 2944–2954, 1990.

[29] R. People, "Physics and applications of Ge_xSi_{1-x}/Si strained layer heterostructures," *IEEE J. Quantum Electron.*, vol. QE-22, pp. 1696–1710, 1986.

[30] S. Voinigescu and C. A. T. Salama, "Optimal channel grading in p-type Si/SiGe metal oxide semiconductor field effect transistors (MOSFET's)," *Can. J. Phys.*, vol. 70, pp. 975–978, 1992.

[31] D. K. Nayak, J. S. Park, J. C. Woo, K. L. Wang, G. K. Yabiku, and K. P. MacWilliams, "High performance GeSi quantum-well PMOS on SIMOX," *Proc. IEDM*, pp. 777–790, 1992.

[32] B. Davari, "Low voltage/low power device technologies," in *IEDM*, Short Course, 1993.

[33] S. Voinigescu, K. Iniewski, R. Lisak, C. A. T. Salama, J. P. Noël, and D. Houghton, "New technique for the characterization of Si/SiGe layers using heterostructure MOS capacitors," *Solid-State Electron.*, vol. 37, pp. 1491–1501, 1994.

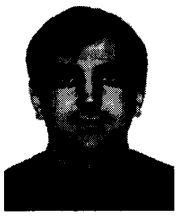
[34] S. E. Laux, "Techniques for small-signal analysis of semiconductor devices," *IEEE Trans. Electron. Devices*, vol. ED-32, pp. 2028–2035, 1985.

[35] M. H. Hanes, A. K. Agarwal, T. W. O'Keeffe, H. M. Hobgood, J. R. Szedon, T. J. Smith, R. R. Siergiej, P. J. McMullen, H. C. Nathanson, M. C. Driver, and R. N. Thomas, "*MICROX*^{TM}—An all-silicon technology for monolithic microwave integrated circuits," *IEEE Electron Device Lett.*, vol. 14, pp. 219–221, 1993.

[36] J. H. Huang, G. B. Zhang, Z. H. Liu, J. Duster, S. J. Wann, P. Ko, and C. Hu, "Temperature dependence of MOSFET substrate current," *IEEE Electron Device Lett.*, vol. 14, pp. 268–271, 1993.

[37] B. Pejčinović, T. W. Tang, S.-C. Lee, and D. H. Navon, "A numerical study of performance potential of $Si_{1-x}Ge_x$ pseudomorphic heterojunction bipolar transistor," *IEEE Trans. Electron. Devices*, vol. 39, pp. 2021–2028, 1992.

[38] B. Agrawal, V. K. De, and J. D. Meindl, "Opportunities for scaling FET's for gigascale integration (GSI)," *European Solid State Device Res. Conf.*, Grenoble, France, vol. ESSDERC-93, pp. 919–926, 1993.



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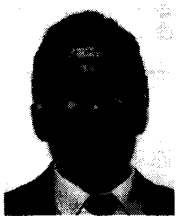

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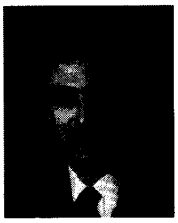

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