De-Embedding Transmission Line Measurements for Accurate Modeling of IC Designs

Alain M. Mangan, Sorin P. Voinigescu, *Senior Member, IEEE*, Ming-Ta Yang, and Mihai Tazlauanu

***Abstract*—A new technique to de-embed the contributions of parasitic structures from transmission line measurements is presented and applied to microstrip lines fabricated in 90- and 130-nm RF-CMOS technologies. De-embedded measurements are used to extract characteristic impedance, attenuation constant, group delay, and effective permittivity. The effective thickness of the ground plane is demonstrated to be as important as the thickness of the top metal layer in minimizing interconnect loss. Furthermore, it is confirmed that metal area densities as low as 65% are adequate for the ground plane of microstrip lines.**

***Index Terms*—Characterization, de-embedding, deep-submicrometer technologies, integrated circuits, interconnect, losses, microstrip lines, slotted ground planes, transmission lines.**

I. Introduction

DEMAND for increased bandwidth in communication systems has lead to ever higher operating frequencies and data rates in integrated circuits. The most recent examples of such developments are radio systems at 60 GHz [1], as well as broad-band communication networks with data rates up to 80 Gb/s [2]. As the frequency range of these applications enters the mm-wave regime, wavelengths become comparable to on-chip component dimensions. Hence, transmission lines play an increasingly vital role in both narrow-band [3] and broad-band [4] circuit design. Whether used intentionally or not, transmission lines are becoming essential in describing circuit behavior. Accurate models are therefore required.

Although transmission line theory is well established, uncertainties in various process parameters demand some form of measurement for model verification. However, any measurement is limited by an inherent flaw whereby test pads and interconnect are needed to access the device under test (DUT) (Fig. 1). Accurate de-embedding is therefore required to eliminate the parasitic contributions. Transmission line de-embedding techniques can also be used to remove parasitics from other device test structures [5].

Most de-embedding procedures rely completely on lumped equivalent circuits to model parasitics [6]–[9]. By contrast, it has been shown that the propagation constant (γ) can be extracted from the measurement of two transmission lines $(\ell_1 \neq \ell_2)$, without using explicit models for the pad parasitics, or calibrating the VNA [10]. Consequently, extraction techniques mostly focus on the characteristic impedance (Z_C) [11]–[14].

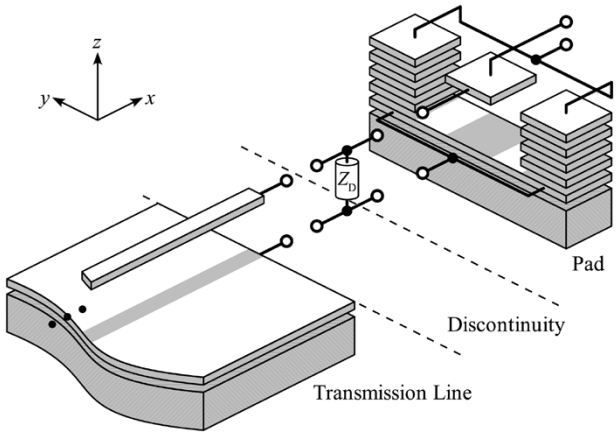

Fig. 1. Composition of a microstrip line test structure.

The new technique proposed in this paper relies on the symmetry of transmission line test structures. With regards to the extraction of γ, it is equivalent to that in [10], thus maintaining the state of the art [5]. It can also be shown that, when the test structure measurements are reciprocal $(S_{12} = S_{21})$, the proposed technique is equivalent to that of [15]. Unlike the latter technique, a more physically intuitive solution is obtained through the appropriate exploitation of *both* $ABCD$ and Y parameter representations.

After a brief description of the de-embedding algorithm, the proposed technique will be applied to microstrip line test structures fabricated in two RF-CMOS technologies. The results will be used to establish a relationship between line configuration and expected circuit performance.

II. Theory

A. De-Embedding

Consider two transmission line test structures of length ℓ_1 and ℓ_2, where $\ell_1 < \ell_2$ (Fig. 2). If properly designed, the structures will be perfectly symmetric about the y axis. By definition, the symmetry signifies that swapping ports 1 and 2 will not change the resulting $\boldsymbol{S}, \boldsymbol{Z}$, or $\boldsymbol{Y}$ matrices

$$\boldsymbol{S} = \text{Swap}\,(\boldsymbol{S}), \quad \boldsymbol{Z} = \text{Swap}\,(\boldsymbol{Z}), \quad \boldsymbol{Y} = \text{Swap}\,(\boldsymbol{Y}) \qquad (1)$$

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where Swap( ) swaps ports 1 and 2 of an S, Z, or Y matrix

$$\text{Swap}\left(\begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}\right) \equiv \left(\begin{bmatrix} a_{22} & a_{21} \\ a_{12} & a_{11} \end{bmatrix}\right). \tag{2}$$

Fig. 1 reveals that the transmission matrix of either test structure can be decomposed into a cascade of 5 two-port networks consisting of the two pads, the intrinsic device, and the associated pad-line discontinuities (Z_{D}). To simplify the derivations, the pad-line discontinuities will be lumped together with the pads, without loss of generality. Consequently, the $(ABCD)$ transmission matrix of test structure $l_i, \boldsymbol{M}^t_{l_i}$, can be represented as the following product:

$$\boldsymbol{M}^t_{l_i} \equiv \boldsymbol{M}_{P1}\boldsymbol{M}_{l_i}\boldsymbol{M}_{P2} \tag{3}$$

where

$\boldsymbol{M}_{l_i}$ represents the intrinsic line segment of structure i;
$\boldsymbol{M}_{P1}$ represents the left pad;
$\boldsymbol{M}_{P2}$ represents the right pad.

With this simple expression describing the test structures, we will derive an equation for the intrinsic transmission line. First, consider multiplying $\boldsymbol{M}^t_{l_2}$ with the inverse of $\boldsymbol{M}^t_{l_1}$ (Fig. 3)

$$\begin{aligned} \boldsymbol{M}^h_{l_2-l_1} &\equiv \boldsymbol{M}^t_{l_2} \times [\boldsymbol{M}^t_{l_1}]^{-1} \\ &= \boldsymbol{M}_{P1}\boldsymbol{M}_{l_2}\boldsymbol{M}^{-1}_{l_1}\boldsymbol{M}^{-1}_{P1} \\ &\equiv \boldsymbol{M}_{P1}\boldsymbol{M}_{l_2-l_1}\boldsymbol{M}^{-1}_{P1} \end{aligned} \tag{4}$$

where we define

$\boldsymbol{M}^h_{l_2-l_1}$ as the hybrid "structure" $\boldsymbol{M}^t_{l_2} \times [\boldsymbol{M}^t_{l_1}]^{-1}$ and
$\boldsymbol{M}_{l_2-l_1}$ as a line segment of length $\ell_2 - \ell_1$.

Assuming that the left pad can be modeled solely by a lumped admittance, Y_L, we have

$$\boldsymbol{M}_{P1} \equiv \begin{bmatrix} 1 & 0 \\ Y_L & 1 \end{bmatrix} \tag{5}$$

$$\boldsymbol{M}^h_{l_2-l_1} = \begin{bmatrix} 1 & 0 \\ Y_L & 1 \end{bmatrix} \boldsymbol{M}_{l_2-l_1} \begin{bmatrix} 1 & 0 \\ -Y_L & 1 \end{bmatrix}. \tag{6}$$

This will be referred to as the lumped pad assumption. Under the lumped pad assumption, the hybrid "structure" can be expressed in terms of Y parameters, as a parallel combination of the intrinsic transmission line and the parasitic lumped pads (Fig. 4)

$$\boldsymbol{Y}^h_{l_2-l_1} \equiv \boldsymbol{Y}_{l_2-l_1} + \begin{bmatrix} Y_L & 0 \\ 0 & -Y_L \end{bmatrix} \tag{7}$$

where $\boldsymbol{Y}^h_{l_2-l_1}$ is the Y parameter representation of $\boldsymbol{M}^h_{l_2-l_1}$ and $\boldsymbol{Y}_{l_2-l_1}$ is the Y parameter representation of $\boldsymbol{M}_{l_2-l_1}$.

Since the intrinsic device is symmetric, its Y parameters can be isolated by connecting $\boldsymbol{Y}^h_{l_2-l_1}$ in parallel with a port-swapped version of itself, thus canceling out the effects of the pads

$$\boldsymbol{Y}_{l_2-l_1} \equiv \frac{\boldsymbol{Y}^h_{l_2-l_1} + \text{Swap}(\boldsymbol{Y})^h_{l_2-l_1}}{2}. \tag{8}$$

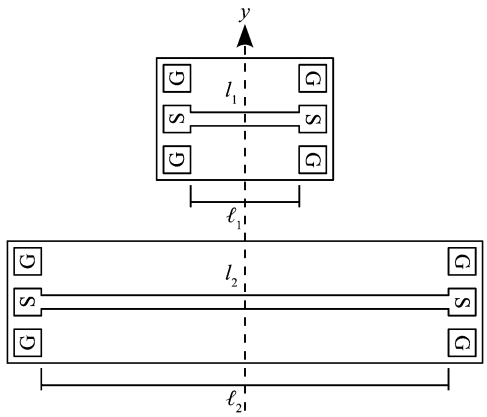

Fig. 2. Two transmission line test structures.

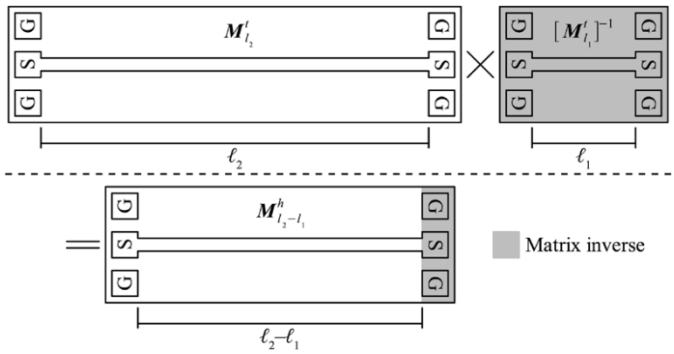

Fig. 3. Multiplying the transmission matrix of line 2 with the matrix inverse of line 1.

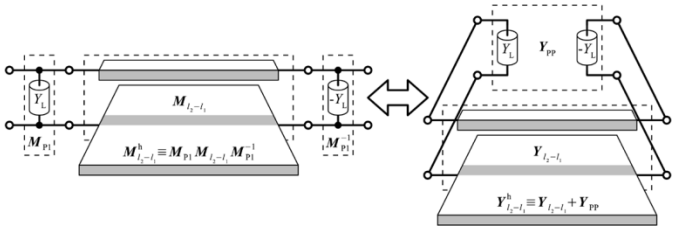

Fig. 4. Equivalent representations of the hybrid "structure" under the lumped pad assumption.

B. Extraction

Assuming that a lossy transmission line of length $\ell_2 - \ell_1$ can be modeled by [16]

$$\begin{aligned} \boldsymbol{M}_{l_2-l_1} &\equiv \begin{bmatrix} A & B \\ C & D \end{bmatrix} \\ &\equiv \begin{bmatrix} \cosh\gamma(\ell_2-\ell_1) & Z_c \sinh\gamma(\ell_2-\ell_1) \\ Z_C^{-1}\sinh\gamma(\ell_2-\ell_1) & \cosh\gamma(\ell_2-\ell_1) \end{bmatrix} \end{aligned} \tag{9}$$

we can extract the characteristic impedance (Z_C) and the propagation constant (γ) using

$$Z_C = \sqrt{\frac{B}{C}}\ [\Omega] \quad \text{and} \quad \gamma = \frac{\cosh^{-1} A}{\ell_2 - \ell_1}. \tag{10}$$

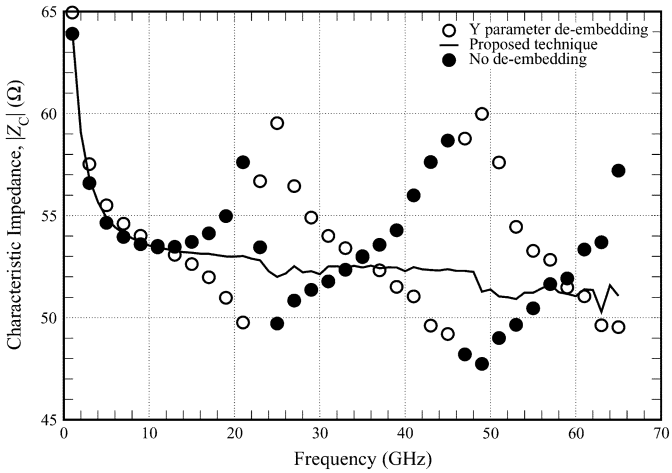

Fig. 5. Measured Z_C of a $\ell_2 = 3.68$ mm meandering microstrip line.

Fig. 5 shows the extracted characteristic impedance of a $\ell_2 = 3.68$ mm meandering microstrip line. The results demonstrate that the proposed technique is more immune to the discontinuities in the $Z_C(f)$ characteristics, which are typically pronounced near frequencies where $\ell = n\lambda/2$. Note that the short microstrip line segment used for de-embedding is only $\ell_1 = 100$ μm long.

III. Measurements

A. Setups

1) 50-GHz Setup: Measurements were performed on an HP8510C VNA with flexible cables and Cascade Microtech device probes at Quake Technologies in Ottawa. The measurements were calibrated using the line-reflect-match (LRM) algorithm provided with the VNA, and the standards from a Cascade Microtech ISS 101–190 substrate.

2) 65-GHz Setup: Measurements were performed on a Wiltron 360B VNA with semi-rigid cables and Cascade Microtech device probes at the University of Toronto. The measurements were calibrated using the LRM algorithm provided by the WinCal software from Cascade Microtech, and the standards from a Cascade Microtech ISS 101–190 substrate.

LRM calibrations were used to compensate for the measurement system and move the reference plane up to the probe tips. Test structures fabricated in the 90-nm process were measured using both setups with excellent agreement between the two setups. The structures fabricated in the 130-nm process were measured solely with the 50-GHz setup.

B. 90-nm RF-CMOS Test Structures

1) Fabricated Devices: Eight pairs of microstrip test structures were designed using various conductor and ground plane configurations (Fig. 6). When comparing characteristics, the convention "metal $[x]$ over $[y]w = [z]$ μm" will refer to a microstrip line designed with a metal x conductor, a metal y ground plane, and a conductor width of z micrometers. For reference, the process uses a 0.9-μm-thick metal 8 layer and a 3.3-μm-thick metal 9 layer, both implemented in copper.

2) Layout: Access to the microstrip line conductors is provided by chamfered 50 $\times$ 50 μm^2 signal pads constructed in metal 9. On either side of each signal pad, larger pads are used to contact the ground plane using ground–signal–ground (GSG) device probes of 100-μm pitch. A highly doped n-well connected to the ground pads is placed under the signal pads. The resultant pad capacitance was measured to be in the order of only 16–17 fF.

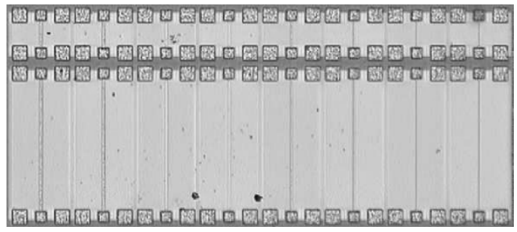

Fig. 6. Micrograph of the eight transmission lines implemented in the 90-nm technology. Both the long (600 μm) and the short (100 μm) lines are present.

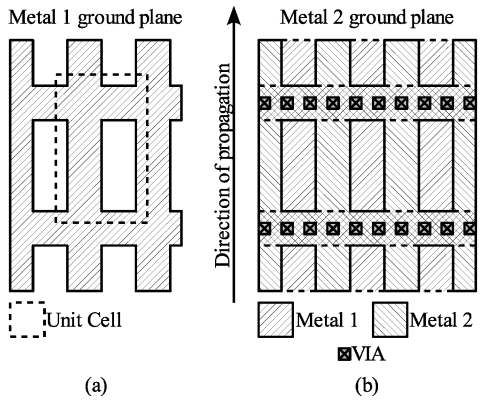

Fig. 7. Mesh pattern used for (a) metal 1 slotted ground planes (b) metal 2 slotted ground planes.

As CMOS technologies advanced beyond the 180-nm node, increasingly stringent metal density rules prohibited the design of solid ground planes. To accommodate these restrictions, metal ground planes must now be slotted. In these technologies, the ideal ground plane design implements the maximum allowed metal density with the smallest slot dimension possible. If the slots are much shorter than the wavelength, they will not affect the line characteristics significantly. With all microstrip lines designed in the 90-nm process, metal 1 ground planes are constructed from the unit cell mesh sketched in Fig. 7(a), corresponding to a metal density of approximately 65%. For lines constructed with metal 2 ground planes, the metal 2 mesh is positioned such as to cover the slots in the metal 1 mesh [Fig. 7(b)]. The two meshes are shunted together to increase the effective ground plane thickness, and reduce its resistance. A micrograph of the slotted ground plane from one of the short lines is presented in Fig. 8.

3) Characteristic Impedance and Dispersion in Lossy Lines: Fig. 9 shows that, with microstrip line configurations typically used in IC designs, Z_C exhibits a strong frequency dependence at frequencies below 10 GHz. Similar results are observed for the group delay below 2 GHz (Fig. 10). It should be emphasized that these nonidealities are neither artifacts of the measurement system nor of the de-embedding technique.

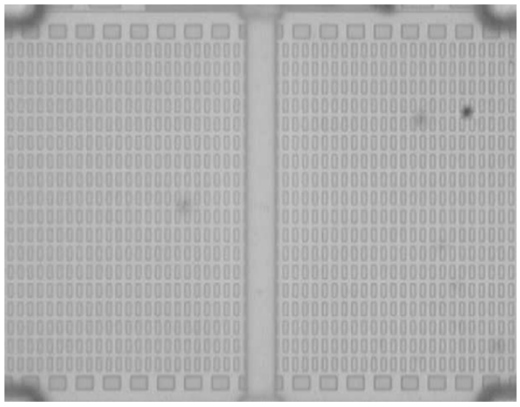

Fig. 8. Micrograph of a slotted ground plane.

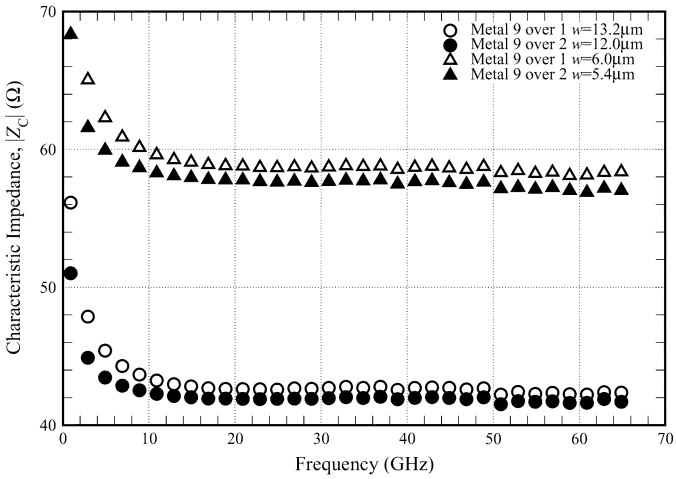

Fig. 9. Characteristic impedance as a function of frequency for transmission lines fabricated with a metal 9 conductor in the 90-nm process.

Z_C and γ can be expressed in terms of $RLGC$ parameters using

$$Z_C = \sqrt{\frac{R+j\omega L}{G+j\omega C}} \tag{11}$$

$$\gamma = \alpha + j\beta = \sqrt{(R+j\omega L)(G+j\omega C)}. \tag{12}$$

At sufficiently high frequencies ($\omega L \gg R$ and $\omega C \gg G$), we have $Z_C \approx \sqrt{L/C}$ and $\beta \approx \sqrt{LC}$. Below these frequencies, Z_C and $\tau \equiv \partial\beta/\partial\omega$ are, in general, frequency dependent. For example, as $\omega \to 0$, the "dc" characteristic impedance is given by $Z_C \approx \sqrt{R/G}$.

Assuming little frequency dependence of the $RLGC$ parameters, it is possible to obtain frequency independent values for both Z_C and τ through circuit design, by ensuring that $R/G = L/C$. Such distortionless lines are preferable for broad-band digital circuits, and can normally be realized by periodically loading the line with either a series inductor [17] or a parallel resistor [18]. The resistive solution increases G, making it possible for the designer to set Z_C to a desired value, whereas increasing L inevitably pulls it closer to the (typically large) "dc" value.

4) Impact of Materials and Geometry on Electrical Characteristics: A preliminary inspection of Figs. 11 and 12 indicates

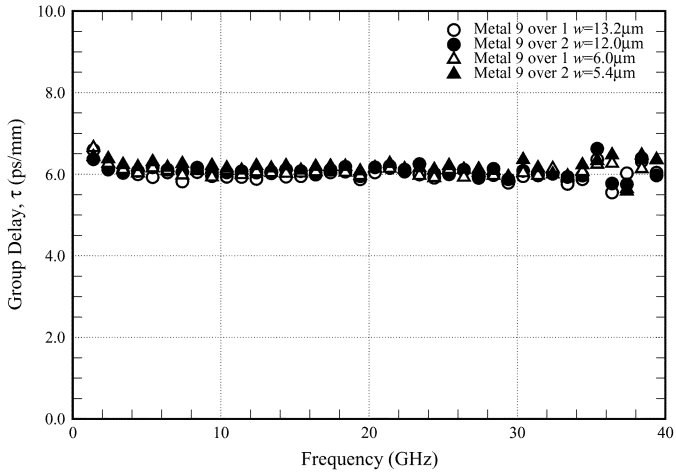

Fig. 10. Group delay as a function of frequency for transmission lines fabricated with a metal 9 conductor in the 90-nm process.

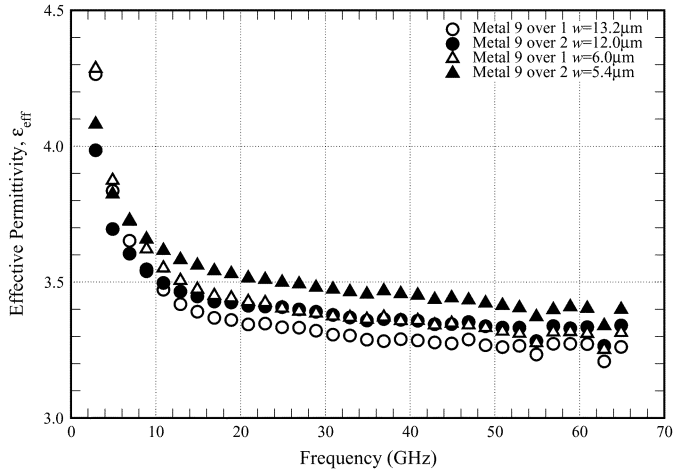

Fig. 11. Effective permittivity as a function of frequency for transmission lines fabricated with a metal 9 conductor in the 90-nm process.

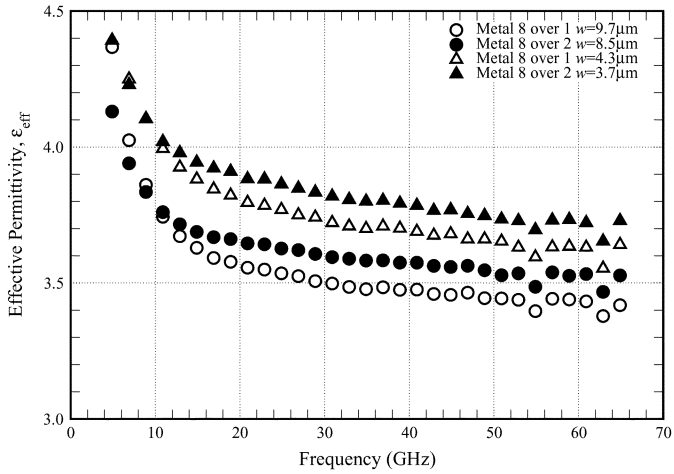

Fig. 12. Effective permittivity as a function of frequency for transmission lines fabricated with a metal 8 conductor in the 90-nm process.

that wider conductors lead to a smaller effective permittivity ($\epsilon_{\text{eff}} \equiv (c(\beta/\omega))^2$). This is a direct result of the passivation layer having a much higher permittivity than the lower-κ interlayer dielectrics (ILDs). Microstrip lines with wider conductors

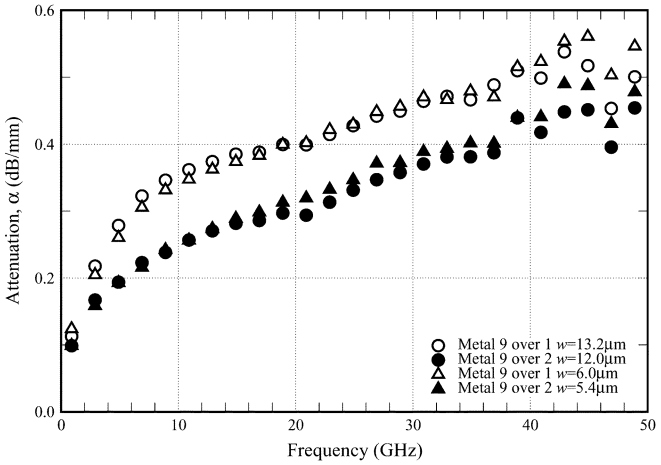

Fig. 13. Attenuation as a function of frequency for transmission lines fabricated with a metal 9 conductor in the 90-nm process.

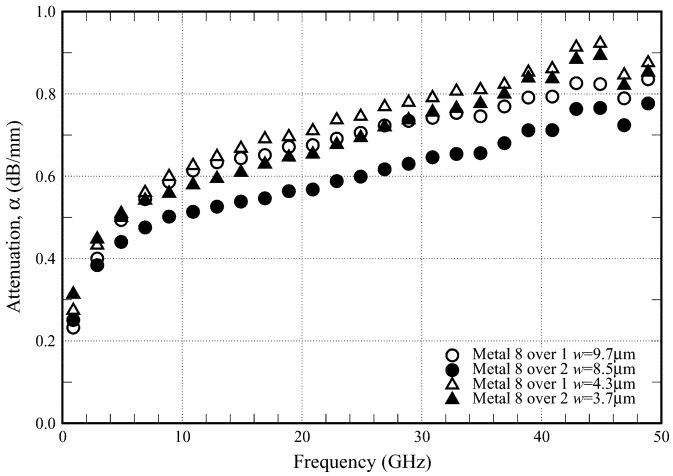

Fig. 14. Attenuation as a function of frequency for transmission lines fabricated with a metal 8 conductor in the 90-nm process.

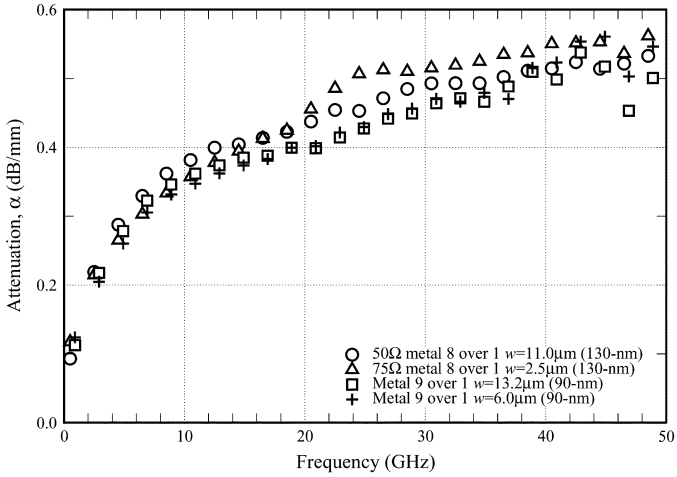

Fig. 15. Technology comparison of the attenuation in lines designed with the topmost conductor and a metal 1 ground plane.

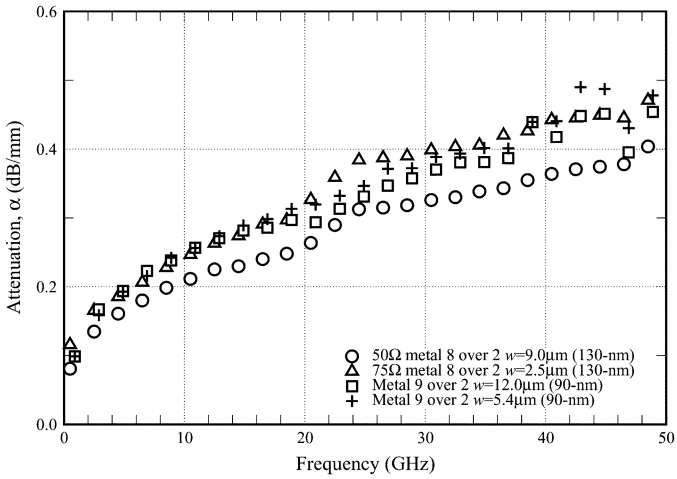

Fig. 16. Technology comparison of the attenuation in lines designed with the topmost conductor and a metal 2 ground plane.

more closely resemble parallel plate waveguides. As a consequence, less field components penetrate the higher-κ passivation layers [17].

When compared to lines with metal 9 conductors, those designed with metal 8 conductors have a noticeably higher effective permittivity. This difference is mainly attributed to the fact that the higher-κ passivation layer does not extend very far over the metal 9 conductor. Consequently, the low permittivity of air helps offset the high permittivity of the passivation layers. For lines designed with metal 8 conductors, the lower-κ layer of air is now much farther away from the conductor surface. Moreover, relatively higher-permittivity dielectrics are used to fill the space of the absent metal 9 material. Combined, these factors cause the systematic jump in ϵ_{eff} observed between the lines using different conductor metals. This explanation is further confirmed by the spread in measured ϵ_{eff}. The lines designed with metal 8 conductors have a larger spread due to the larger difference in permittivities above and below the conductor.

In order to minimize losses, it is important to be able to identify the dominant source. Comparing Figs. 13 and 14, we can see that lines with metal 8 conductors are lossier than those realized with metal 9 conductors. This trend starts at low frequencies, where a difference in dc resistance is readily apparent. The consistently lower dc resistance of the lines with metal 9 conductors is a direct result of the thicker metal 9 layer. Even the narrowest metal 9 line has a larger cross-sectional area than the widest one using metal 8.

A second trend is related to the ground plane and is made evident from the attenuation plots. As the frequency increases, the lines with a metal 1 ground plane exhibit more loss than those with a metal 2 ground plane. This can be explained by the larger effective thickness of the metal 2 ground planes which are shunted together with a metal 1 mesh. The only exception occurs for the narrowest line ($w = 3.7$ μm), for which the conductor remains the dominant source of loss.

C. Technology Comparison

In order to cover a larger device space, microstrip lines fabricated in a 130-nm RF-CMOS process were also characterized. Although the two processes have similar backend, they use slightly different ILD and metal thicknesses, as well as conductivities. The most noteworthy difference is that the 130-nm process does not feature lower-κ dielectrics. To ensure a fair

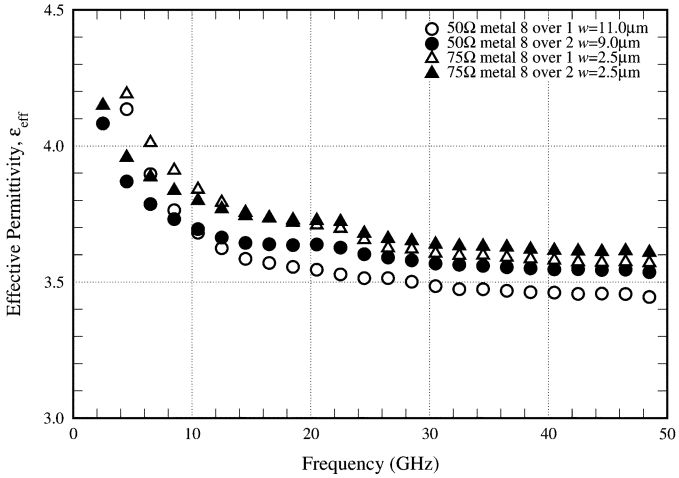

Fig. 17. Effective permittivity as a function of frequency for transmission lines fabricated in the 130-nm process.

comparison, only lines with conductors designed in the top-most metal layers will be considered. These conductors are fabricated with a thickness of 3.3 μm in both technologies.

Figs. 15 and 16 show a remarkable agreement between the attenuation versus frequency characteristics of the two technologies. The close match is attributed to the similar thicknesses of corresponding ground planes.

With respect to permittivity, Fig. 17 also shows a clear width dependence, as in Fig. 11. Since the 130-nm process does not have lower-κ dielectrics, the extracted values of ϵ_{eff} are higher than those of Fig. 11.

IV. Conclusion

A new de-embedding technique which accurately removes pad parasitics and pad-line discontinuities was presented for the characterization of lossy IC transmission lines. It was found that line pairs as small as 600 μm and 100 μm provide adequate results if the pad parasitics are minimized. Measurements also indicate that, with the thick top metal layers available in RF-CMOS technologies, ground planes are often the dominant source of high frequency loss. Furthermore, the characteristic impedance and group delay of microstrip transmission lines are strongly frequency dependent up to 10 and 2 GHz, respectively. Therefore, it can be concluded that the dispersive behavior of interconnect lines in broad-band higher-speed digital circuits must be mitigated by periodically loading the signal lines.

Acknowledgment

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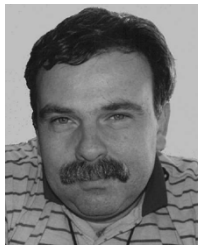

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