A 1GHz Bandwidth Low-Pass ΔΣ ADC with 20GHz to 50GHz Adjustable Sampling Rate

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***Abstract* — This paper presents a wideband continuous-time ΔΣ-modulator intended for multi-gigabit OFDM receiver applications. Two versions of the circuit were fabricated in a 130-nm SiGe BiCMOS process with 170GHz f_T in order to investigate the effect of finite quantizer gain and delay on dynamic range. The ADC achieves an SNDR of 44.3dB over a 500MHz passband and an SNDR of 37.1dB over a 1GHz passband while consuming 350mW from a 2.5V supply (650mW including clock distribution).**

***Index Terms* — Analog-digital conversion, continuous-time, delta-sigma, low-pass, metastability, radio receivers.**

I. Introduction

Over the past decade, continuous-time ΔΣ ADCs have been gaining in popularity due to their ability to exploit time-resolution instead of amplitude resolution. Unlike their discrete-time switch capacitor counterparts, continuous-time modulators are not limited by settling-time and can therefore be sampled at very high speeds, making best use of the ever-increasing transistor f_T [1]-[2].

In this paper, we present the first ΔΣ modulator with 1GHz passband and high enough resolution for 60GHz OFDM radio applications. As shown in Fig. 1, two ADCs can be used in a direct conversion receiver to digitize the I and Q signals; providing 1GHz of bandwidth for 4Gb/s 16 QAM. A continuous-time ΔΣ modulator with high sampling rate is particularly well suited for this application since a high frequency clock is already available from the 60GHz front end. Furthermore, the ADC provides built-in anti-alias filtering.

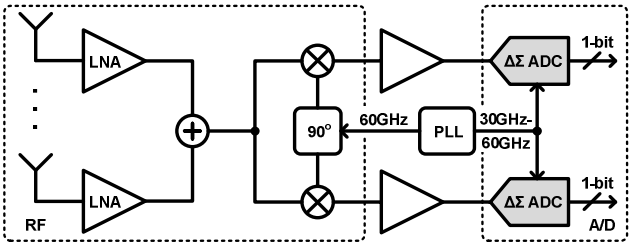

Fig. 1. 60GHz radio receiver with proposed ADC.

II. ADC Design

A top-level block diagram of the ADC is shown in Fig. 2. Second-order noise shaping is achieved by employing two opamp-based integrators with feedback from DAC1 and DAC2. The third feedback path, through DAC3, is for delay compensation and mitigates the cumulative delays introduced by the quantizer amplifiers and latches. The DAC currents are adjustable in order to preserve the desired Noise Transfer Function (NTF) over the entire range of sampling frequencies.

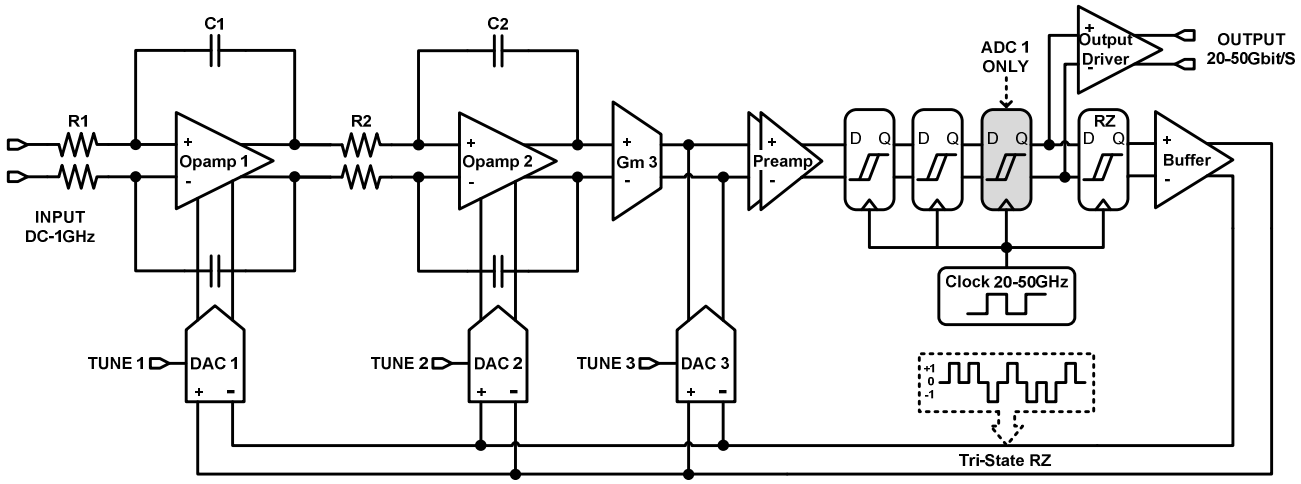

Fig. 2. Top-level block diagram of ADC1 and ADC2.

The opamp described in Fig. 3 employs a pMOS-HBT folded-cascode and achieves similar performance to the telescopic cascode described in [3] while operating from a lower supply voltage of 2.5V. Consequently, the DC voltage at the input (0.5V) is too low to properly operate the feedback DACs which consist of an HBT differential pair and current source. A more feasible location to connect the feedback is at the high impedance output node of the opamp, as shown in Fig. 3. In addition to providing ample voltage headroom for the feedback, this configuration merges the current sources for the opamp and feedback DACs. The current mismatches introduced by the DACs are corrected by the common-mode feedback of the opamp through transistors M1 and M2.

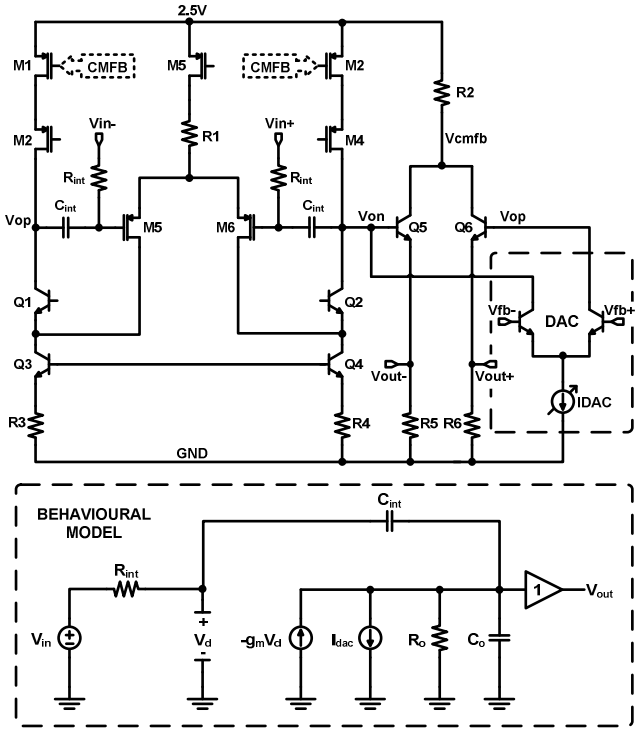

Fig. 3. Opamp-integrator schematic and behavioral model.

The behavioral model of the opamp shown at the bottom of Fig. 3 is employed in system-level simulations. Parameters R_o and C_o represent the finite impedance and capacitance at nodes Von and Vop while g_m is the transconductance of the input transistors M5 and M6. The gain of the integrator is largely dependent on R_{int} and C_{int}. Since noise added to the input of the circuit is not noise-shaped, R_{int} must be made as small as possible while the size of C_{int} must be limited in order to avoid slewing. In this design, both stages use 50Ω resistors for R_{int} in combination with integration capacitors of 500fF and 250fF for the first and second stage respectively. The linear signal transfer function from voltage input to voltage output is

$$\frac{V_{out}}{V_{in}} = \frac{-g_m R_o}{s^2 RCR_oC_o + s(RC + R_oC_o + RR_oCg_m) + 1} \quad (1)$$

while the feedback transfer function is given by

$$\frac{V_{out}}{I_{DAC}} = \frac{-R_o(sRC+1)}{s^2 RCR_oC_o + s(RC + R_oC_o + RR_oCg_m) + 1}. \quad (2)$$

The quantizer consists of a preamplifier, two (ADC2) or three (ADC1) latches followed by a return-to-zero (RZ) latch and a buffer that drives the three DACs in the feedback path. The RZ signal is implemented by a tri-state latch [4], as shown with dotted lines in Fig. 4, providing half a clock cycle of delay compensation and avoiding the errors introduced by the finite rise and fall times of the digital feedback signal.

The clock distribution is adapted from [2] to operate from 20GHz to 50GHz and delivers a differential clock to the quantizer from a single-ended input. A five-stage BiCMOS cascode topology is used for sufficient gain and common-mode rejection.

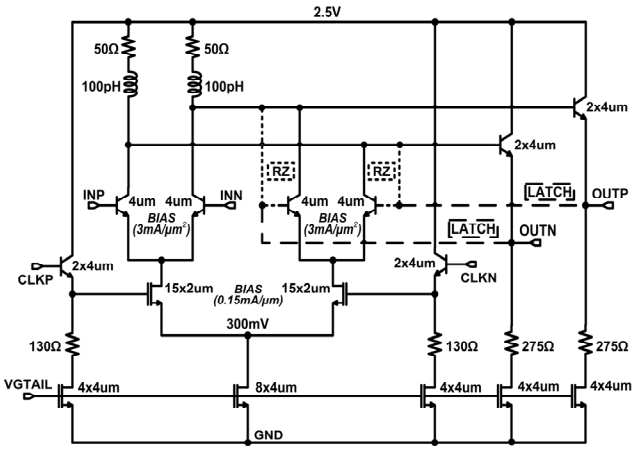

Fig. 4. Quantizer latch: regular (dashed) and RZ (dotted).

A detailed behavioral model of the ADC is implemented in Matlab and Simulink in order to validate the design and study the impact of circuit non-idealities on dynamic range. The model includes independently-controlled parameters for finite opamp gain, bandwidth and slew rate, quantizer gain and hysteresis, feedback delay, and finite voltage swing at critical nodes. Among all the parameters, quantizer gain and delay are most critical. At low gain, the dynamic range is limited by metastability, especially because the quantizer is single-bit. As preamplifiers and latches are cascaded together to increase quantizer gain and improve metastability, the

cumulative delay introduced by each block eventually limits performance. As shown in Fig. 5, the dynamic range over a 100MHz bandwidth at 40GS/s is optimal around a delay of 1.9 sample periods (Ts) and gain of 475V/V. To investigate this tradeoff and optimize performance, two versions of the ADC are implemented: one with 4 latches (ADC1) and the other with 3 latches (ADC2).

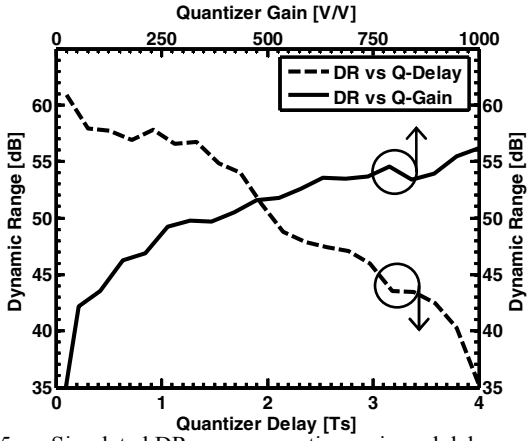

Fig. 5. Simulated DR versus quantizer gain and delay

III. Measurement Results

A test chip including the two ADCs, a retimer breakout and device test structures was manufactured by STM in a 130-nm SiGe BiCMOS process with 170GHz f_T (Fig. 6).

Fig. 7 shows the measured output eye diagram of the retimer breakout when a 25Gb/s input signal with 23mV$_{pp}$ amplitude is retimed by a 50GHz clock. The rms jitter improves from 2.53pS to 0.38pS.

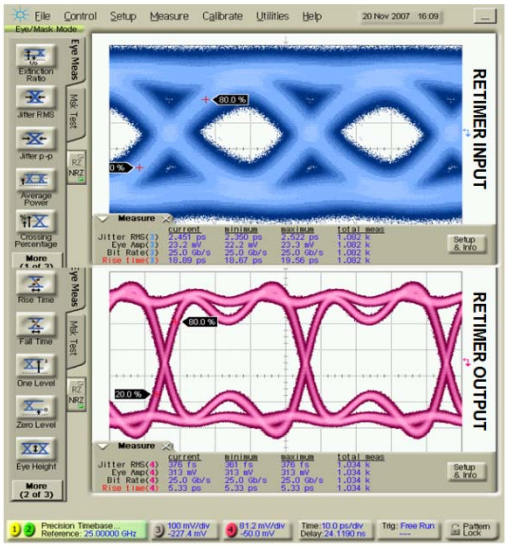

Fig. 7. Measured retimer input (top) and output (bottom).

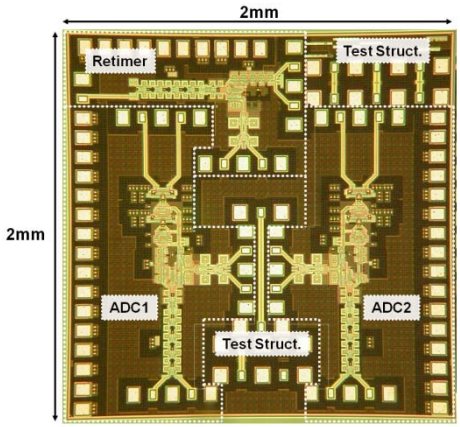

Fig. 6. Die photo of ADC, retimer breakout and test structures.

The ADC was measured using the Agilent E8257D and E4422B signal sources to generate a 20-50GHz clock and 1-1000MHz input, respectively. The dynamic range is measured by directly connecting one end of the digital output to an Agilent E4448A power spectrum analyzer. For any given passband (PB), the input frequency is at ⅓PB so that the second and third harmonics are included in the integrated noise plus distortion measurement. The spectrum of ADC2 is shown in Fig. 8 for a 150MHz input. The inset plots the spectrum on a log scale, confirming second-order noise shaping.

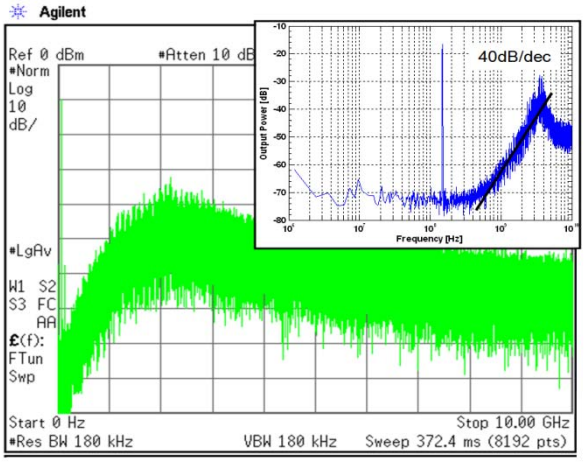

Fig. 8. Power spectral density from PSA (log-scale inset).

Fig. 9 compares the measured dynamic range of both ADCs as a function of sampling rate for passbands of 100MHz, 500MHz, and 1GHz. As the bandwidth increases, the peak SNDR occurs at higher sampling rates. For a passband of 1GHz, increasing the sampling rate of ADC1 from 22GHz to 50GHz adds nearly 2 bits of resolution. These results emphasize the necessity of using high sampling rates for ΔΣ ADCs operating in the hundreds of megahertz passband range.

While the ADC with 3 latches has higher peak performance over all bandwidths, the one with 4 latches is superior for sampling rates above 45GHz. This suggests that ADC1 is performance-limited by loop delay while ADC2 is limited by metastability - as predicted by our system-level simulations.

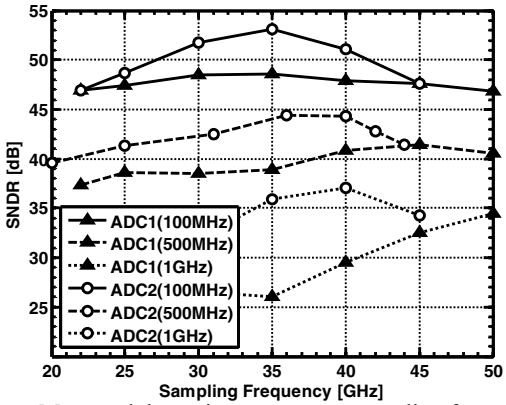

Fig. 9. Measured dynamic range versus sampling frequency.

The peak SNDR versus bandwidth is shown on the left of Fig. 10. The performance drops by approximately 15dB/dec for passbands between 200MHz and 500MHz. At bandwidths beyond 500MHz, the noise floor begins to rise, leading to faster degradation in SNDR. A comparison of this work to the-state-of-the-art is demonstrated in Fig. 11 including ADCs of all types [5].

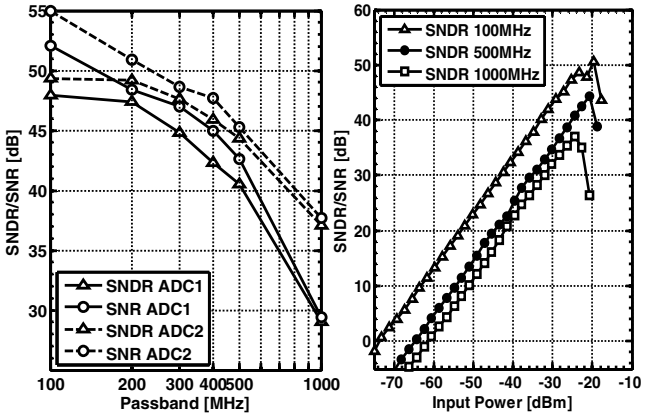

Fig. 10. Measured SNR & SNDR versus passband (left) and input power (right) with 40GHz sampling rate.

IV. Conclusion

We presented the first ΔΣ modulator achieving an ENOB of 6 bits at 1GHz. This ADC exploits the ever-higher f_T of modern transistor technologies and has comparable FoM to flash and pipeline topologies while employing a much simpler architecture.

TABLE I
SUMMARY OF ADC PERFORMANCE

Signal Bandwidth	100MHz	500MHz	1GHz
Sampling Rate	35GHz	37GHz	40 GHz
OSR	175	37	20
SNR	58.9 dB	45.9 dB	37.7 dB
SNDR	53.1 dB	44.4 dB	37.1 dB
ENOB	8.5 bits	7.1 bits	5.9 bits
SFDR	65 dB	63 dB	50 dB
Power	650 mW		
FoM	8.8 pJ/conv	4.48 pJ/conv	5.55 pJ/conv
Power†	350 mW		
FoM†	4.74 pJ/conv	2.58 pJ/conv	2.99 pJ/conv

†Assuming ADC is used inside a receiver with available clock

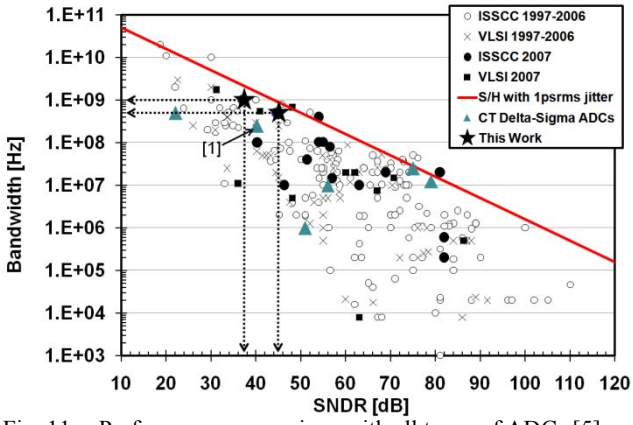

Fig. 11. Performance comparison with all types of ADCs [5].

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References

[1] S. Krishnan, et al, "An 8-GHz continuous-time ΔΣ analog-digital converter in an InP-based HBT technology," *IEEE Trans. Microwave Theory Tech*., vol. 51, no. 12, pp. 2555–2561, Dec. 2003.

[2] T. Chalvatzis, E. Gagnon, M. Repeta and S.P. Voinigescu, "A low-noise 40-GS/s continuous-time bandpass delta-sigma ADC centered at 2GHz for direct sampling receivers," *IEEE Journal of Solid State Circuits*. Vol.42, No.5, pp.1065-1075, May. 2007.

[3] S.P. Voinigescu, R. Beerkens, T. O. Dickson, and T. Chalvatzis, "Design methodology and applications of SiGe BiCMOS cascode opamps with up to 37-GHz unity gain bandwidth," *IEEE CSICS,* Technical Digest, pp.283-286, Nov. 2005.

[4] W. Gao, J.A. Cherry, W.M. Snelgrove, "A 4 GHz fourth-order SiGe HBT band-pass ΔΣ modulator", *Tech. Dig. Symp. On VLSI Ckt*. 1998, pp. 174-175

[5] B. Murmann, "ADC performance survey 1997-2007," [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.htm