A High Modulation Bandwidth, 110 GHz Power-DAC Cell for IQ Transmitter Arrays With Direct Amplitude and Phase Modulation

Andreea Balteanu, *Student Member, IEEE*, Stefan Shopov, *Student Member, IEEE*, and Sorin P. Voinigescu, *Senior Member, IEEE*

***Abstract*—This paper studies the maximum Baud rate and the scalability to the W-Band of the mm-wave power-DAC transmitter architecture. Proof-of-concept implementations of a single DAC lane and of a 2×2 IQ transmitter array are reported in 45 nm SOI CMOS. The DAC cell achieved 29 GHz OOK and 29 GHz BPSK modulation bandwidth and 2×44 Gb/s BPSK+OOK data rates for carriers in the 100–110 GHz range. The corresponding energy efficiency is 7.5 pJ/bit at an output power of 12 dBm. For the 2×2 IQ array, an EVM of 9.0% is estimated over a 12 GHz bandwidth, from large signal power and S-parameter phase measurements.**

***Index Terms*—BPSK modulator, IQ array, mm-wave, mm-wave DAC, OOK modulator, power amplifier, power-added efficiency, power-DAC, QAM modulator, quadrature mm-wave modulator, SOI CMOS, W band.**

I. Introduction

THE W-band (75–110 GHz) spectrum has traditionally been used for automotive and military radar applications. In recent years, the ever-increasing bandwidth needs of users streaming videos to their mobile devices as well as the increased prevalence of picocells have also made the W-band attractive for cellular backhaul. Simultaneously, as most of our personal communications and entertainment moves to wireless platforms, the demand for low-cost, energy-efficient wireless transceivers whose power consumption scales with the data rate rules out the use of current-mode logic (CML) in the baseband sections of such radio transceivers, even at data rates of tens of Gb/s. To achieve operation at 40–50 Gbaud in standard CMOS logic, an aggressively scaled CMOS technology with fast p-MOSFETs is required. Although deeply scaled CMOS technologies with f_T and f_{MAX} values exceeding 250 GHz offer low-power integration and reasonable W-band performance with several CMOS transmitters being recently published [1]–[6], they suffer from low breakdown voltages which limit the achievable output power, power-added efficiency (PAE), and linearity needed for high order m-ary QAM transmitters. To circumvent some of these problems, a fully digital, direct modulation transmitter architecture with free-space power combining was recently proposed and demonstrated in the Q band (33–50 GHz) in [7]. This IQ transmitter array consists of directly modulated 3-state power-DAC antenna elements which are driven in saturation by the quadrature LO signal for maximum output power and efficiency. To overcome the low-breakdown voltage of the 45 nm SOI-CMOS process in which it was manufactured, the power DAC features a series-stacked supercascode output stage. It also incorporates binary phase- shift keying (BPSK) and on/off keying (OOK) modulation. The independent OOK modulation of each antenna element allows the entire IQ transmitter array to act as a IQ power-DAC with antenna level segmentation. The BPSK- and OOK-modulated output signals from each DAC segment are combined in free space to form an arbitrary QAM constellation. In contrast, in [8], the outputs of two QPSK modulators are combined on-chip to produce a 4-point QPSK constellation at 114 GHz in a 45 nm LP CMOS technology. In [9], a system with reconfigurable QAM constellation and off-chip power combining is investigated at 45 GHz in a 65 nm CMOS technology. A 4-element I/Q array employing spatial combining was previously demonstrated in [10] at 60 GHz, also in a 65 nm CMOS technology.

This paper explores the circuit topologies needed to scale the Q-band IQ transmitter array concept described earlier to the W-band. The 3-state power-DAC element, briefly discussed in [11], and a new 2×2 IQ array transmitter with record modulation rate are demonstrated in the same 45 nm SOI CMOS process as in [7]. The transmitter array design considerations and circuit implementations of the key building blocks are discussed in Sections II and III, respectively. Section IV provides an overview of the 45 nm SOI CMOS technology along with a detailed description of the passive component design and layout challenges. The main measurement results are summarized in Section V, followed by concluding remarks in Section VI.

II. Transmitter Chiplet Architecture

Fig. 1 shows the block diagram of the proposed 2×2 IQ transmitter array chiplet. Each array element consists of a 3-state power-DAC whose block diagram is described in Fig. 2. The external LO-signal is applied to a power splitter followed by two 90-degree hybrids which feed the four identical power-DAC array elements in quadrature pairs. The first

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The authors are with the Electrical and Computer Engineering Department, University of Toronto, Toronto, ON, M5S 3G4, Canada (e-mail: baltean1@eecg.utoronto.ca).

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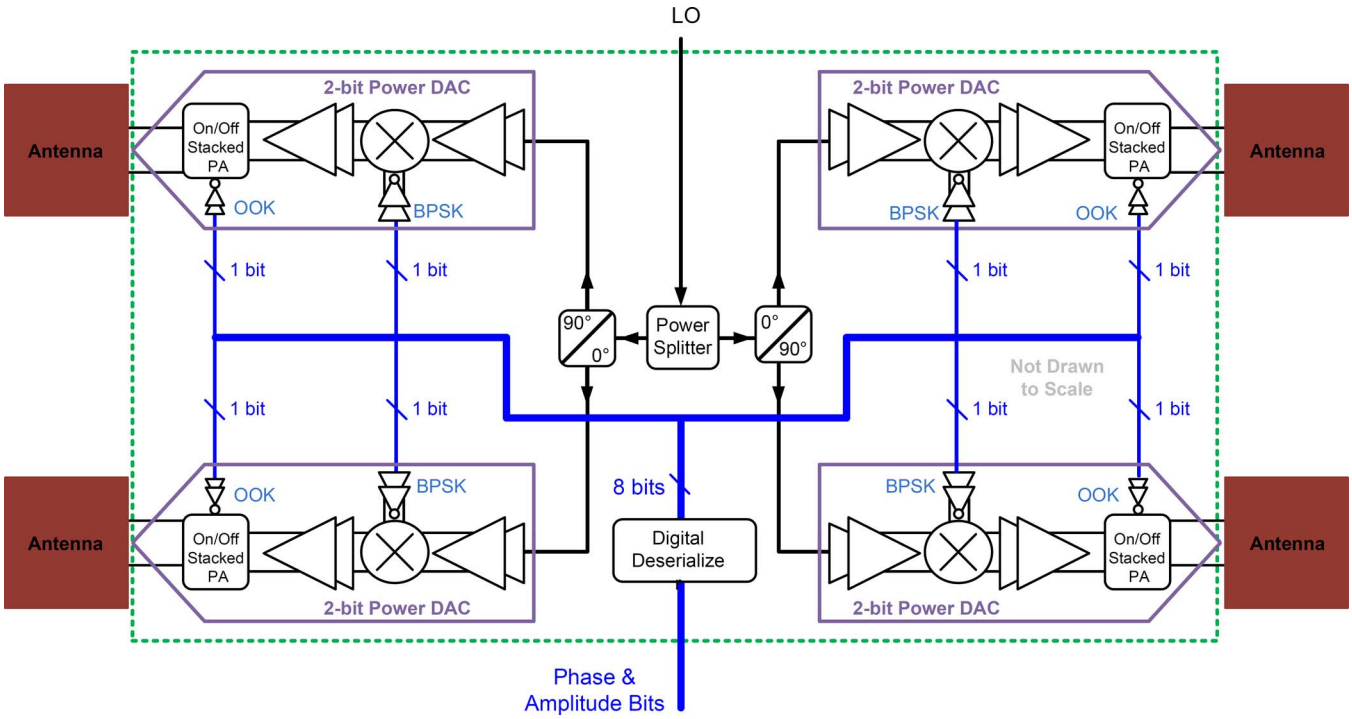

Fig. 1. Block diagram of the 2×2 IQ transmitter array chiplet.

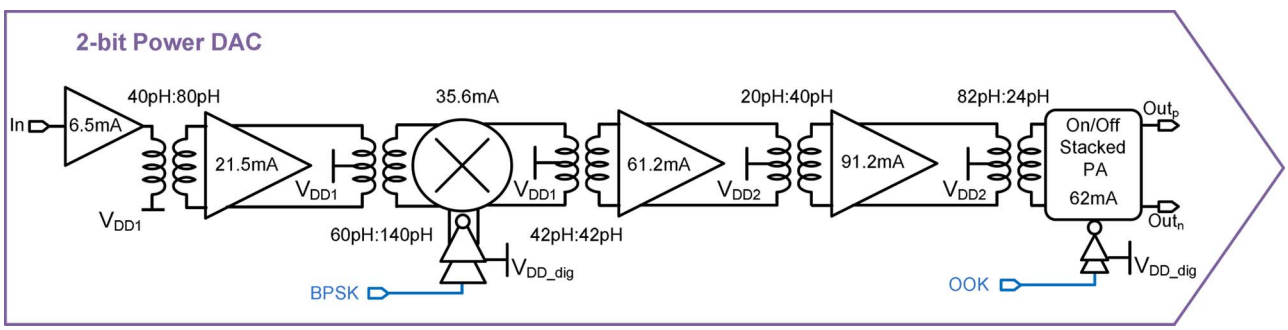

Fig. 2. Block diagram of the 3-state power-DAC array element. The DC current consumption for each stage is indicated when operating under small-signal conditions.

stage of each power-DAC provides single-ended to differential conversion, broadband 50 Ω input impedance matching and several dB of power gain. The signal is then further amplified before being applied to the input of the BPSK modulator. Two more amplifier stages are inserted after the BPSK modulator to boost the signal to a level suitable for the output stage. While large power gain is essential to drive the output stage into saturation for peak PAE performance, the number of amplifier stages after the BPSK modulator should be minimized so that their cascaded bandwidth does not limit the achievable BPSK data rate. Operating the output stage in saturated power mode also ensures that mismatches between the MOSFETs of the output stages of the array elements are the only contributors to variations in the saturated output power, P_{SAT}, between the power-DAC segments of the IQ transmitter array. A tunable hybrid structure similar to the one in [2] can be implemented in order to compensate for phase offsets. Since the OOK modulation is implemented in the output stage, its data rate is limited only by the bandwidth of the output matching network and antenna.

The four OOK and four BPSK baseband data streams are provided through a clocked serial interface and are then deserialized on-chip before being distributed to the appropriate power-DAC element. The BPSK and OOK modulation provided in each array element can produce 3 output states $\{P_{SAT}, 0, -P_{SAT}\}$. If each array element drives a differential antenna, an m-ary QAM output signal with up to 25 constellation symbols can be formed in free-space, at the array zenith, as sketched in Fig. 3. With the exception of the 4 corner symbols of the constellation in Fig. 3, all the other symbols can be generated using two or more baseband bit settings. This redundancy can be exploited to crudely mitigate for inherent mismatches between the array elements. The number of distinct baseband bit settings that can synthesize each of the symbols generated by the 2×2 IQ array is indicated for each symbol in Fig. 3.

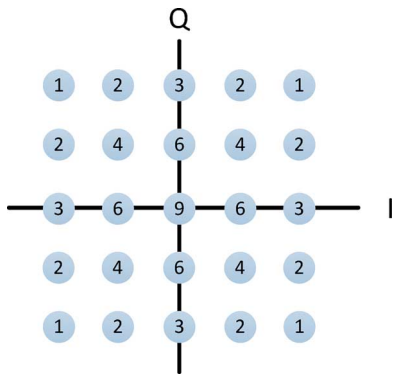

Fig. 3. Signal constellation produced by the 2×2 IQ array transmitter showing the number of redundant bit settings that can be used to generate each particular symbol.

Since the OOK modulation is performed by turning on and off the output stage of the power DAC, this maximizes the power added efficiency of the transmitter for each transmitted symbol, not just for the 4 corner symbols in Fig. 3. For example, when the IQ array transmits the $(\mathrm{P_{SAT}} + 0 \times j\mathrm{P_{SAT}})$ symbol, the output signals of the two Q power-DACs could be $j\mathrm{P_{SAT}}$ and $-j\mathrm{P_{SAT}}$, respectively, thus cancelling each other (at the zenith only), or they could both be turned off, not consuming DC power in the corresponding output stages. By turning off unnecessary array elements when a particular symbol is being transmitted, the undesired sidelobes of the array radiation pattern are also reduced.

In general, several 2×2 IQ array chiplets can be combined in a symmetrical $n \times n$ IQ array transmitter which can produce a total of $(2n+1)^2$ distinct signal constellation symbols. Rather simplistically, a constellation symbol can be described as $(m_I \times \mathrm{P_{SAT}} + j \times m_\mathrm{Q} \times \mathrm{P_{SAT}})$ where m_I and m_Q are integers between $-n$ and n [7]. However, if m_I or m_Q are odd, the peak of the array radiation pattern will be off the array zenith and the corresponding constellation symbols will be somewhat distorted at the zenith. A multi-bit output stage that can compensate for this distortion is discussed elsewhere [2].

III. Building Block Design

Although the block diagram of the W-Band array element in Fig. 2 is similar to that of the array element in [7], the individual block topologies are quite different. The purely digital, class D predriver in [7], consisting of a broadband LO distribution network based on inductively series-peaked CMOS inverters and of the CMOS pass-logic BPSK modulator, both of which operated from DC to 50 GHz, could not be extended to 110 GHz. In the W-band array, the pre-driver and BPSK modulator had to be realized as broadband, tuned analog circuits. Moreover, since the output power requirements were reduced by 6 dB (from 24 dBm at Q band to 18 dBm per array element at W band) this allowed for halving the total gate periphery of the transistors in the output stage and in all preceding stages. The design of the array element started with the power output stage. After the output stage was optimized, an LO amplifier capable of driving it into saturation was implemented.

A. Power Output Stage

Series stacking of SOI CMOS transistor in SOI has been used to increase the output voltage swing, $\mathrm{R_{LOPT}}$, and the output power while preventing transistor breakdown in the Q-band [7], [9], [11]–[15] and more recently has been expanded to the W-band [2], [11], [16]–[18].

The differential output stage, shown in Fig. 4(a) uses the same topology as in the Q-band version, Fig. 4(b), presented in [7] with four series stacked n-MOSFETS. The capacitors in series with the gates of the common gate MOSFETs were reduced, and their layout was optimized to push their self-resonance frequency beyond 100 GHz. The finger width of each MOSFET was reduced from 1.25 μm to 0.77 μm and the overall transistor gate widths were halved. The smaller finger width improves the maximum available gain (MAG) by about 2 dB at 100 GHz, as demonstrated in the simulations of the single-ended versions of the Q-band and W-band output stages, shown in Fig. 5.

The PAE of the output stage is given by:

$$PAE = \eta \times \left(1 - \frac{1}{G}\right) \tag{1}$$

where η is the drain efficiency and G is the power gain. At mm-wave frequencies, even a small increase in gain has a significant impact on PAE. For example, at a drain efficiency of 40% and power gain of 4 dB, the PAE is 24%. Increasing the gain by 2 dB results in a PAE of 30%, an improvement of 25%. As in [11], [13], in order to maximize the gain while simultaneously increasing η, the gate width of the transistors higher up in the stack was progressively reduced by a factor of 1.3. This is particularly beneficial at W band because the impedances of the parasitic capacitance paths to ground become very small and result in signal current leaking to ground rather than flowing into the output node. Simulations of a single-ended version of the output stage show that gate periphery tapering increases the MAG from 10.6 dB to 16 dB at 100 GHz when compared to an output stage in which all MOSFETs have an identical size of $4 \times 52 \times 40$ nm $\times$ 0.77 μm. The reduced parasitics improve the peak PAE from 16.3% to 23.47% while the simulated saturated output power $(\mathrm{P_{SAT}})$ remains the same: 17 dBm. The $\mathrm{P_{SAT}}$ is determined by the size of the bottom transistor which is identical in both cases. The output stage with tapered gate periphery also has 2 dB higher small-signal gain $(\mathrm{S_{21}})$. Tapering also increases the optimum load impedance from 5.9 Ω to 14.9 Ω which helps reduce the losses in the output matching network.

Unlike in the Q-Band version, the gate capacitors are set to 400 fF throughout the output stage. The low transistor gain at W-band prevents the drain-source and drain-gate voltage swing on the output transistor from reaching high enough levels for transistor breakdown to occur, thus eliminating the need to reduce the gate capacitor sizes higher up in the stack. The 400 fF capacitors act as AC shorts at W-band maximizing the small-signal gain. The resistive divider provides the DC bias voltages to each gate in the output stage which satisfy the following condition:

$$V_{G,n} = \left(\frac{n-1}{n} V_{DD} + V_{GS,1}\right), \quad n = 1, 2, 3 \ldots N \tag{2}$$

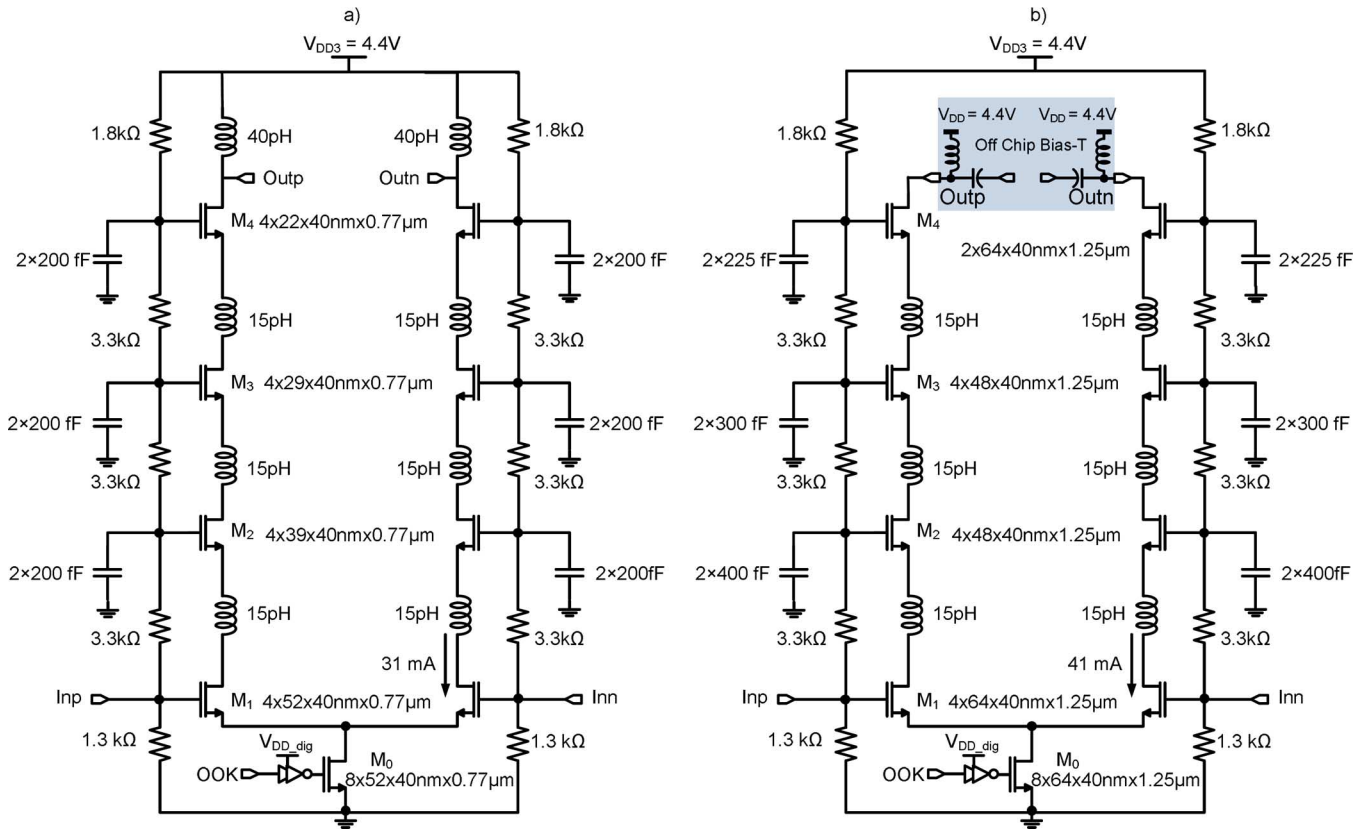

Fig. 4. Schematic of the a) W-Band and b) Q-Band differential power output stages.

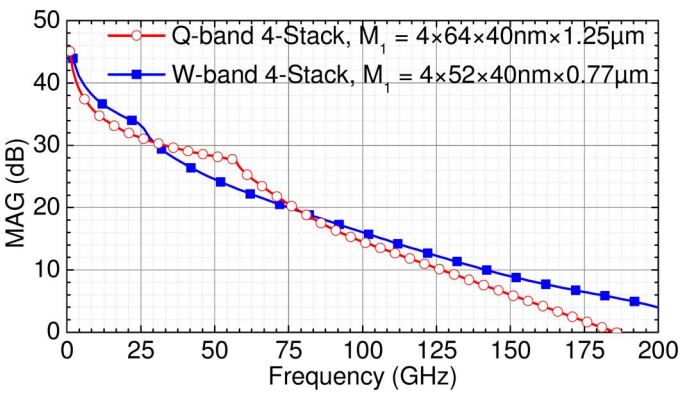

Fig. 5. Simulated MAG of the Q-Band [7] and new W-band n-MOS series stacked power output stage after layout extraction.

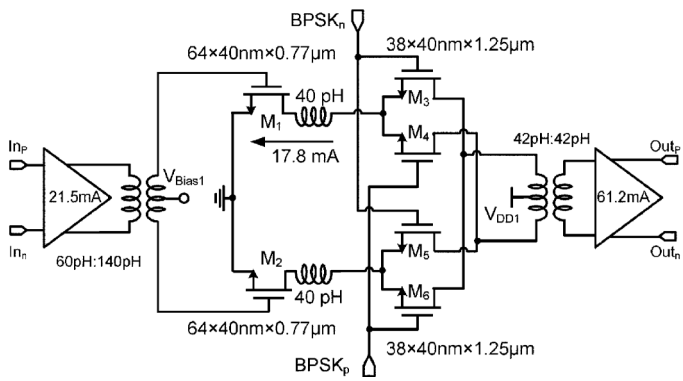

Fig. 6. Schematic of the BPSK modulator [11].

where $V_{GS,n}$ is the DC gate voltage of the n^{th} transistor and V_{DD} is the supply voltage (4.4 V in this case). $V_{GS,1}$ is the gate source bias voltage of the bottom common source transistor and it is set to 0.4 V for class AB operation. The resistive divider plays no role in the W-band response of the output stage.

B. BPSK Modulator

The BPSK modulator is biased from a 1.1 V supply and is implemented using the double-balanced telescopic Gilbert cell topology [19] with inductive broadbanding depicted in Fig. 6. The LO signal is applied at the gates of M_1 and M_2 and the baseband data to the gates of the mixing quad MOSFETs (M_{3-6}). This arrangement maximizes the W-band power gain since the LO signal passes through a cascode stage, whereas the baseband data are applied to the common gate nodes where larger capacitances can be tolerated. M_1 and M_2 are biased for maximum power gain and linearity at 0.36 mA/μm which corresponds to the peak $-\mathrm{f}_{\mathrm{MAX}}$ current density at a V_{DS} of 1.1 V [7]. Transistors M_1 and M_2 have a finger width of 0.77 μm for maximum gain while a larger, 1.25 μm, finger width was used for transistors M_{3-6} in order to decrease their lateral footprint and minimize the output capacitance. Transistors M_{3-6} act as switches. A 40 pH inductor was used to absorb the input capacitance of the mixing quad and the output capacitance of the transconductor pair $\mathrm{M}_1-\mathrm{M}_2$ into an artificial transmission line. Some parasitic capacitance and parasitic inductance asymmetry is inherent to the layout of the Gilbert cell due to the metal crossing at the

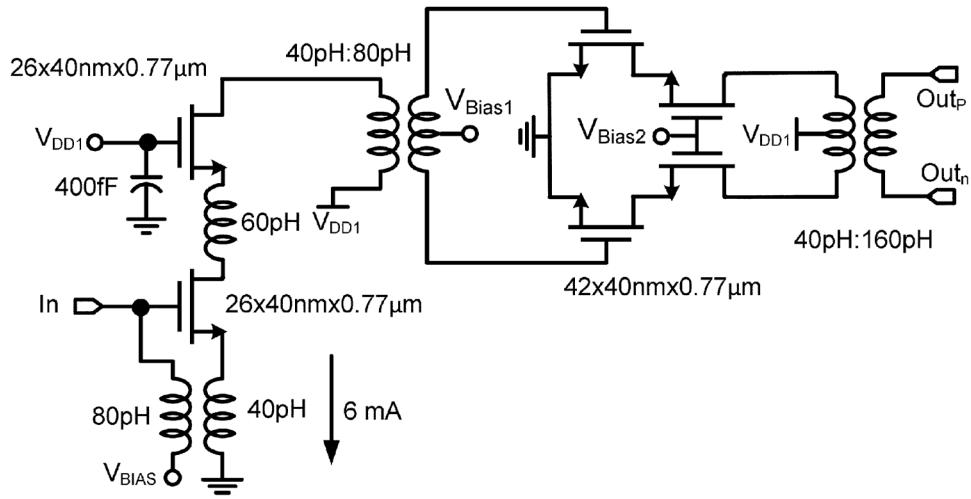

Fig. 7. Schematic of the first two stages of the LO amplifier.

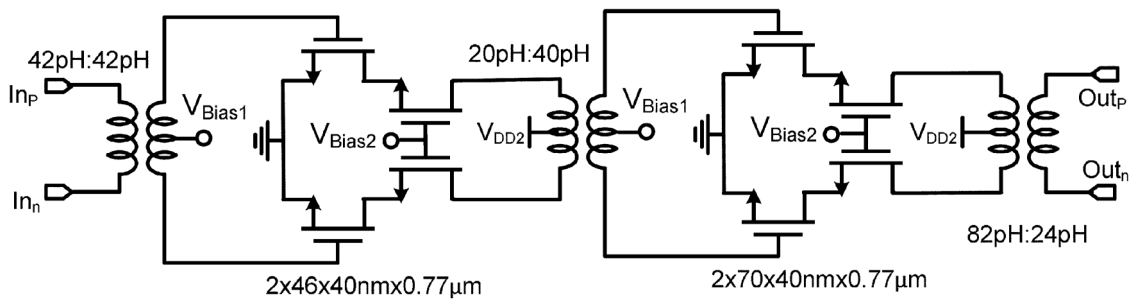

Fig. 8. Schematic of the last two LO amplifier stages.

output of the mixing quad. This asymmetry introduces phase and amplitude errors, as shown in the experimental section.

Baluns are employed to couple the differential LO signal in and out of the modulator while suppressing common-mode leakage. Similar to the mixing-quad layout asymmetries, common-mode signal feedthrough due to an imperfect differential LO signal can cause both amplitude and phase errors and is particularly challenging to overcome at mm-wave frequencies. While the amplitude error between the two states of the BPSK modulator is attenuated by the limiting action of the following amplifier stages, the phase error propagates to the output and causes EVM degradation. As mentioned, the BPSK modulator should ideally be placed close to the output stage in order to avoid limiting the bandwidth of the BPSK-modulated carrier. However, it was determined that two gain stages were essential to raise the level of the external LO signal to properly drive the output stage.

C. LO Amplifier

The LO amplifier consists of five stages, one of them being the BPSK modulator. The first two stages, depicted in Fig. 7, operate from 1.1 V and the final two stages use a 2.2 V supply which maximizes the gain and allows for a larger swing needed to drive the output stage into saturation. The schematic of the last two stages is shown in Fig. 8 along with the transformer ratio. Symmetrical baluns are used between stages for impedance matching and for common-mode rejection. The bias voltage is provided to the gates of the common source transistors through the center tap of the input balun. A transistor size ratio of 1.7 is used between stages in order to maximize the signal power and power gain while minimizing the number of amplifier stages. Once the transistor sizes were chosen, each amplifier stage was first layed out and full parasitic extraction was performed before sizing the interstage transformers for best matching.

With the exception of the first, all other stages use a differential cascode topology. The first stage features a single-ended cascode with shunt-series transformer feedback [20]. Unlike in [20] where noise figure and input matching were the main design priorities, the MOSFETs in the cascode are sized for broadband input matching and biased at the peak f_{MAX} current density for maximum gain. The inductive load was replaced with a balun in order to provide the single-ended-to-differential conversion needed to drive the following differential stage.

D. Baseband Data Paths

Since one of the goals of this study was to demonstrate the highest possible modulation rate for a wirelesss transmitter, while, at the same time, achieving data-rate scalable power consumption, the baseband data lane introduced in [7], [13] was optimized for the highest bandwidth. Each data lane consists of a custom, inductively series-peaked CMOS inverter chain with a fanout of at most 1.5 and suitably sized to drive the BPSK modulator and the OOK input of the large power output stage

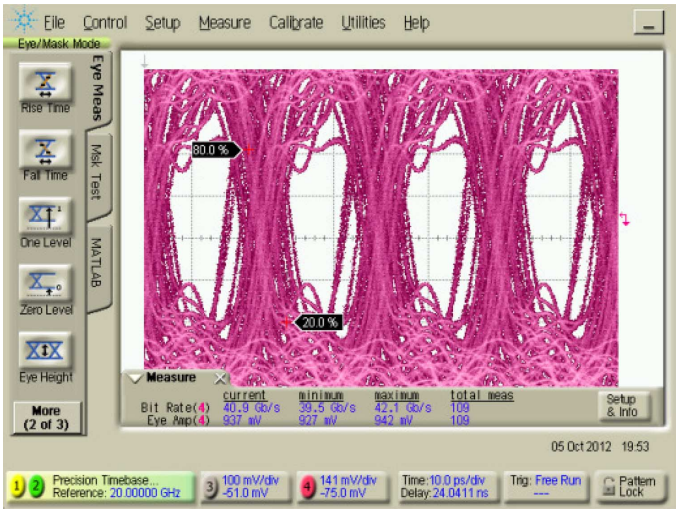

Fig. 9. Measured 40 Gb/s eye diagram at the output of a data path breakout driving 50Ω [8].

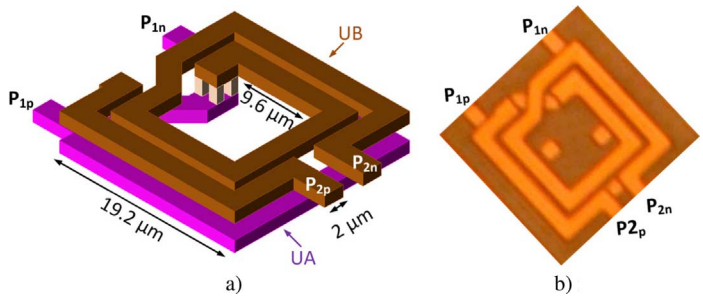

Fig. 10. a) To-scale 3-D layout view of the 34 pH:73 pH transformer as well as b) micrograph of the implemented transformer.

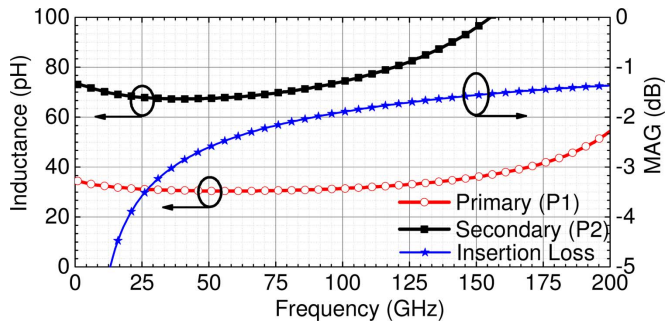

Fig. 11. Simulated performance of the 34 pH:73 pH transformer.

described earlier. Additional inverters were introduced on the OOK paths in order to compensate for the extra delay seen by the BPSK bit as it travels through the BPSK modulator and the two amplifier stages before reaching the output stage. The extra inverters were also necessary to accommodate the higher load capacitance provided by the M_0 switch in Fig. 4. The timing of the BPSK and OOK data bits is critical in ensuring that the carrier is synchronously modulated in amplitude and in phase at 40+ Gbaud. A circuit consisting of an input TIA and a series peaked CMOS inverter chain described in [7], [13], was fabricated as a stand alone breakout to test the performance of the baseband data lane. Measurements, reproduced in Fig. 9, prove that it is capable of over 40 Gb/s operation driving a 50 Ω load rail-to-rail, with over 1.1 V swing.

In order to evaluate the maximum achievable data rate per power-DAC lane, a standalone 3-state power-DAC element was fabricated in which the OOK and BPSK bits are directly supplied by external signal sources, removing the need for the on-chip deserializer which limits the maximum achievable data rate. The external data signals were amplified by the TIA and then reshaped by the scaled CMOS inverter chains described earlier.

In the transmitter array, the external clock (CLK) and the serialized data (DATA) signals for the 8 data paths are first amplified using the TIA input stage. The data are then retimed using standard logic cells available in the design kit before being fed to an 8-bit shift register that acts as a deserializer. The outputs of the shift register are again retimed using eight phase shifted versions of an on-chip generated clock (CLK8), which is a divide-by-eight version of the external CLK. The retimed and deserialized OOK and BPSK data are then distributed to the appropriate power-DAC element using scaled CMOS inverter chains. Simulations show that the deserializer can operate with a maximum CLK signal of 10 GHz for a maximum data rate of 1.25 Gb/s for each OOK and BPSK bit. The digital data path consumes a static power of 11 mW mostly due to the two TIAs used at the input of the CLK and DATA paths. It is estimated that the dynamic power consumption of the data path is 1.5 mW when using a 1 GHz CLK and 15 mW for a 10 GHz clock.

IV. Fabrication

The IQ transmitter array, one array element with high-speed data pads, and building block breakouts were fabricated in two different fabrication runs of a commercial 45 nm SOI CMOS technology featuring a copper back-end-of-line (BEOL) with 11 metal layers. The topmost metal (LB) is 2.2 μm thick aluminum. Two 1.2 μm thick copper layers (UA and UB) are also available. A more detailed cross section of the BEOL can be found in [21].

All circuits use only minimum gate length (i.e., 40 nm) floating-body MOSFETs because of their higher f_T/f_{MAX} over body-tied transistors [22]. Measurements of a fully wired (up to LB) 40 × 40 nm × 0.77 μm n-MOSFET show f_T/f_{MAX} of 243/244 GHz [7]. Vertical Natural Capacitors (VNCAPs), which are formed using interdigitated metal fingers, were used throughout.

Transformers and baluns were formed in the UA and UB layers which provide the best trade-off between coupling and quality factor (Q) when using a vertically stacked balun topology. A to-scale view of the 34 pH:73 pH transformer and the corresponding micrograph can be seen in Fig. 10. Simulations of the transformer, in Fig. 11, show an insertion loss (i.e., MAG) better than 2 dB from 90 and 200 GHz, with a self-resonance frequency (SRF) over 200 GHz.

Throughout the chip, the supply and ground are distributed using a multi-layered metal mesh formed of 5 × 5 μm^2 unit cells, similar to the one described in [23]. Even-numbered metals shunted together provide the supply voltage while

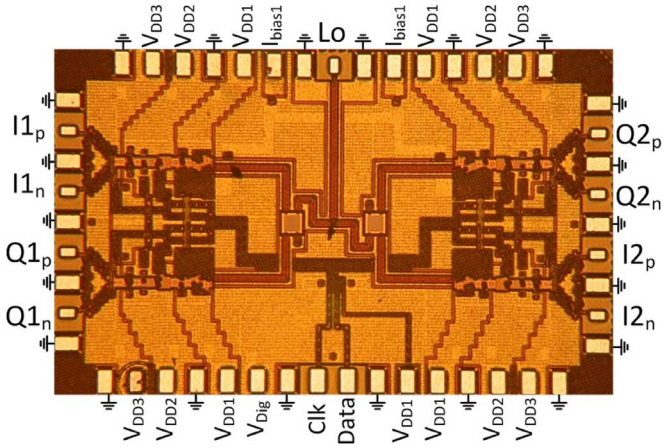

Fig. 12. Die micrograph of the 2×2 IQ transmitter array chiplet.

odd-numbered metals are employed for the ground. This arrangement reduces the ground and supply inductance and resistance while simultaneously providing distributed power supply decoupling.

The die photograph of the 2×2 IQ transmitter array is shown in Fig. 12. It occupies an area of 1850 μm × 1150 μm and is pad limited.

V. Experimental Results

A. Building Block Breakouts

All the measurements presented in this section were conducted on wafer in a 50 Ω environment. Different vector network analyzers (VNAs) were used for W-band and D-band measurements, which explains the measurement discontinuities seen at the 110 GHz transition frequency. In order to characterize the performance of the output stage of a power-DAC element, two single-ended versions of the output stage were manufactured with and without the on-chip output matching inductor. The measured and simulated S-parameters and MAG of the output stage without matching inductor show excellent agreement, validating the transistor model accuracy even at D-band. Although, the measured S_{21} in Fig. 13 shows good agreement with simulation, it is immediately apparent that modelling of the loss of the output inductor is not as good, with the measured gain being 1.5 dB lower than simulation. The S_{21} of the single-ended output stage with the on-chip output inductor is larger than that of the same stage without output matching and remains larger than 0 dB from 67 GHz to 110 GHz, even in the absence of an input matching network. However, the peak gain is only 3 dB at 88 GHz, much smaller than the measured MAG of 11 dB. The difference between the measured S_{21} and measured MAG is due to the lack of input matching network in the output stage breakout.

A breakout of the LO amplifier, with its output matched to 50 Ω using a transformer, was fabricated in the first run. This version of the LO amplifier, minus the output matching transformer, was also used in the 3-state power-DAC breakout in [11]. At room temperature, the LO amplifier breakout has a measured peak gain of 20 dB and a 3 dB bandwidth extending from 100 to 113 GHz, as illustrated in Fig. 14. The maximum

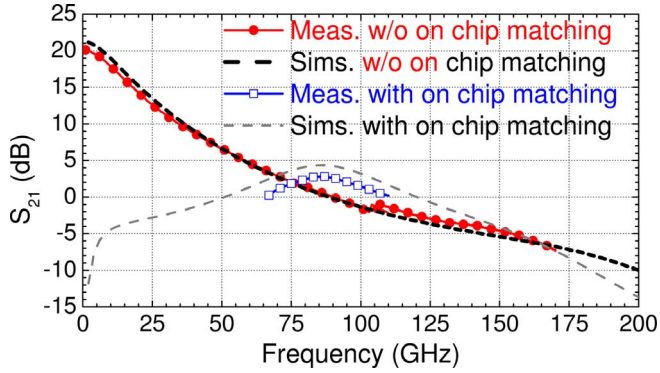

Fig. 13. Comparison of the measured and simulated S_{21} of a single ended output stage breakout, with and without the output matching inductor.

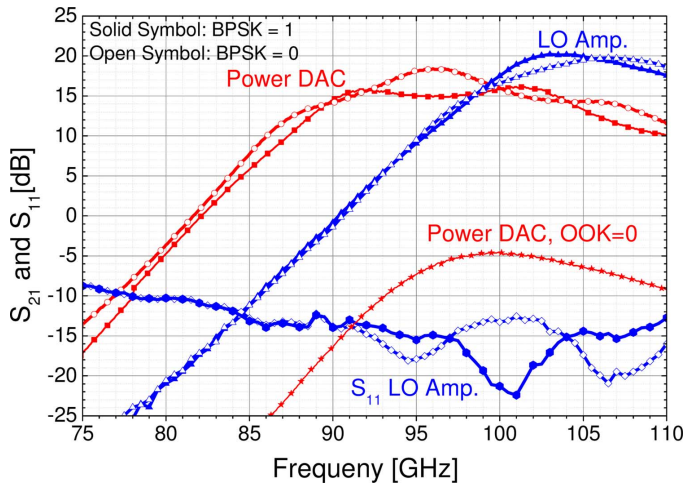

Fig. 14. Single-ended S-parameter measurements of the power DAC and LO amplifier for the three BPSK/OOK modulator settings.

gain reduces to 12.6 dB when measured at 100 °C. S_{11} remains better than −10 dB over a 50 GHz bandwidth, demonstrating the excellent matching capabilities of the shunt-series transformer feedback topology used in the input stage.

B. 3-State Power-DAC Breakout

S-parameter measurements of a new 3-state power-DAC breakout from the second fabrication run, with the LO amplifier tuned 5 GHz lower in frequency, are shown in Fig. 14 and compared with those of the original LO amplifier for all three possible BPSK and ASK settings. The differential gain of the power-DAC is 21.4 dB with a 3 dB bandwidth from 89 to 105 GHz, or from 92 to 101 GHz, depending on the BPSK setting. Imperfect single-ended-to-differential conversion in the second LO amplifier stage as well as layout asymmetries in the BPSK modulator itself are responsible for the gain variation between the two BPSK settings. The amplitude imbalance between the two BPSK settings was measured under both large-signal and small-signal conditions and plotted versus frequency in Fig. 15. When operating in small-signal mode, the maximum amplitude imbalance of the LO amplifier breakout is 1.8 dB and increases to 3.4 dB for the 3-state power-DAC breakout. However, the amplitude imbalance is corrected when the LO amplifier and output stage operate in saturation, with a

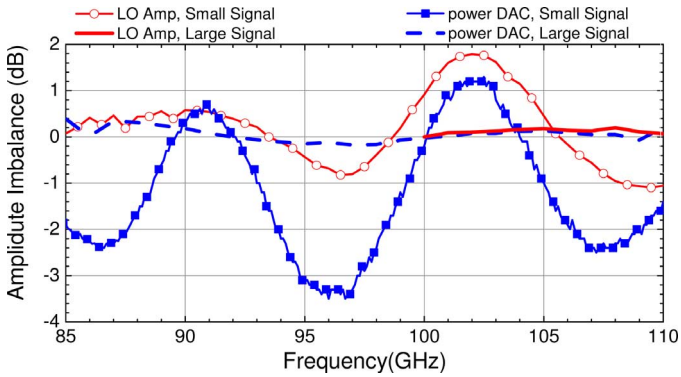

Fig. 15. Measured amplitude imbalance for the two BPSK modulator settings from both large and small-signal measurements.

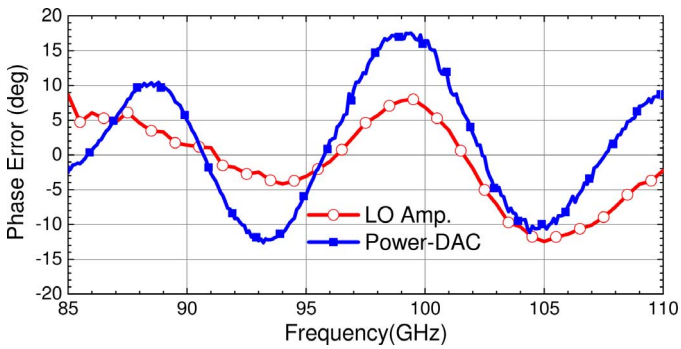

Fig. 16. Measured phase error for the two BPSK modulator settings from small-signal measurements.

maximum amplitude imbalance of 0.2 dB and 0.4 dB for the LO amplifier and power DAC, respectively. The phase error between the two BPSK settings was obtained from S-parameter measurements and plotted as a function of frequency in Fig. 16. The maximum phase error across the 85 to 110 GHz band is 12.4 degrees for the LO amplifier and 16.5 degrees for the power DAC.

Large signal output power and gain measurements are shown in Fig. 17. The LO amplifier has a peak saturated output power of 11.7 dBm at 105 GHz while the power-DAC provides 11.8 dBm at 96 GHz and 8.9 dBm at 105 GHz. The comparison is somewhat obscured by the fact that the LO amplifier breakout is tuned at a higher frequency than the LO amplifier in the 3-state power-DAC breakout.

C. 2×2 IQ Transmitter Array

The ON/OFF ratio, which defines the dynamic range of the power-DAC array element, was characterized for each of the four power DACs and for both the positive and negative terminals of their differential outputs. The measurement results, reproduced in Fig. 18, show that the dynamic range of the power DACs is better than 24.4 dB between 86 and 110 GHz. Over the same frequency range, the output power variation between the 8 outputs for all BPSK settings is less than 1.8 dB. The output power variation is largest at the edges of the frequency range, Fig. 19. This is due to the fact that the power DAC has less gain and the output stage is not driven in saturation at these frequencies. The smallest P_{out} variation between the array elements of

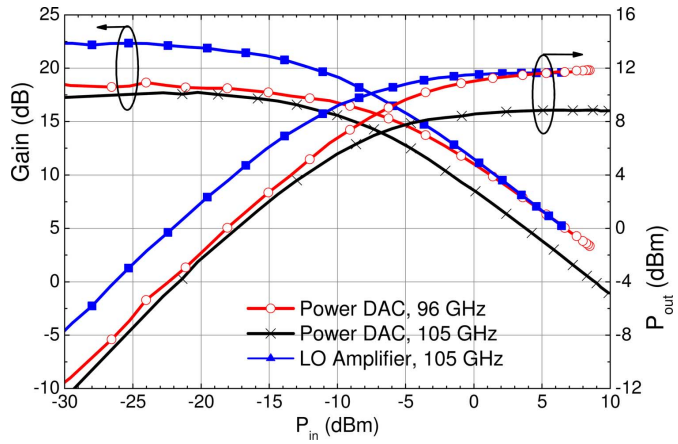

Fig. 17. Measured output power and large-signal gain of the LO amplifier breakout and of the 3-state power DAC.

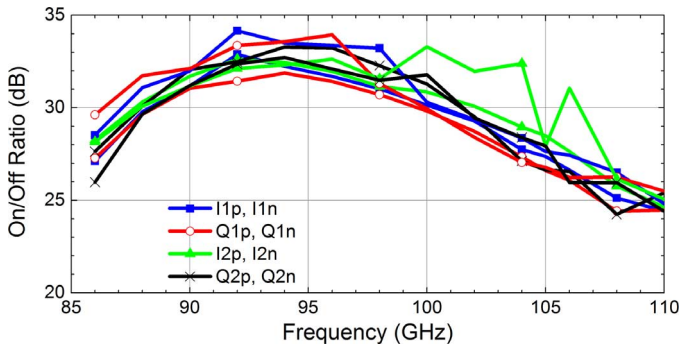

Fig. 18. Measured On/Off ratio for each of the 8 outputs of the 2×2 IQ transmitter array.

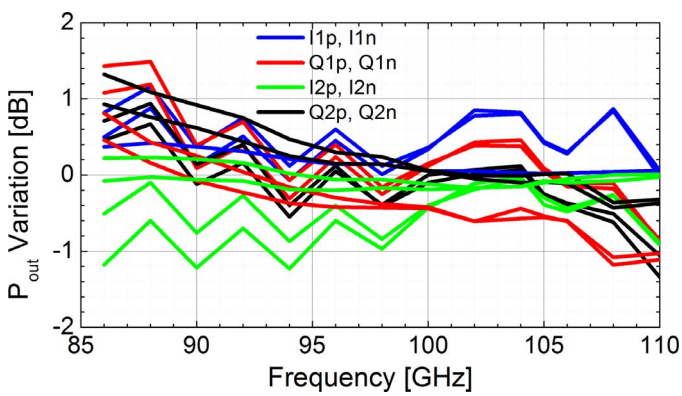

Fig. 19. Measured variation in P_{out} for each of the 8 outputs of the the 2×2 IQ transmitter array for the two BPSK settings. Output I_{1p} with $BPSK = 0$ is taken as the reference.

0.6 dB is observed at 96 GHz, coinciding with the peak gain frequency of the power-DAC.

The P_{out} of the 4 power-DACs in the array was measured while the BPSK and ASK bits were manually swept. Using the phase error from the S-parameter measurements, the constellation in Fig. 20 was mathematically constructed. Measurements at carrier frequencies of 94, 102, 104, 105 and 106 GHz are superimposed to illustrate the worst-case spread that would occur for a BPSK/ASK modulation bandwidth of 12 GHz. The overall EVM is calculated to be 9.0%

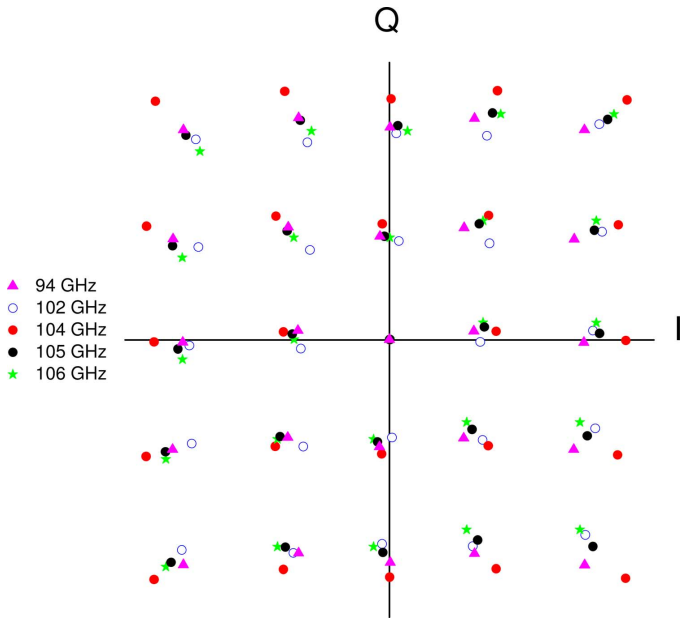

Fig. 20. Constructed constellation from P_{out} measurements of the the 2×2 IQ transmitter array at 94 GHz, 102 GHz, 104 GHz, 105 GHz and 106 GHz.

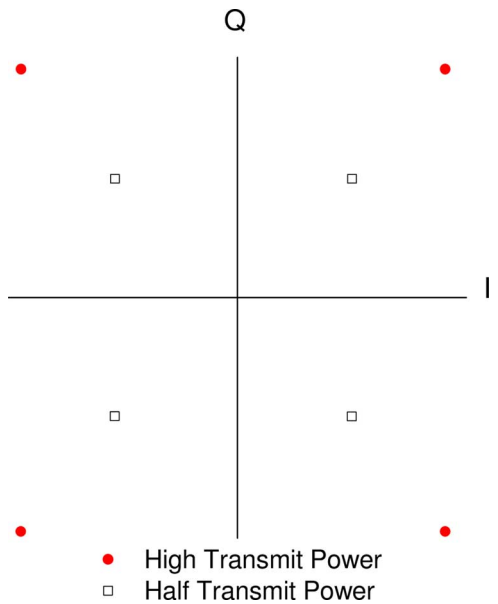

Fig. 21. Constructed constellation of all the generated points at 96 GHz from P_{out} measurements of the 2×2 IQ transmitter array. Phase information from S-parameter measurements was also incorporated.

Fig. 21 illustrates how the 2×2 IQ transmitter array can generate a QPSK constellation at 96 GHz at maximum output power and maximum PAE when all 4 array elements are on (ASK bits set to logic 1) as well as a second QPSK constellation at half the output power with only one IQ pair of elements on (ASK bits set to logic "1") and the other pair of power-DAC elements being turned off (ASK bits set to logic "0"). For maximum output power transmission the EVM is calculated to be 2.5% with a PAE of 1.7% for the whole 2×2 array. For half output power, the EVM is calculated to be 3.4% with a PAE of 0.8%.

The maximum bandwidth of the OOK and BPSK data paths was determined by applying sinusoidal signals at the data inputs and different carrier frequencies at the LO input. As shown in Fig. 22, the data paths have at least 29 GHz modulation bandwidth when a 110 GHz carrier is employed. This measurement is limited by the VNA setup which cannot display wider spectra at W-band. Even in this experiment, the upper sideband of the 110 GHz carrier modulated by a 29 GHz sinusoid in amplitude or in phase cannot be captured by the VNA. Finally, the 3-state power-DAC element was tested by applying a PRBS-7 pattern at the BPSK and OOK data inputs for different W-band carrier frequencies. Fig. 23(a). shows the output spectra a 105 GHz carrier with 5 Gb/s BPSK modulation and 39.4 MHz (5 Gbps/2^7-1) tone spacing, while the lower sideband of a 110 GHz carrier BPSK-modulated by a 44 Gb/s PRBS-7 pattern and 346 MHz (44 Gbps/2^7-1) tone spacing is shown in Fig. 23(b). The maximum data rate was limited to 44 Gb/s by the available PRBS generator. The spectra shown in Fig. 23 are not de-embedded and include the loss of the output probe, waveguide to coaxial transitions and the loss of the VNA downconverter.

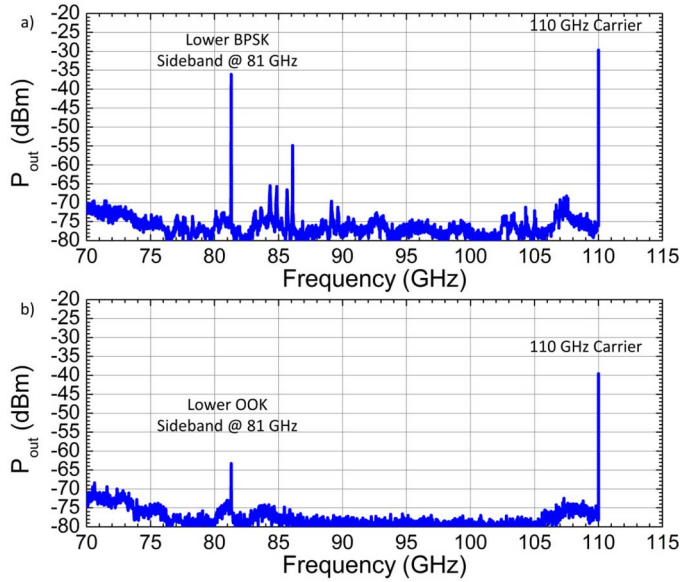

Fig. 22. Measured, non-de-embedded spectra for a 110 GHz carrier with a) 29 GHz sinusoidal BPSK modulation and b) 29 GHz sinusoidal OOK modulation.

VI. Conclusions

A 2×2 IQ transmitter array capable of arbitrary 44 Gbaud QAM-modulation of a W-Band carrier was manufactured and characterized at W-band. Simultaneous OOK and BPSK modulation with record 29 GHz sinusoidal inputs and 44 Gb/s PRBS patterns was demonstrated at carrier frequencies in the 100–110 GHz range. Each power-DAC element is capable of transmitting a peak saturated power of 11.7 dBm at 96 GHz. The measured output power variation between the power-DAC elements of less than ±1.4 dB over a 24 GHz bandwidth suggest that the transmitter array architecture is resilient to device mismatches, IQ-hybrid design imperfections and differential circuit layout inductive and capacitive parasitic asymmetries. An array element output power ON/OFF ratio better than 24 dB was observed over the 85–110 GHz band which is sufficient

TABLE I
PERFORMANCE COMPARISON OF W-BAND TRANSMITTERS.

Ref.	[10]	[24]	[2]	[5]	[25]	[4]	[3]	[8]	[1]	[26]	[27]	**This Work**
Tech.	65 nm CMOS	40 nm CMOS	45 nm SOI	65 nm CMOS	180 nm BiCMOS	45 nm LP CMOS	65 nm CMOS	45 nm LP CMOS	40 nm CMOS	100 nm InP HEMT	40-nm CMOS	45 nm SOI
f_{MAX} [GHz]	--	--	244	--	270	--	--	--	--	350	--	244
Freq. [GHz]	60	70.3-85.5	85-95	86.5-87.5	70-100	100	116	114.3	122.5	115-135	135	100-113
Data [Gb/s]	6	5	8x15	2.5	10	5	10	10	10	10	10	4×2×29 GHz sinusoidal
Mod.	QPSK 16 QAM	QPSK QAM	M-ary QAM	QPSK	16 QAM 32 QAM	ASK	8QAM	QPSK QAM	ASK	BPSK	ASK	BPSK OOK
P_{sat} [dBm]	9.6	20.4	19	> 6.5	>6	0.1	> 6.5	3**	0.1	--	0.1	11.7
Power [mW]	382	375	--	212	500*	28	200	220	28.3	400	17.9	870 per array element @ 2×29 GHz

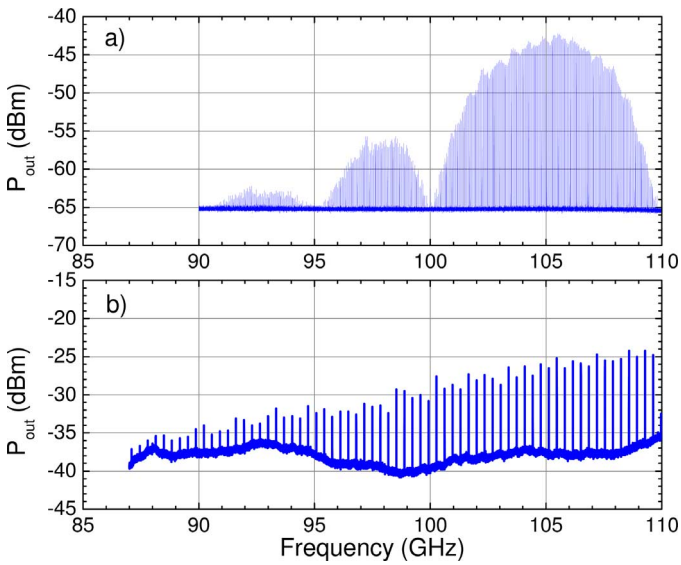

Fig. 23. Measured a) 105 GHz carrier with 5 Gb/s BPSK and b) 110 GHz carrier with 44 Gb/s BPSK PRBS-7 modulation.

to synthesize 16-QAM or higher-order constellations in free space. A comparison with recently reported W- and D-Band band transmitters with direct amplitude or phase modulation is provided in Table I.

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Andreea Balteanu (S'10) is currently pursuing the Ph.D. degree at the University of Toronto under the supervision of Prof. Sorin Voinigescu. She received the B.A.Sc. degree in electrical engineering from the University of Waterloo in 2007 and the M.A.Sc degree in 2010 from the University of Toronto. Her research interests include the design of high speed and millimeter-wave integrated circuits.

At the 2012 IEEE International Microwave Symposium, she received the Best Student Paper Award. Ms. Balteanu has previously held internship positions at IBM T. J.Watson Research Center, Altera Corp. and Texas Instruments Inc.

Stefan Shopov (S'09) received the B.Eng. and M.A.Sc. degree in electrical engineering from Carleton University, Ottawa, ON, Canada, in 2009 and 2011, respectively. He is currently pursuing the Ph.D. degree at the Department of Electrical and Computer Engineering, University of Toronto, ON, Canada.

He has previously held internship positions at NXP Semiconductors, Zurich, Switzerland, and at the National Research Council, Ottawa, ON, Canada. His research interests include silicon power amplifiers, integrated passive components, and millimeter-wave integrated circuits.

Sorin P. Voinigescu (M'90–SM'02) received the M.Sc. degree in electronics from the Polytechnic Institute of Bucharest, Romania, in 1984, and the Ph.D. degree in electrical and computer engineering from the University of Toronto, Canada, in 1994.

Between 1994 and 2002 he was first with Nortel Networks and later with Quake Technologies in Ottawa, Canada, where he was responsible for projects in high-frequency characterization and statistical scalable compact model development for Si, SiGe, and III-V devices. He later conducted research on wireless and optical fiber building blocks and transceivers in these technologies. In 2002 he joined the University of Toronto, where he is a full Professor. His research and teaching interests focus on nano-scale semiconductor devices and their application in integrated circuits at frequencies beyond 300 GHz. In 2008-2009 he spent a sabbatical year at Fujitsu Laboratories of America, Sunnyvale, CA, USA.

Dr. Voinigescu is a member of the ITRS RF/AMS Committee and of the TPCs of the IEEE CSICS and BCTM. He received NORTEL's President Award for Innovation in 1996 and is a co-recipient of the Best Paper Award at the 2001 IEEE CICC, the 2005 IEEE CSICS, and of the Beatrice Winner Award at the 2008 IEEE ISSCC. His students have won Student Paper Awards at the 2004 VLSI Circuits Symposium, the 2006 SiRF Meeting, RFIC Symposium and BCTM, and at the 2008 and 2012 International Microwave Symposium.