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Harnessing the unique features of FDSOI CMOS technology in fibreoptic, millimetre-wave, and quantum computing circuits from 2 K to 400 K

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Mm-wave
Semiconductor quantum dot
Silicon germanium
Stacked cascode amplifier
Switch
Transimpedance amplifier (TIA)

A B S T R A C T

Starting with the full characterization of the *n*- and *p*-MOSFETs in a 22-nm FDSOI CMOS process from DC and S-parameter measurements over temperature in the 2 K to 400 K range, we develop circuit design guidelines and design methodologies for digital, analog mixed-signal and mm-wave circuit building blocks that take advantage of the unique features of FDSOI transistors enabled by the presence of the back gate and buried oxide. A constant-current–density-to-backgate-voltage-conversion bias circuit, operating across the entire temperature range is demonstrated to optimally bias CMOS inverters in a variety of digital, analog-mixed-signal and mm-wave circuits for different use scenarios that optimize noise, gain, linearity, and/or bandwidth. Measurement data and constant current density design methodologies are used to illustrate the design of transimpedance amplifiers for qubit readout and fibreoptic receivers, broadband switches, mm-wave time-interleaved ADC samplers, large-swing DACs, and power amplifiers.

1. Introduction

FDSOI CMOS offers unique features in the form of MOSFET back gate bias and DC isolation from the silicon substrate which set it apart from competing FinFET and SiGe BiCMOS technologies. Characterization of FDSOI MOSFETs up to 125 °C [1] and at cryogenic [2–5] temperatures shows excellent performance over the entire range from 2 K to 400 K, making it an interesting technology for a wide range of applications. For example, it can be used in large-swing DACs [6] to replace FinFET DACs and the linear, broadband, large-swing SiGe BiCMOS optical modulator driver, and thus reduce the power consumption and improve the energy efficiency per bit of a dual-polarization, 64-GBaud fibreoptic transmitter with QAM-16 or QAM-32 modulation, as illustrated in Fig. 1. It can also compete with 5-nm FinFET and SiGe BiCMOS technologies for the TIAs [7,8] and provides a lower cost alternative to 5-nm FinFET technologies in the ADC using the architecture in Fig. 2 [9,10]. CMOS TIAs with competitive power consumption and input-referred noise current at similar bandwidths as SiGe BiCMOS TIAs have also been reported [11], offering the opportunity for the fibreoptic receiver to be fully implemented in FDSOI as well. FDSOI technology is already used in 77-GHz automotive radar transceivers [12] and has demonstrated excellent performance in radio [13] and radar transceivers at D-band, Fig. 3, [14]. Finally, for emerging quantum computing applications, FDSOI CMOS is the only technology which offers the capability to compensate for the MOSFET threshold voltage increase at 1–4 K from the back gate to maximize the performance and minimize the power consumption of the cryogenic classical controller to less than ~ 1 W. The latter is needed to comply with the power lift of state-of-the-art cryostats and to avoid increasing the physical temperature of the qubits in the quantum core, which would compromise the fidelity of the quantum gates. Additionally, FDSOI CMOS technology offers a promising platform for the implementation of semiconductor quantum dot qubits [15], paving the

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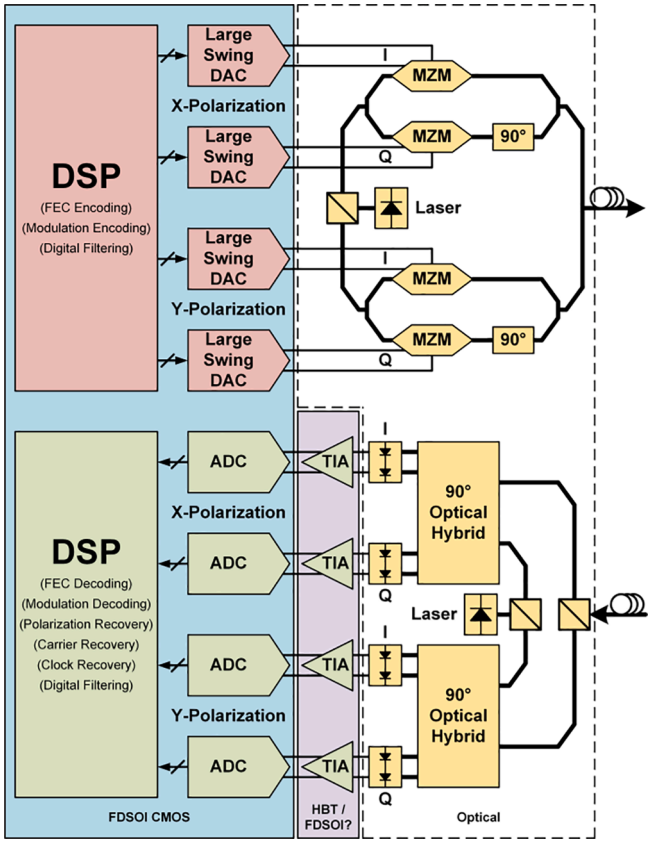


Fig. 1. Block diagram of dual-polarization fibreoptic system with 16-QAM or higher order modulation.

path for a monolithically integrated quantum processor unit (QPU) such as that proposed in Fig. 4, where the qubits and control/readout electronics are integrated on the same die. Such a monolithic implementation has been suggested by several groups [16–19] as the means of overcoming the interconnect bottleneck which has thus far contributed to the limited number (50–127) of qubits in state-of-the-art quantum processors [20].

The article is organized as follows. Section 2 describes the DC and S-parameter measurement characterization of the MOSFETs in a production 22-nm FDSOI CMOS technology from 2 K to 400 K. The measured MOSFET behaviour over temperature and unique-to-FDSOI features are then used to guide the design of a variety of circuit topologies for fibreoptic, mm-wave, and quantum computing applications in Section 3. The significance of the work is discussed in the Conclusion.

2. FDSOI transistor characterization

A full set of super-low threshold voltage (SLVT) *n*- and *p*-MOSFETs with different gate length (L_g), finger width (W_f), and number of gate fingers (N_f) and different contact-poly-pitch (CPP) were characterized at temperatures from 2 K to 400 K in two variants, with thin and thick metal back-end-of-line (BEOL), of the 22-nm FDSOI CMOS process studied in this work [21]. The *n*- and *p*-MOSFET cross sections are depicted in Fig. 5a, while Fig. 5b, illustrates how the *n*-MOSFET back gate voltage bias is applied through a reverse biased n-well. The *p*-MOSFET backgate voltage is applied via a p-well isolated from the substrate by a deep n-well (Fig. 5c) which may either be merged with the n-well of the *n*-MOSFET for more compact layouts or separate to enable independent biasing.

Fig. 6 shows a microphotograph of a portion of a sample die containing transistor test structures intended for DC and millimetre-wave S-parameter characterization. Fig. 7 depicts a sample MOSFET test

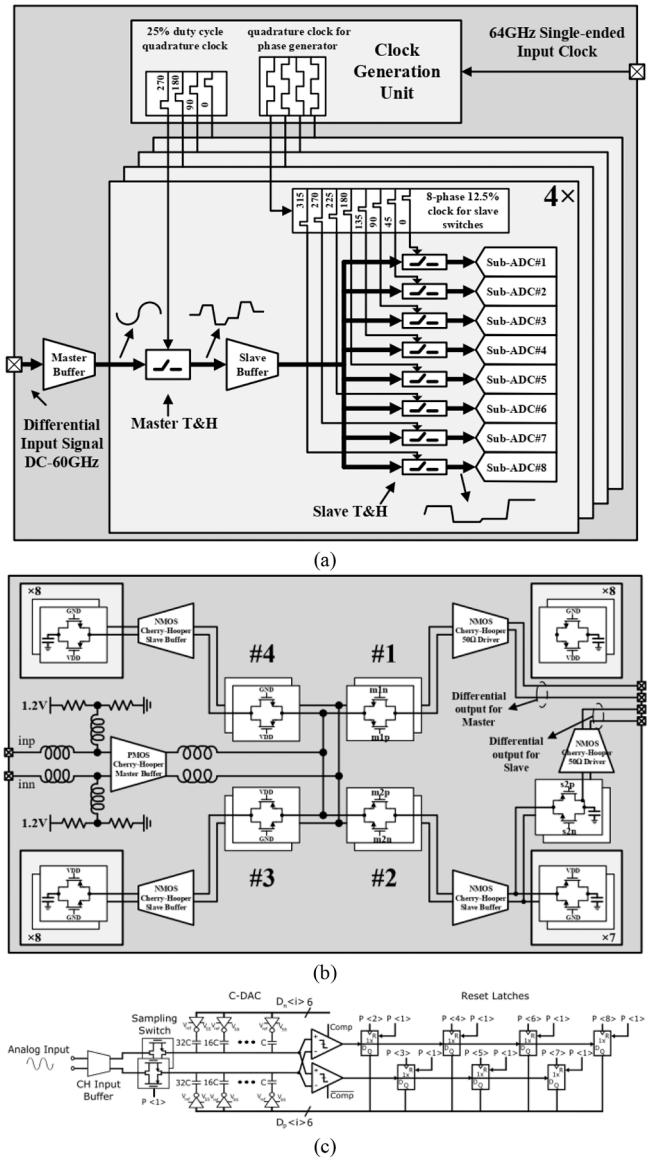


Fig. 2. a) Block diagram of proposed ADC architecture incorporating b) an ADC front-end and Sub-ADC lanes composed of c) the SAR ADC [9,10]. The output of the master and slave TH stages are indicated on the right side of (b).

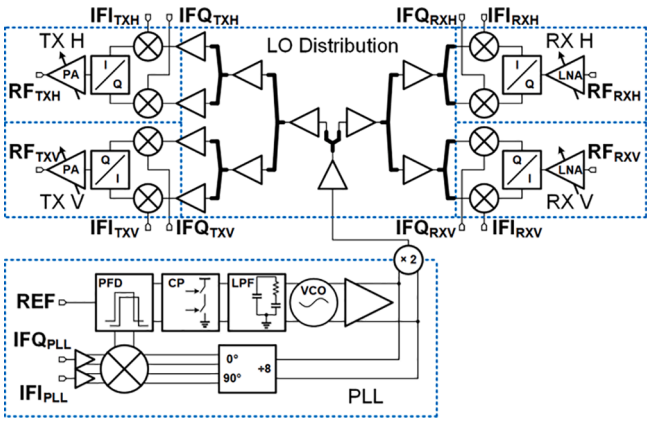


Fig. 3. Block diagram of D-band dual-channel IQ radar sensor transceiver front-end with integrated PLL [14].

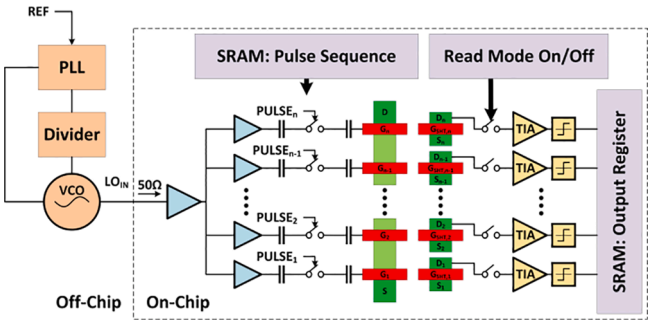


Fig. 4. Block diagram of hole-spin quantum processor with 1D quantum dot qubit array consisting of gates G_1 through G_n monolithically integrated with control and readout electronics on the same chip and operating in the 2 – 4 K temperature range. Capacitively-coupled single-hole transistors (SHTs) detect the number of holes with amplification from a TIA for qubit readout.

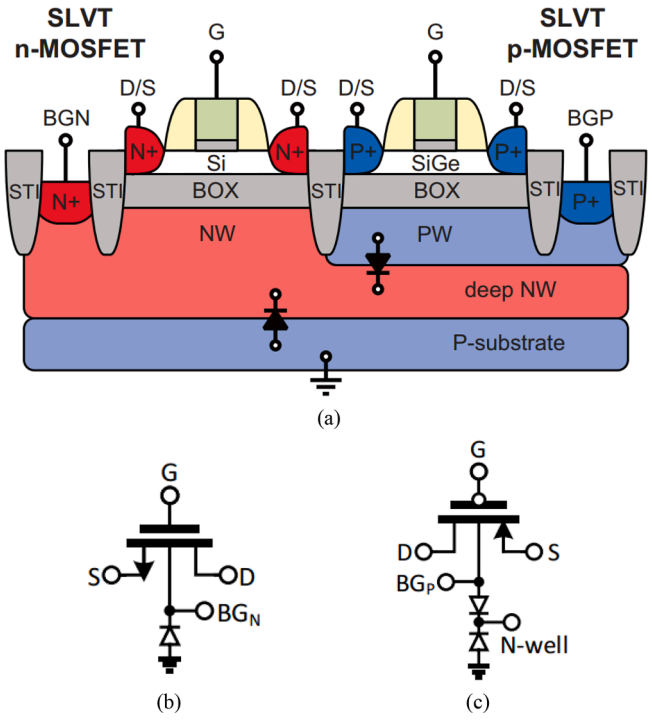


Fig. 5. a) Cross-section diagram of SLVT FDSOI CMOS transistors [22] and schematic representations of the b) *n*-MOSFET and c) *p*-MOSFET transistors showing the backgate wells and deep n-well.

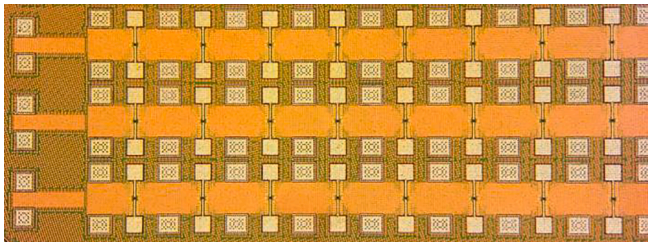


Fig. 6. Zoomed in image of a die microphotograph containing multiple transistor test structures.

structure. The MOSFET gate and drain are metallized up to the top metal in the BEOL and connected to the signal pads through microstrip transmission lines. The MOSFET source is connected to the ground pads and to the Si substrate through an extensive multi-metal mesh with

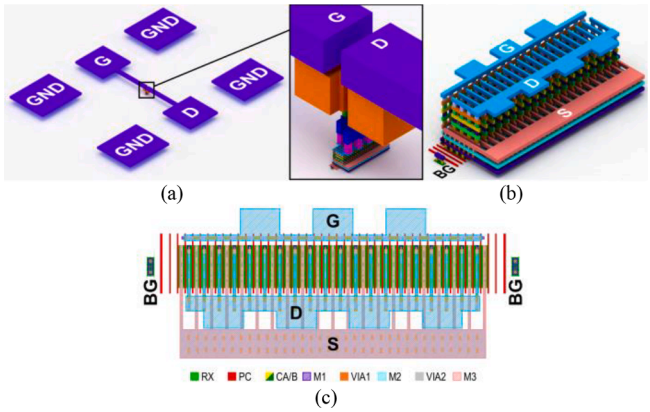


Fig. 7. Fully-wired 40 × 20 nm × 590 nm 1× pitch transistor test structure layout showing a) metallization up to the pads for probing, b) a zoomed-in image of the transistor and just the first 7 metal layers, and c) a top-down view of the transistor layout [22]. Transistor source is connected to GND via extensive metal mesh (not shown).

substrate p-taps to ensure that ground series resistance and inductance, which might degrade the measured figures-of-merit (FoMs), are minimized. The transistor test structures in each row of Fig. 6 share the same back gate pad on the west side to fit a larger number of test structures within the available die area while ensuring the pads have enough clearance to be probed.

The transistors were measured using a Lakeshore CPX-VF probe station with low-temperature option between 2 and 300 K and in a Cascade Summit 11741B probe station between 300 K and 400 K. In both probe stations, the dies rest on a grounded sample holder. In this paper, the MOSFET dimensions are denoted using the convention (N_f)x(L_g)x(W_f) where the total MOSFET width is $W = N_f W_f$. Unless otherwise stated, the MOSFET backgate pad was left floating and unbiased.

2.1. DC performance over temperature

As can be observed from the measured width-normalized I_{DS}-V_{GS} transfer characteristics in saturation (V_{DS} = 0.8 V) depicted in Fig. 8a and the transconductance (g_m) vs. V_{GS} characteristics in Fig. 8b, a linear dependence of the drain current on V_{GS} more aptly describes the behavior of the MOSFET except for a small range between the MOSFET threshold voltage (V_t) and ~ V_t + 0.2 V. In the saturation region, the MOSFET transfer characteristics can be described by.

$$I_{DS} = N_f \frac{W_f}{2L_g} \mu(L_g, W_f) C_{OX,eff} \frac{(V_{GS} - V_t)^2}{1 + \theta(V_{GS} - V_t)} (1 + \lambda V_{DS}) \quad (1)$$

where the channel mobility, μ, is expressed as a function of both L_g and W_f to capture short-channel and finger width dependent strain effects, $C_{OX,eff}$ is the effective oxide capacitance between the gate and the channel, λ captures the channel length modulation effect, and θ captures the combined impact of mobility degradation due to the vertical electric field between the gate and the channel and due to velocity saturation as a result of the drain-to-source electric field [23]. Comparing the saturation regime behavior between 3.3 K, 300 K, and 400 K, the MOSFET threshold voltage and peak g_m both increase with decreasing temperature. Although the g_m vs. V_{GS} curves shift with temperature, Fig. 8c shows that the peak g_m is achieved when the MOSFETs are biased at a width-normalized drain-source current density $J_{pgmsat} = I_{DS}/W = 0.475$ mA/μm irrespective of temperature. Similarly, when biased at V_{DS} = ±50 mV on the edge of the linear triode region, the peak g_m is achieved at a current density of J_{pgmlin} = 45 μA/μm, as illustrated in Fig. 8d.

Although J_{pgmsat} and J_{pgmsat} are independent of temperature, Fig. 9a shows that the peak g_m value does change significantly over the 3.3 to 400 K temperature range. The width-normalized $g'_{m,peak}$ of the *n*-

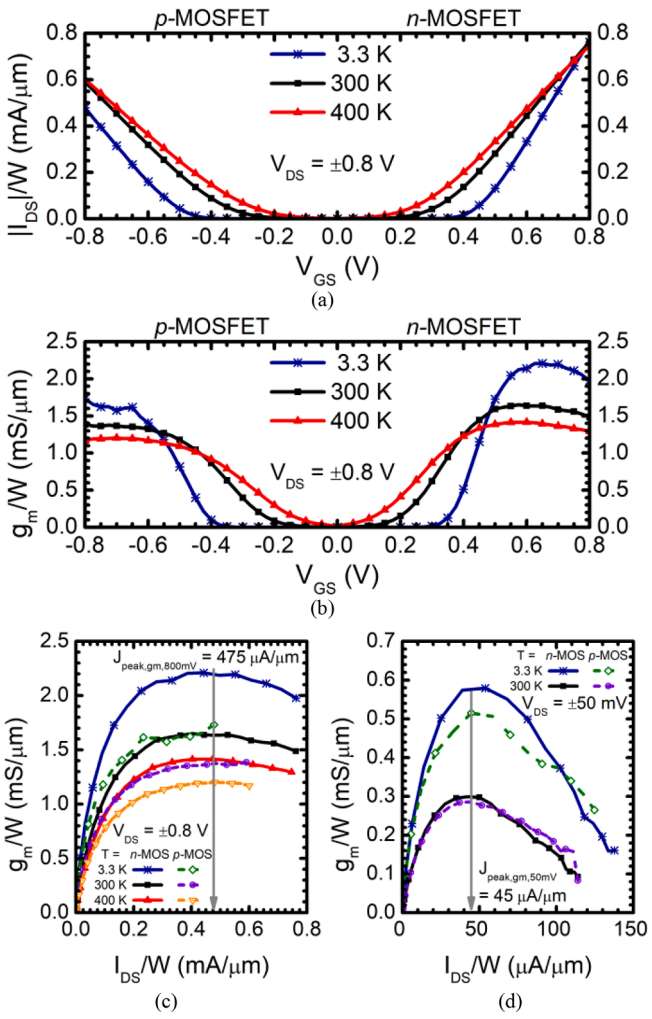


Fig. 8. Measured 40 × 20 nm × 590nm MOSFET a) I_{DS}/W vs. V_{GS} b) g_m/W vs. V_{GS} and c) g_m/W vs. I_{DS}/W at 3.3 K, 300 K, and 400 K at $V_{DS} = \pm 0.8$ V. d) Measured 40 × 20 nm × 590nm MOSFET g_m/W vs. I_{DS}/W at 2 K and 300 K at $V_{DS} = \pm 50$ mV.

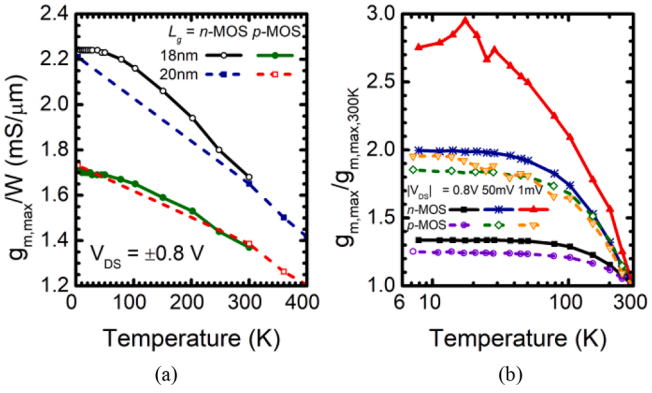


Fig. 9. a) Measured 40 × 18 nm × 590nm and 40 × 20 nm × 590nm MOSFET peak g_m/W vs. temperature from 3.3 K to 400 K at $V_{DS} = \pm 0.8$ V. b) Measured 40 × 18 nm × 590nm MOSFET peak g_m normalized relative to peak g_m at 300 K vs. temperature from 3.3 K to 300 K $V_{DS} = \pm 0.8$ V, ±50 mV, and ± 1 mV.

MOSFET is 1.68 mS/μm at 300 K, degrading to 1.42 mS/μm at 400 K and improving to 2.24 mS/μm at 3.3 K. The *p*-MOSFET $g'_{m,peak}$ is 1.37 mS/μm at 300 K, 1.2 mS/μm at 400 K, and 1.71 mS/μm at 3.3 K. For CMOS circuits where the transconductances of the *n*- MOSFET and *p*-MOSFET must be matched, this indicates that the relative width of the *p*-MOSFET must be approximately 1.31, 1.23, and 1.18 times the width of the *n*-MOSFET at 3.3 K, 300 K, and 400 K, respectively. Fig. 9b shows $g_{m,peak}$ normalized to its room temperature value for the MOSFETs biased at different V_{DS} from 8 K to 300 K. Improvement in $g_{m,peak}$ mostly occurs over the 300 K to 100 K range for $V_{DS} = \pm 0.8$ V and remains practically flat below 70 K. In the triode region, at low V_{DS}, the peak transconductance continues to increase down to 2 K. This suggests that low-field mobility continues to improve below 70 K whereas saturation velocity, which impacts $g_{msat,peak}$ in the saturation region the most, does not change with temperature below 70 K.

An important figure of merit, FoM, for low-power analog circuit design is the g_m/I_{DS} ratio. This is plotted in Fig. 10a vs. bias current density for six temperatures when the MOSFETs are biased in saturation. The *n*-MOSFET is superior to the *p*-MOSFET, but both have improved g_m/I_{DS} as temperature and current density decrease. Fig. 10b depicts the g_m/I_{DS} as a function of temperature at four different bias current densities in the 0.1 mA/μm to 0.4 mA/μm range, relevant for mm-wave, high-speed and fibreoptic circuit design, showing that, as with $g_{m,peak}$, there is little improvement as temperature decreases from 100 K down to 8 K.

Another useful FoM in analog circuit design is the small-signal intrinsic voltage gain of the transistor ($A_V = g_m/g_{ds}$, where g_{ds} is the output conductance of the MOSFET). Fig. 11 shows the measured transconductance and intrinsic voltage gain of the *n*- and *p*-MOSFETs vs. V_{DS}. The degradation in g_m from $V_{DS} = \pm 0.8$ V to $V_{DS} = \pm 0.4$ V is small at all temperatures, which is good for MOSFET amplifier and linear transconductor stages where MOSFETs are biased at $V_{DS} = \pm 0.4$ V. A_V improves from ~ 5 V/V at 400 K to ~ 10 V/V at 3.3 K for both the *n*-MOSFET and *p*-MOSFET at $V_{DS} = \pm 0.4$ V.

2.2. RF performance over temperature

The MOSFET S-parameters were measured in the DC – 40 GHz range (limited by the 3.3 K measurement setup) for devices with the thin metal BEOL option. All transistors have 1× gate pitch and are contacted on only one side of the gate. Fig. 12 compiles the measured f_T and f_{MAX} FoMs of the fully metallized *n*- and *p*-MOSFETs at 3.3 K, 300 K, and 400 K. The parasitics associated with the pads and with the microstrip interconnect lines from the pad to the edge of the transistor (i.e. the top metal of the test structure in Fig. 7a) were de-embedded using the t-line technique described in [24]. However, the capacitive and resistive parasitics of the wiring on top of the transistor were not removed to capture the true performance of the transistor when used in mm-wave or high-speed circuits. It is worth noting that the MOSFET metallization was designed to satisfy the electromigration rules for current densities up to 0.3 mA/μm and temperatures up to 105 °C. For applications at

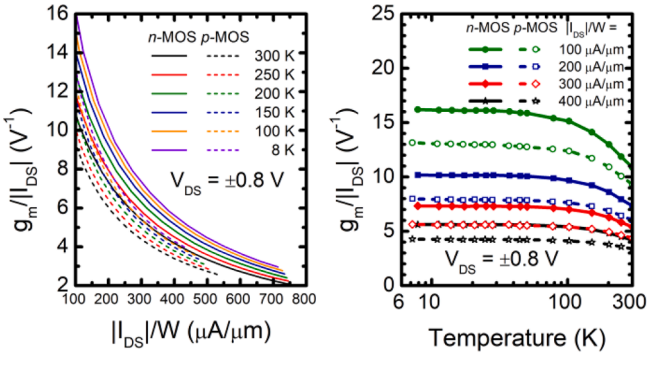


Fig. 10. Measured 40 × 18 nm × 590nm MOSFET g_m/I_{DS} a) vs. I_{DS}/W for the indicated temperatures and b) vs. temperature for the indicated current densities I_{DS}/W at $V_{DS} = \pm 0.8$ V.

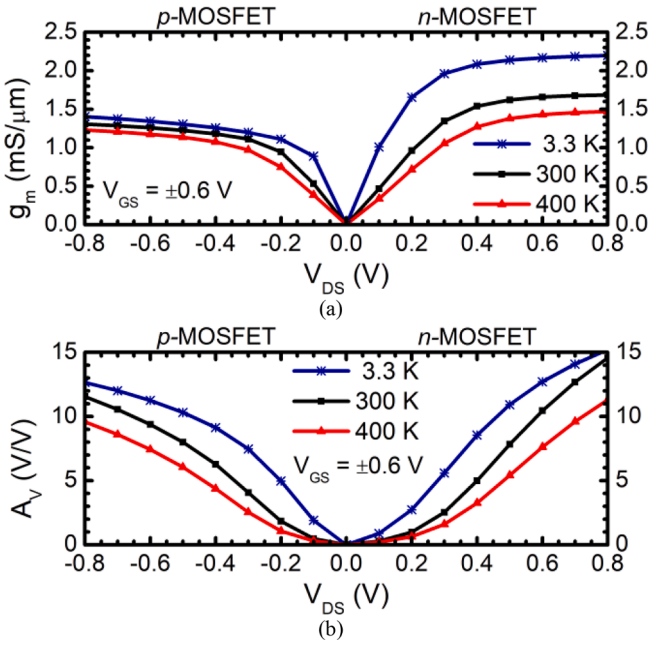


Fig. 11. Measured 40 × 20 nm × 590nm MOSFET a) g_m and b) voltage gain $A_V = g_m/g_{ds}$ vs. V_{DS} at 3.3 K, 300 K, and 400 K at $V_{GS} = \pm 0.6$ V and $V_{DS} = \pm 0.8$ V.

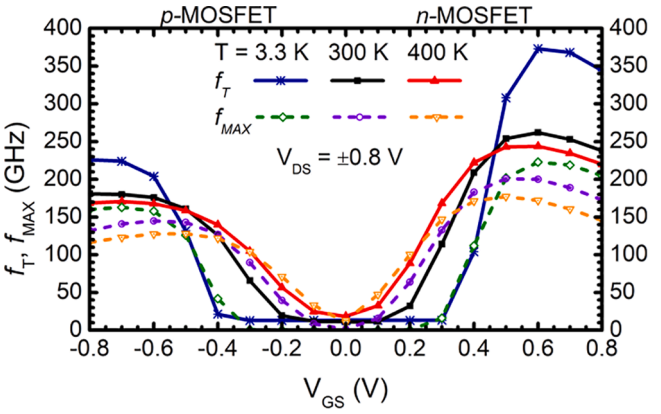


Fig. 12. Measured fully-wired 1× pitch 40 × 20 nm × 590nm MOSFET f_T and f_{MAX} vs. V_{GS} at 3.3 K, 300 K, and 400 K at $V_{DS} = \pm 0.8$ V.

lower temperatures, less metallization is required to pull the current out of the MOSFET and the parasitic metallization capacitance can be reduced. Just like what was observed for transconductance, the measured f_T and f_{MAX} improve at lower temperature but the curves shift to higher $|V_{GS}|$ bias due to the increased threshold voltage as temperature decreases. The *n*-MOSFET peak f_T/f_{MAX} improve from 244/177 GHz at 400 K, to 262/201 GHz at 300 K, to 373/223 GHz at 3.3 K. The *p*-MOSFET peak f_T/f_{MAX} improve from 171/128 GHz at 400 K, to 181/145 GHz at 300 K, to 226/163 GHz at 3.3 K.

Fig. 13a and 13b plot the same f_T and f_{MAX} data against MOSFET current density for the *p*- and *n*-MOSFET, respectively, showing that the peak f_T and peak f_{MAX} bias current densities, J_{pfT} and J_{pfMAX}, are independent of temperature. J_{pfMAX} is 0.3 mA/μm and 0.35 mA/μm for the *p*- and *n*-MOSFET, respectively. The ratio between this *n*-MOSFET and *p*-MOSFET J_{pfMAX} values (1.17) is approximately equal to the ratio of the g'_{mpeak} values of the *n*- and *p*-MOSFETs at 400 K, indicating the devices are subtly optimized to keep f_{MAX} as high as possible in balanced CMOS inverter transconductors and source-follower buffers operating at temperatures higher than 300 K. J_{pfT} is 0.5 mA/μm and 0.45 mA/μm for the *p*- and *n*-MOSFETs, respectively, equal to the J_{pgm} of 0.475 mA/μm

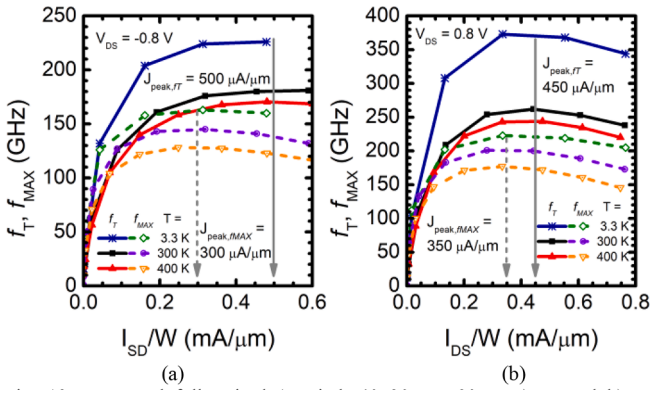


Fig. 13. Measured fully-wired 1× pitch 40 × 20 nm × 590nm a) *p*- and b) *n*-MOSFET f_T, f_{MAX} vs. I_{DS}/W at 3.3 K, 300 K and 400 K, at $V_{DS} = \pm 0.8$ V.

within the measurement precision. Regardless of there being an optimal current density bias for either f_T or f_{MAX}, Fig. 13a and 13b show that the f_T and f_{MAX} vary by very little over a wide range of current densities above 0.1 – 0.15 mA/μm.

The MOSFET parasitic resistances were extracted from the measured Z-parameters when the MOSFET is biased in triode regime ($V_{DS} = 0$ V, $V_{GS} = \pm 0.6$ V) using the methodology and equations in [25]:

$$R_g = Re\{Z_{11} - Z_{12}\} \tag{2}$$

$$R_s = Re\{Z_{12}\} \tag{3}$$

$$R_d = Re\{Z_{22} - Z_{12}\} \tag{4}$$

These resistances should be extracted as an average over the highest range of frequencies where *Z*-parameters are available where (2)–(4) are flat with respect to frequency. Fig. 14 plots the value of R_g and the width-normalized values of R_s and R_d in the 20–40 GHz range at 3.3 K, 300 K, and 400 K. R_g is not width normalized because it increases with W_f and decreases with N_f and is therefore a more complicated function of the MOSFET metallization and chosen finger width. Fig. 14a shows that the gate resistance remains constant with temperature within the measurement uncertainty (estimated as the deviation of the extracted gate resistance value at each frequency compared to the mean value over frequency), while Fig. 14b reveals that, although the source resistance of the *n*-MOSFET does not change at 3.3 K from the 220 Ω·μm value measured at 300 K, it increases slightly to 250 Ω·μm at 400 K. The *p*-MOSFET source resistance increases from 250 Ω·μm at 300 K to 300 Ω·μm at 400 K and to 400 Ω·μm at 3.3 K. The increase in R_s at 400 K in both MOSFET types is attributed to a combination of increased resistance in the metal mesh and in the salicide contact resistance. The increase in the *p*-MOSFET R_s at 3.3 K relative to 300 K is attributed to the SiGe heterojunction between the channel and the source/drain regions

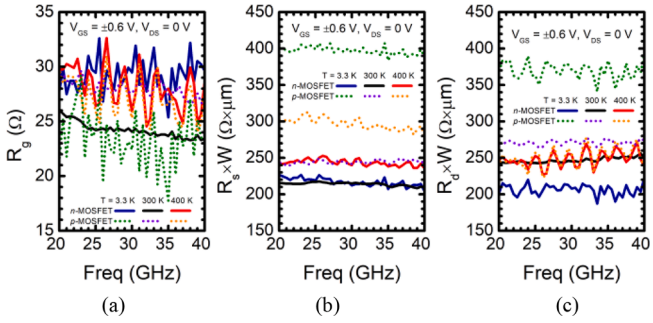


Fig. 14. Measured fully-wired 1× pitch 40 × 20 nm × 590nm MOSFET a) R_g, and width-normalized b) R_s and c) R_d vs. frequency at $V_{GS} = \pm 0.6$ V and $V_{DS} = 0$ V.

[26] which creates a small energy barrier to hole transport with more pronounced effect at lower temperatures. The drain resistance in Fig. 14c is approximately equal to 250 – 260 Ω·μm for both the *p*- and *n*-MOSFETs at both 300 K and 400 K, slightly higher than R_s, suggesting the drain resistance is dominated by the via stack used to connect the MOSFET drain fingers up to the top metal. The *n*-MOSFET shows a reduced 200-Ω·μm R_d at 3.3 K, as is expected from the increased conductivity of the via stack at 3.3 K. The *p*-MOSFET R_d at 3.3 K has the same reduced via resistance, but at 375 Ω·μm R_d is still higher than at room temperature due to the SiGe heterojunction.

Finally, Fig. 15 compares the f_T and f_{MAX} vs. current density measurements for different *n*- and *p*-MOSFETs with different $W_f = 80$ nm, 270 nm, 430 nm, and 590 nm and the same $N_f = 40$ fingers at 3.3 K and 300 K. These finger widths were chosen because they maximize the number of source/drain contacts per μm of finger width, minimizing R_s and R_d. At both temperatures and for both *n*- and *p*-MOSFETs, the $W_f =$ 590 nm device has the highest f_T, and the transistor f_T decreases with decreasing transistor width. Looking at Fig. 15a and c, the optimal W_f to maximize f_{MAX} for the *p*-MOSFET is somewhere between 270 nm and 430 nm, although the peak f_{MAX} for $W_f = 590$ nm is only about 5% smaller. For the *n*-MOSFET in Fig. 15b and d, the optimal W_f to maximize f_{MAX} is between 430 nm and 590 nm. The situation is different for MOSFETs in the thick metal backend with 1×, 2×, and 3× pitch and contacted on both sides of the gate. For the latter devices, the highest f_T and f_{MAX} measured at 300 K, approximately 270 GHz, was obtained for fully wired 40 × 18 nm × 720 nm *n*-MOSFETs with 2× gate pitch and double gate contacts [1]. Regardless of MOSFET finger width, Fig. 15 shows that I_{DS}/W remains the best indicator for ensuring the MOSFET bias is optimized for either peak f_T or peak f_{MAX}.

2.3. Quantum dots in subthreshold region below 50 K

The subthreshold region of nanoscale MOSFETs is particularly interesting at cryogenic temperatures. At low temperature and at low V_{DS}, the subthreshold region of the MOSFET transfer characteristics will exhibit "peaks" and "valleys" indicative of Coulomb Blockade [2,16–18,27,28]. Fig. 16a shows typical Coulomb Blockade behaviour in 1 × 20 nm × 80 nm *p*- and *n*-MOSFET quantum dots, QDs, at 2 K and compares it to room temperature behaviour for the indicated V_{DS} bias. Moving from lower to higher $|V_{GS}|$, the crossing of each peak represents

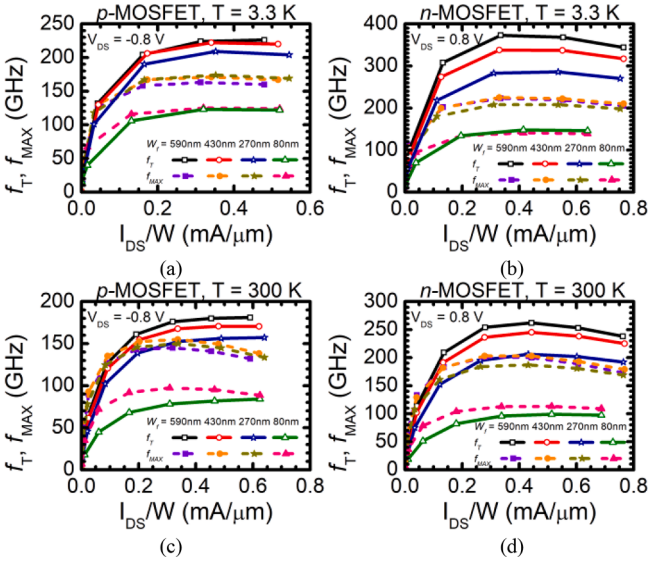


Fig. 15. Measured f_T and f_{MAX} vs. I_{DS}/W at $V_{DS} = \pm 0.8$ V for fully-wired 1× pitch 40 × 20 nm × W_f MOSFETs of different finger width ($W_f = 590$ nm, 430 nm, 270 nm, and 80 nm) for a) *p*-MOSFETs at 3.3 K, b) *n*-MOSFETs at 3.3 K, c) *p*-MOSFETs at 300 K, and d) *n*-MOSFETs at 300 K.

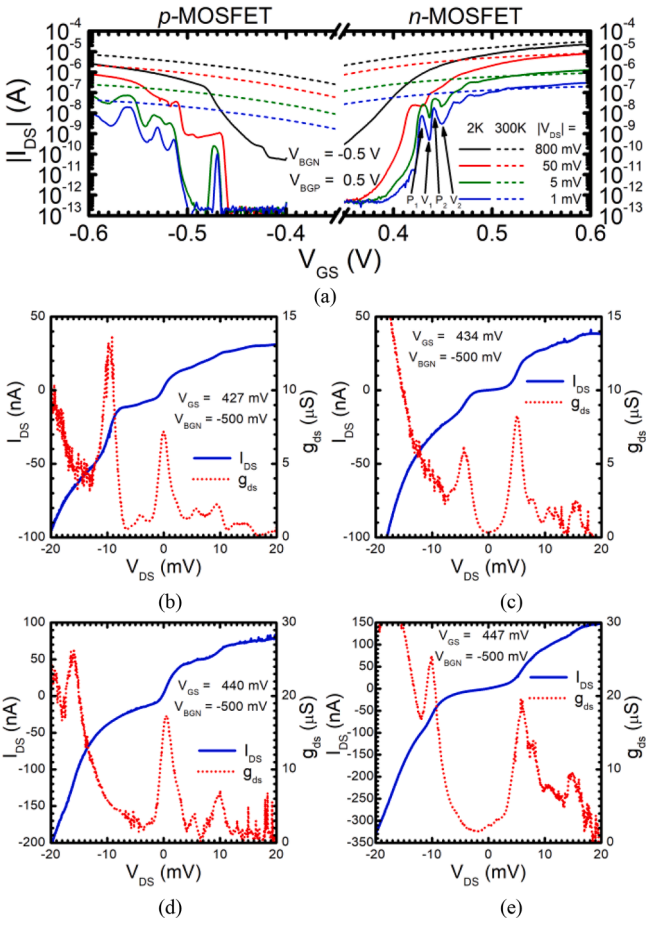


Fig. 16. a) Measured 1 × 20 nm × 80nm MOSFET I_{DS} vs. V_{GS} at 2 K and 300 K at the indicated V_{DS} bias with V_{GS} bias points of interest for SET operation marked for the *n*-MOSFET. Measured I_{DS} and output conductance vs. V_{DS} for the 1 × 20 nm × 80nm *n*-MOSFET when V_{GS} is biased at b) peak 1 (P_1), c) valley 1 (V_1), d) peak 2 (P_2), and e) valley 2 (V_2) of the transfer characteristic.

the addition of a single electron/hole to the QD formed in the conduction/valence band under the MOSFET gate in the *n*-/*p*-MOSFET. The first and second sets of peaks/valleys are marked in Fig. 16a for the *n*-MOSFET transfer characteristic at $V_{DS} = 1$ mV and 2 K. Because the number of electrons/holes occupying the QD can be controlled in single electron/hole increments, the *n*-MOSFET/*p*-MOSFETs biased in this regime are also called single-electron/single-hole transistors (SETs or SHTs). Fig. 16b – 16e show the n-MOSFET output characteristics (I_{DS} vs. V_{DS}) over a small range of V_{DS} centered on $V_{DS} = 0$ V when the *n*-MOSFET is biased at the V_{GS} corresponding to the peaks and valleys in Fig. 16a. The sharp peaks in small signal output conductance ($g_{ds} = \partial I_{DS}/\partial V_{DS}$) also correspond to the change of the number of electrons contained within the SET by 1. The output conductance peaks range between 5 and 20 μS (50–200 kΩ output resistance) for these bias points, being higher for peak/valley 2 relative to peak/valley 1. The larger conductance obtained when biased at peak/valley 2 is preferred because it reduces the time constant at the output of the SET when it drives a readout TIA in a monolithic QPU, improving the readout fidelity for qubits with low charge-state lifetimes.

In FDSOI technology, the electron or hole confinement in the QD formed in the channel of the MOSFET is provided by the large energy barrier at the interface between the channel and the gate-, buried-, and shallow trench isolation oxides in the two directions perpendicular to the channel, and by the weaker energy barriers formed under the gate oxide spacers in the direction of current flow between source and drain. In the case of the *p*-MOSFET, the SiGe heterojunction between the

channel and the source/drain regions further increases the valence band energy barriers under the gate oxide spacers [16]. The impact of this higher energy barrier in the *p*-MOSFET in reducing current is readily apparent in Fig. 16a, where the first few current peaks are 101 pA, 265 pA, and 1.1nA compared to the values of the first current peaks in the *n*-MOSFET of 8.2 and 20nA.

Two conditions must be satisfied to observe Coulomb Blockade when the *n*th electron/hole is added to a QD: i) the energy required add the *n*th electron/hole must be larger than the ambient thermal energy (k_BT where k_B is Boltzmann's constant) and ii) the source and drain access resistances must be larger than $h/q^2 = 25.8$ kΩ (where h is Planck's constant and q is the electron charge) [29]. The measurements in Fig. 17a show that Coulomb Blockade behaviour is maintained in the 1 × 18 nm × 70 nm *p*-MOSFET up to 50 K, which implies that the first condition can be satisfied in this technology up to at least 50 K. The consequence of the second condition is that the small-signal output conductance of MOSFETs behaving as SETs or SHTs cannot exceed ~ 78 μS (i.e. two 25.8-kΩ resistors in series), in good agreement with the observed g_{ds} in Fig. 16b–e. While outside the scope of this work, it is worth noting that Fig. 17a and b demonstrate that the Coulomb Blockade behavior of the *p*- and *n*-MOSFETs can be simulated by using a subcircuit with the foundry design kit MOSFET model connected in parallel with a custom-developed Verilog-A model of the QD whose parameters were extracted from QD measurements over temperature [27]. This compact model reproduces the full measured QD stability diagram (I_{DS} vs. V_{GS} and V_{DS}) for the 1 × 18 nm × 70 nm *p*-MOSFET (Fig. 18).

The subthreshold behavior of minimum gate length MOSFETs with larger finger width and number of gate fingers is shown in Fig. 19a for different V_{DS} at 8 K and 300 K. The Coulomb Blockade behavior is less pronounced in devices with larger finger width, although it is not fully suppressed. It can be observed that even for $|V_{DS}| \geq 50$ mV, there are still signatures of quantum effects in the form of "plateaus" in the 8 K transfer characteristics. These plateaus are the result of electron/hole energy quantization in the two directions perpendicular to the drain-source current flow and cannot be suppressed by a choice of bias at low temperature.

The presence of the Coulomb Blockade effects makes the subthreshold swing (SS) difficult to define. It will be different depending on which range of V_{GS} values it is extracted from [3]. The SS vs. temperature characteristics shown in Fig. 19b were obtained from the range of V_{GS} values where the drain current is 1–3 orders of magnitude above the measurement noise floor and below the first Coulomb current peak. The V_{GS} regions used at 8 K and 300 K are indicated by circles in Fig. 19a. The measured *p*- and *n*-MOSFET subthreshold swing follows closely the expected linear dependence on temperature down to 10 K, although the more accurate models proposed in [30] and [31] would certainly fit

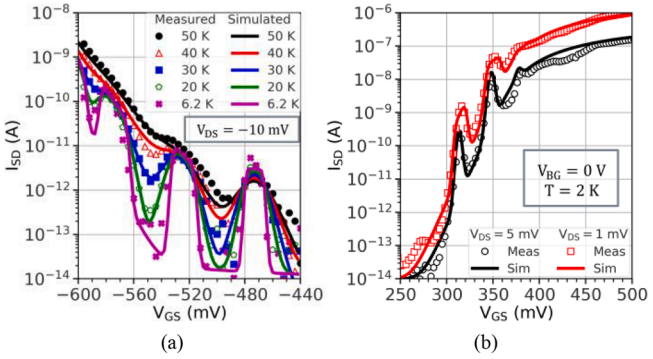


Fig. 17. Measured (symbols) and simulated (lines) 1 × 18 nm × 70nm I_{DS} vs. V_{GS} of a) *p*-MOSFET at different temperatures and b) *n*-MOSFET at different V_{DS} biases at 2 K. The I–V characteristics are modelled by a Verilog-A compact model added in parallel with the foundry MOSFET model [27].

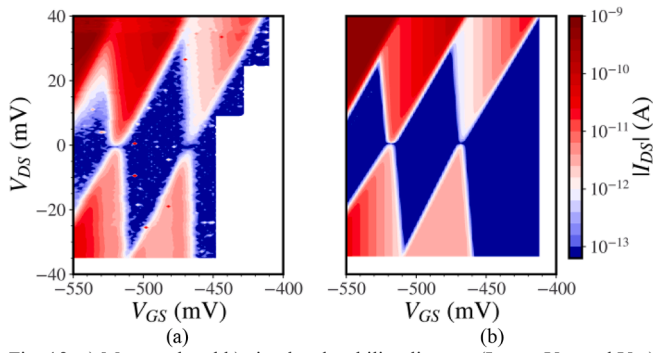


Fig. 18. a) Measured and b) simulated stability diagram (I_{DS} vs. V_{GS} and V_{DS}) of the same 1 × 18 nm × 70nm *p*-MOSFET of Fig. 17 at 6.2 K in the few-hole regime [27].

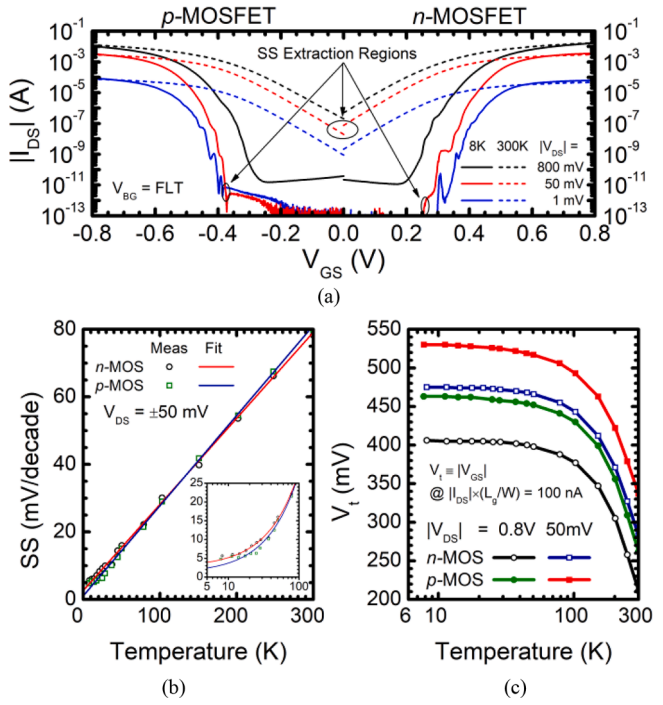


Fig. 19. a) Measured 40 × 18 nm × 590nm MOSFET I_{DS} vs. V_{GS} at 8 K and 300 K and V_{DS} = ±0.8 V, ±50 mV, and ± 1 mV with the regions at which subthreshold swing is extracted marked. Measured b) subthreshold swing and c) threshold voltage from 8 K to 300 K at the indicated V_{DS} bias. Inset of b) zooms in on the low temperature data points, showing a linear fit to subthreshold swing extracted at the deepest part of subthreshold is reasonable down to ~ 10 K.

better. The linear dependence on temperature suggests that Fermi-Dirac statistics are still a reasonable approximation over this temperature range. V_t, defined as the V_{GS} value at which $I_{DS} = 100\text{nA} \times W/L_g$ at a given V_{DS}, is plotted in Fig. 19c for these MOSFETs from 8 K to 300 K. Most of the change in threshold voltage by this definition occurs in the 300 K to 100 K range and saturates by 10 K, identically to the g_m-based FoMs discussed previously. Between 300 K and 8 K, the difference in *n*-MOSFET threshold voltage is 195 mV at $V_{DS} = 0.8$ V and 192 mV at $V_{DS} = 50$ mV. For the *p*-MOSFET, the threshold voltage change over temperature is 201 mV at $V_{DS} = -0.8$ V and 193 mV at $V_{DS} = -50$ mV. The change in V_t from 300 K to 10 K reported here is consistent with that measured down to 2.95 K by another group for short-channel MOSFETs fabricated in the same technology [5].

2.4. Back gate voltage optimization to compensate the impact of temperature variation

Unlike bulk planar or FinFET CMOS technologies, in FDSOI the threshold voltage and bias current density of a transistor can be adjusted from the back gate voltage, without having to change the supply voltage or drain-source voltage to compensate for the threshold voltage variation with temperature. Fig. 20a shows the width-normalized transfer characteristics of *n*- and *p*-MOSFETs for the full range of safe back gate voltages at 10 K and 300 K at $V_{DS} = \pm 0.8$ V. The corresponding g_m/W vs. V_{GS} curves are plotted in Fig. 20b. As the back gate voltage increases/decreases in the *n*-/*p*-MOSFET, the V_t decreases/increases. Back gate voltage values, V_{BG}, which reduce V_t relative to its nominal value at $V_{BG} = 0$ V are referred to as forward body-biased while back gate voltage values which increase V_t are referred to as reverse body-biased. Fig. 21a plots the MOSFET V_t (using the $V_t = V_{GS}$ @ $I_{DS} = 100\text{nA} \times W/L_g$ definition) vs. back gate voltage, showing that the back gate voltage dependence of V_t is an approximately linear function at both 10 K and 300 K with a slope of approximately 80 mV/V for the *p*-MOSFET and 95 mV/V for the *n*-MOSFET independent of temperature. The temperature invariance of dV_t/dV_{BG} in FDSOI CMOS was also reported in [4] and [5] for another FDSOI technology.

A unique feature of FDSOI technology is also that J_{pgm} increases with increasing forward body bias. This is very important in linear, large-swing optical modulator driver and linear power amplifier design. In the *n*-MOSFET, J_{pgm} can be tuned from 0.475 mA/μm at $V_{BG} = -0.5$ V to over 1 mA/μm at $V_{BG} = 4$ V. In the *p*-MOSFET, J_{pgm} increases up to 0.8 mA/μm at $V_{BG} = -4$ V. The larger J_{pgm}, the larger the output power and the larger the linear current swing that can be accommodated by the driver/PA stage with minimum distortion. By biasing the *n*-MOSFET at J_{pgm}, its g_m changes by less than 10% for current density swings from 0.3 to 0.8 mA/μm. By comparing Fig. 22a, b, it can be noticed that the *n*-MOSFET exhibits a larger peak-g_m variation with V_{BG} than the *p*-MOSFET at the same temperature.

The main application of the back gate voltage in circuit design is to control V_t and through it many other transistor parameters such as bias current, peak g_m, peak f_T, peak f_{MAX}, voltage, and power gain. An important scenario is the use of V_{BG} to compensate for V_t variation over temperature while holding the MOSFET, I_{DS}, V_{GS} and V_{DS} constant for maximum linearity and to maintain constant power consumption. The suitable V_{BG} for a given circuit bias scenario can be first determined at 300 K using either simulation or room temperature measurements and then a back gate voltage correction can be found from Fig. 23 to

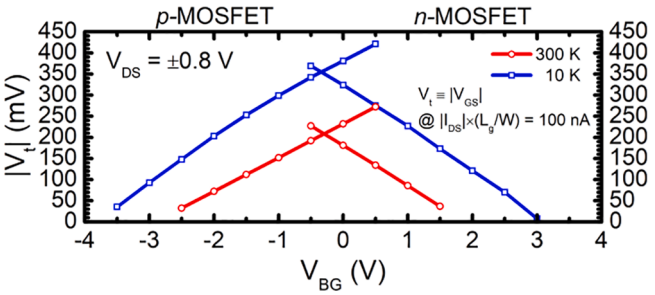


Fig. 21. Measured 40 × 18 nm × 590 nm MOSFET V_t vs. V_{BG} at 10 K and 300 K and $V_{DS} = \pm 0.8$ V.

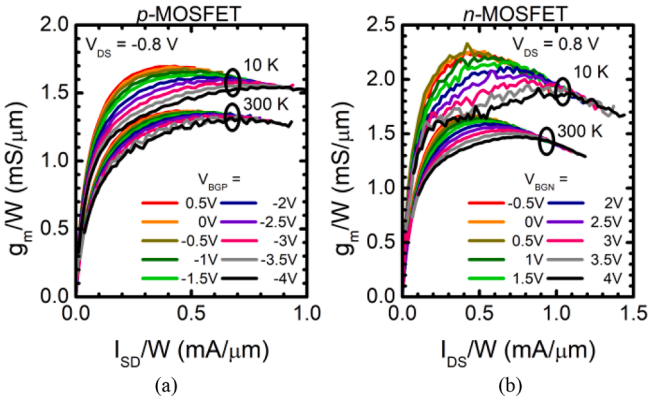


Fig. 22. Measured 40 × 18 nm × 590nm a) *p*-MOSFET and b) *n*-MOSFET g_m/W vs. I_{DS}/W vs. V_{BG} at 10 K and 300 K at $V_{DS} = \pm 0.8$ V.

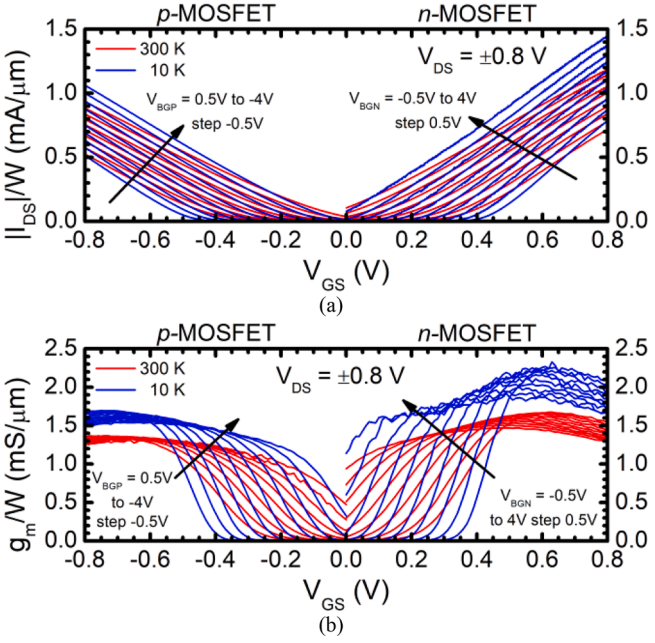


Fig. 20. Measured 40 × 18 nm × 590nm MOSFET a) I_{DS}/W vs. V_{GS} and b) g_m/W vs. V_{GS} at 10 K and 300 K and $V_{DS} = \pm 0.8$ V for backgate voltages $V_{BG(P/N)} = \mp 0.5$ V to ± 4 V with 0.5 V steps.

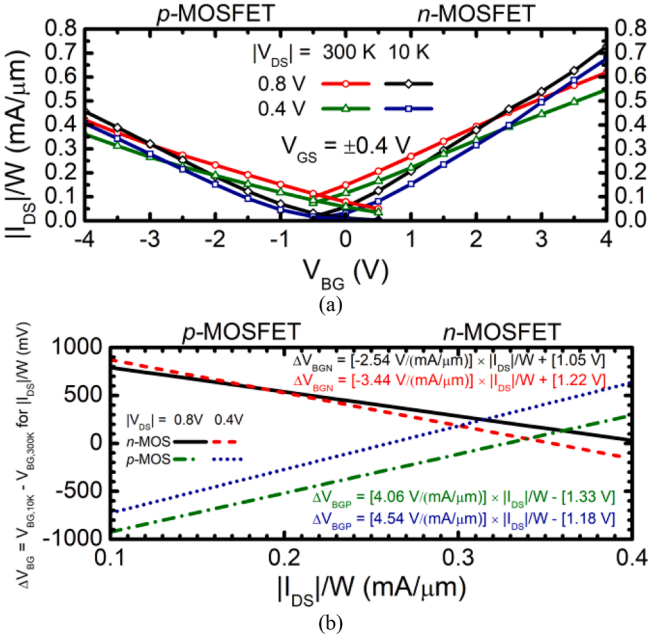


Fig. 23. Measured 40 × 18nm × 590 nm MOSFET a) I_{DS}/W vs. V_{BG} and b) required change in V_{BG} bias at 10 K relative to 300 K to maintain the same current density at $V_{GS} = \pm 0.4$ V and $V_{DS} =$ $= \pm 0.4$ V and $\pm$ 0.8 V.

maintain the same bias current density at cryogenic temperature. For example, this method can be applied to determine the back gate bias correction required for CMOS inverters in TIAs and source follower (SF) input buffers in high-speed ADCs operating below 50 K (where g_m and V_t are almost constant across temperature for $V_{DS} = 0.4$ V to 0.8 V) when $V_{GS} = \pm 0.4$ V (i.e. half of the nominal supply voltage of V_{DD} of 0.8 V) to maximize the input and output linear voltage swing range. Fig. 23a plots the I_{DS}/W vs. V_{BG} characteristics (i.e. back gate transfer characteristics) for the same 40 × 18 nm × 590nm *p*- and *n*-MOSFETs whose transfer characteristics were plotted in Fig. 20 at 10 K and 300 K and for V_{DS} values of ± 0.4 V and ± 0.8 V. The back gate transfer characteristics are linear for current densities larger than 0.1 mA/μm. Therefore, a linear fit can be applied to obtain the V_{BG} required to bias these devices at a particular current density at the desired V_{DS} at 10 K and 300 K. The I_{DS}-V_{BG} normalized transfer characteristics can be approximated by.

$$|I_{DS}/W| = \left(g'_{m,bg}\right)V_{BG} + I_{DS,0V}/W \tag{5}$$

where the fitting parameters $g'_{m,bg}$, the back-gate transconductance per gate width, and $I_{DS,0V}/W$ are listed in Table 1 for the *p*- and *n*-MOSFET at the four relevant V_{DS} values and temperature combinations. Equation (5) can now be applied for both *n*- and *p*-MOSFETs to obtain the V_{BG} at 10 K which will maintain the same current density, V_{GS}, and V_{DS} as at 300 K:

$$V_{BG,10K} - V_{BG,300K} = \frac{\left(I_{DS} - I_{DS,0V,10K}\right)}{g_{m,bg,10K}} - \frac{\left(I_{DS} - I_{DS,0V,300K}\right)}{g_{m,bg,300K}} \tag{6}$$

where either the width-normalized or absolute values for the drain-source current and back-gate transconductance can be used because the width self-cancels in the equation. The V_{BG} correction between 10 K and 300 K is plotted in Fig. 23b for the *n*- and *p*-MOSFET using the parameter values in Table 1. Interestingly, little to no V_{BG} correction is required for the *n*-MOSFET when biased near 0.35 mA/μm with $V_{DS} =$ 0.4 V or for the *p*-MOSFET when biased near 0.26 mA/μm with $V_{DS} =$ −0.4 V. Considering i) that these current densities are very close to the J_{pfMAX} of the *n*- and *p*-MOSFETs and ii) that the ratio between the *n*-MOSFET and *p*-MOSFET zero back-gate correction $J_{pfMAX,nmos}/J_{pfMAX,pmos}$ (0.35 mA/μm:0.26 mA/μm = 1.35) is very close to g_{mn}/g_{mp} at $V_{DS} =$ ±0.4 V and 10 K (1.86 mS/μm:1.46 mS/μm = 1.27), CMOS inverters with $Wp = 1.35xW_n$ and biased at *n*-MOSFET J_{pfMAX} of 0.35 mA/μm do not need any back gate voltage correction from 300 K to 10 K while being biased at the maximum possible f_{MAX}. Although the analysis for back gate voltage correction was performed using measurements at 10 K, it is valid for all temperatures between 2 K and 50 K because both V_t and g_m remain practically constant below 50 K at large $|V_{DS}|$ (>= 400 mV) in the saturation region.

3. Optimal circuit topologies and design techniques in fdsoi cmos technology

This section describes several improved circuit topologies and design techniques that take advantage of features unique to FDSOI CMOS to achieve state-of-the-art performance in a variety of digital, analog-mixed-signal, and mm-wave circuits for applications in fibreoptic systems, mm-wave radar and radio, and in quantum computing.

Table 1
Backgate transfer characteristics linear fit parameters*.

P/N	V_{DS} (V)	Temperature (K)	$g'_{m,bg}$ (μS/μm)	$I_{DS,0V}/W$ (μA/μm)
P	−0.8	10	−134	−82
		300	−87	63
	−0.4	10	−126	−99
		300	−80	32
N	0.8	10	170	38
		300	119	151
	0.4	10	175	−29
		300	109	115

*Values measured for 40 × 18 nm × 590nm *p*- and *n*-MOSFETs in Fig. 23a.

3.1. Balanced CMOS inverters with constant current density bias in the 2-to-400 K range

In the absence of measurements or design kit models valid at cryogenic temperatures, it is still possible to ensure that all *p*-MOSFETs and *n*-MOSFETs in all CMOS logic and analog circuits on an integrated circuit are well matched at all temperatures from 2 K to 400 K when biased at any current density between 0.1 and 0.4 mA/μm. To that end, a constant-current–density-to-back-gate-voltage conversion circuit is proposed in Fig. 24 [32]. M_1 and M_2 have the same gate length, gate finger width, and number of gate fingers. The total gate width of the *p*-MOSFET M_3 is chosen such that $g_{m3} = g_{m1}$, with $|V_{GSn,p}| = |V_{DSn,p}| = V_{DD}/2$ at the desired temperature of operation. The role of the two resistors is to ensure current limitation and ESD protection. The following step-by-step algorithm is applied to obtain the appropriate *n*-MOSFET and *p*-MOSFET back gate voltages in the ± 4 V range for a given current density and temperature. (i) A DC bias current, I_{BIAS}, is applied to the I_{BIAS} node such that the desired bias current density value I_{BIAS}/W_n is selected at the intended operating temperature of the circuit. (ii) V_{nback} is adjusted and recorded when V_{outn} becomes equal to $V_{DD}/2$. The V_{nback} voltage thus obtained is distributed and applied to all *n*-MOSFETs in the IC, for example the quantum processor in Fig. 4. (iii) With the bias current and V_{nback} set from steps (i) and (ii), V_{pback} is adjusted until V_{pout}

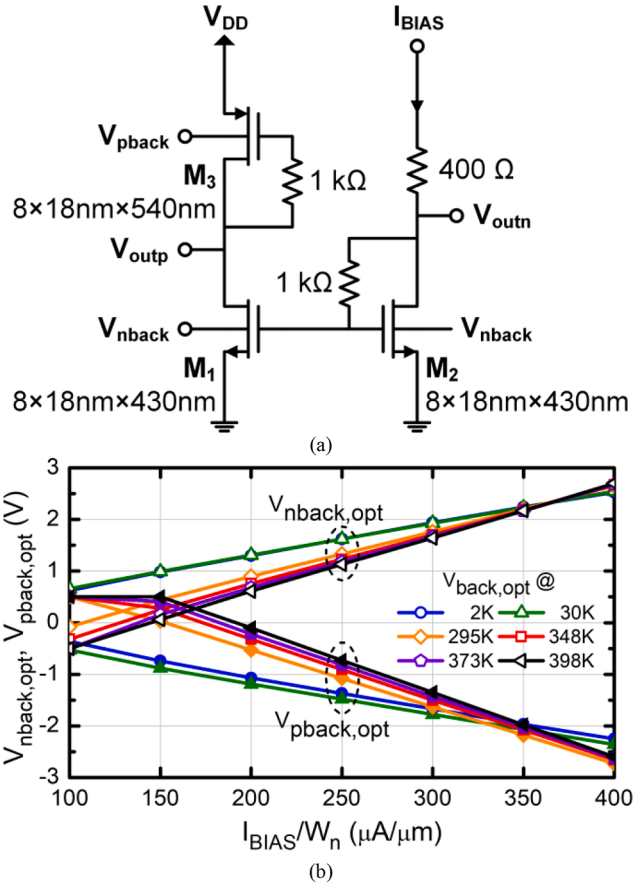


Fig. 24. a) Schematic of circuit used to determine back gate voltages required to optimally bias CMOS amplifiers/buffers at desired constant current density over temperature. b) Measured backgate voltages required for the target *n*-MOSFET current density at different temperatures in the 2 K to ~ 400 K range.

$= V_{DD}/2$. The V_{pback} value thus obtained is distributed and applied to all *p*-MOSFETs in the IC. It is important to note that the *n*-MOSFET and *p*-MOSFET in the conversion circuit must have the same gate length and finger width as all the *n*- and *p*-MOSFETs in the IC. The MOSFETs in the IC may only be different in the number of gate fingers to avoid mismatches due to gate-length and finger-width dependent mobility. Therefore, on a large IC, separate bias circuits must be used for circuit blocks with different gate lengths and finger widths.

The measured optimal V_{nback} and V_{pback} for different ambient temperatures in the 2 K to 400 K range are plotted vs. the target *n*-MOSFET bias current density in Fig. 24b. Because in the most compact layouts the *p*-MOSFET and *n*-MOSFET are formed in the same deep n-well, to avoid turning on the p-well to deep n-well diode, the following condition must hold:

$$V_{pback} - V_{nback} \leq 0.6V \tag{7}$$

As can be seen from Fig. 24b, (7) is more difficult to satisfy at higher temperatures for the lower bias current densities since the MOSFET V_t decreases.

3.2. CMOS inverter performance optimization with V_{BG}

Since the introduction of strain engineering in the *p*-MOSFET at the 90-nm node [33], semiconductor foundries have attempted to provide *p*-MOSFETs with improved performance to better match that of the *n*-MOSFET thus minimizing the area and maximizing the switching speed of the CMOS inverter and CMOS logic, in general. Any mismatch between the two complementary transistors is compensated by choosing the W_p/W_n ratio to match the inverse of their I_{ON} or mobility ratios. However, even with this approach, the matching between the *n*- and *p*-channel devices in bulk planar or FinFET CMOS is only good over a limited range of temperatures and supply voltage. In FDSOI CMOS, the constant-current–density-to-back-gate-voltage conversion circuit ensures that CMOS inverters remain balanced over a wide range of useful current densities at the desired temperature of operation.

The first application of this technique is in current-starved CMOS inverter delay cells whose conventional schematic is depicted in Fig. 25a while that of the simpler FDSOI equivalent is shown in Fig. 25b. In the traditional current-starved CMOS inverter, the resistances of M_{N2} and M_{P2} are tuned from $V_{N,Gate}$ and $V_{P,Gate}$, respectively, to adjust the inverter delay. The downside to this topology is that even when M_{N2} and M_{P2} are turned on fully, the delay of the inverter is still larger than that of a standard CMOS inverter due to the added parasitic resistances. The FDSOI version overcomes this issue by tuning the delay from the back gate voltage without adding transistors in the signal path while maintaining perfect balance between the *n*- and *p*-MOSFETs.

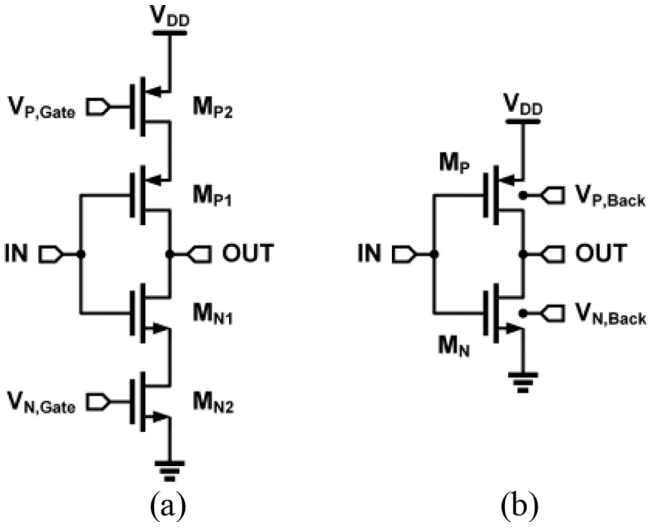


Fig. 25. Schematic of a) current-starved CMOS inverter in technology without backgate voltage terminal and b) current-starved CMOS inverter with backgate voltage.

Fig. 26a through c illustrate how the simulated CMOS inverter voltage gain, delay, and unity gain frequency can be optimized as a function of the *n*-MOSFET current density. The voltage gain (Fig. 26a) is highest at the most reverse body-biased backgate (corresponding to the lowest current density), decreasing from 20.5 dB at $V_{N,BACK} = -0.5$ V a to 12.5 dB at $V_{N,BACK} = 4$ V. The tuneable delay (Fig. 26b) is simulated for a rail-to-rail input and is slew-rate limited. The minimum inverter delay is 4 ps and 6 ps for fanouts of 1 and 2, respectively, and is achieved at the highest current density bias. It and can be increased by 1.5 ps in both cases. The unity gain frequency (Fig. 26c) is defined in this case as the maximum frequency at which the inverter can operate with rail-to-rail voltage swing. The simulated unity gain frequency has a maximum value of 84.5 GHz for a fanout of 1 in agreement with the measurements reported in [1] where a CMOS inverter chain with a fanout of 1 was used at the output of a 80-GHz VCO to drive the 50-Ω off-chip loads with 0.8-V_{pp} swing. The optimal V_{BG} for peak unity gain corresponds to a *n*-MOSFET drain current density of 0.3–0.35 mA/μm, which corresponds to its measured J_{pfMAX} and to that of the *p*-MOSFET sized for Wp/Wn = 540 nm/430 nm, as confirmed in Fig. 26d.

An example application of the tuneable CMOS inverter delay cell is in the 8-phase clock generation block (Fig. 27) of the SAR ADC shown in Fig. 2c, where it is used to align the comparator clock with the outputs of the 8-phase clock generator driving the latches in the SAR. In measurements, the back-gate tuneable CMOS inverter delay cell operates at up to 40 GHz. Fig. 28 shows the simulated rising edge of the clock signal for different $V_{N,Back}$ values. Over 5 ps of delay adjustment is possible at the nominal 32-GHz clock signal when the adjustable delay cell drives the input of the clock generation block. The 5 ps of delay adjustment is roughly twice the 2.25 ps of delay adjustment simulated in Fig. 26b for a fanout of 2 due to the current-starved CMOS inverter being placed before an $N = 2$ frequency divider.

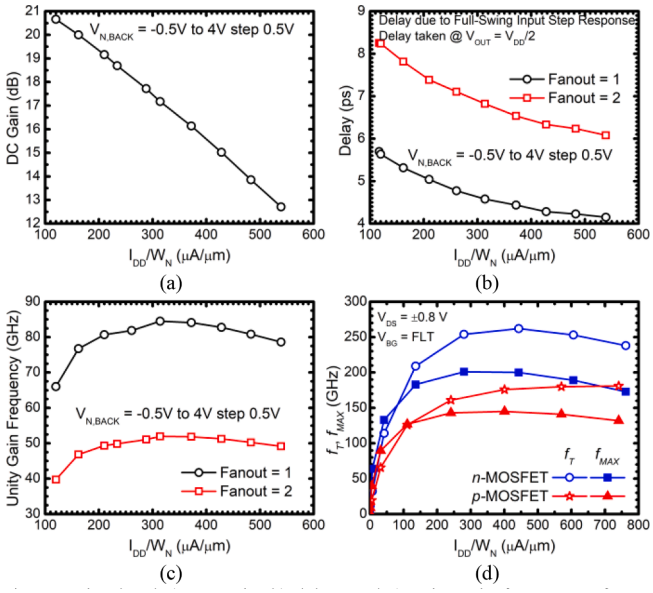


Fig. 26. Simulated a) DC gain, b) delay, and c) unity gain frequency of a 16 finger, width and backgate biased CMOS inverter with layout parasitics extracted vs. *n*-MOSFET current density bias (achieved via different backgate voltage biases) at 65 °C junction temperature and different fanouts. d) Measured *n*- and *p*-MOSFET f_T and f_{MAX} vs. *n*-MOSFET current density at room temperature for 1× pitch, single gate contact 40×20 nm × 590nm MOSFETs (*p*-MOSFET current density corrected by the 540 nm:430 nm finger width ratio used in the CMOS inverter).

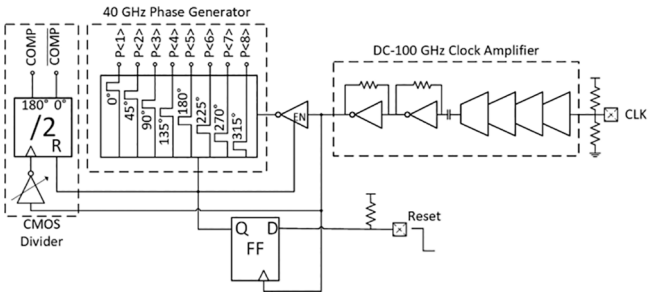


Fig. 27. Clock generation block used to time the comparator and SAR logic [10].

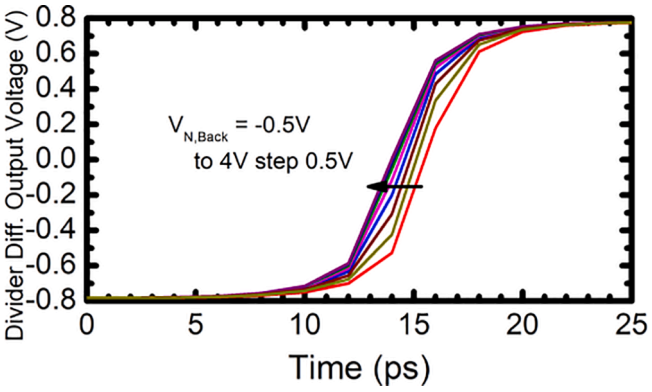


Fig. 28. Simulated delay cell differential output voltage for different current-starved inverter *n*-MOSFET back gate voltages, zoomed in on the rising edge.

3.3. Comparators with tunable decision time

The back gate control of the current density can also be used to minimize the decision time of the latched comparator in the 40-GHz bandwidth SAR ADC of Fig. 2c [10]. The comparator schematic, consisting of a clocked preamplifier followed by an un-clocked latch [34], is shown in Fig. 29. The comparator latch pulls a constant current from V_{DD} which can be tuned between 0.1 and 0.4 mA/μm using the *n*- and *p*-MOSFET back gate voltages. For a given capacitive load due to the resettable flip- flops in the successive approximation register (SAR), this allows the designer to trade-off latch power consumption with decision time. Fig. 30 shows the simulated comparator decision time for a comparator input voltage of LSB/2 = 2 mV_{ppd} as a function of the latch *n*-MOSFET back gate voltage. The decision time decreases from 25 to 20 ps when V_{BG} changes from −0.5 to + 4 V.

3.4. Optimal biasing and design of Linear, high bandwidth buffers

The back gate voltage can also be used to simultaneously maximize the linearity and bandwidth of high-speed ADC input buffers based on

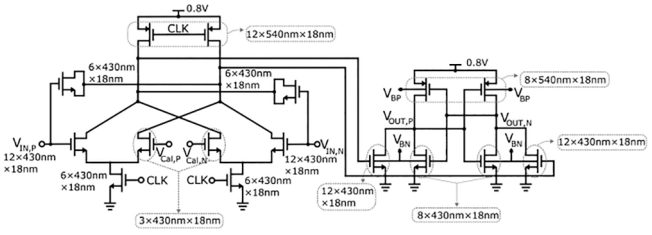


Fig. 29. Schematic of double-tail comparator with un-clocked latch, Miller neutralization differential pair, and second differential pair for offset calibration used in the sub-ADC of Fig. 2c [10].

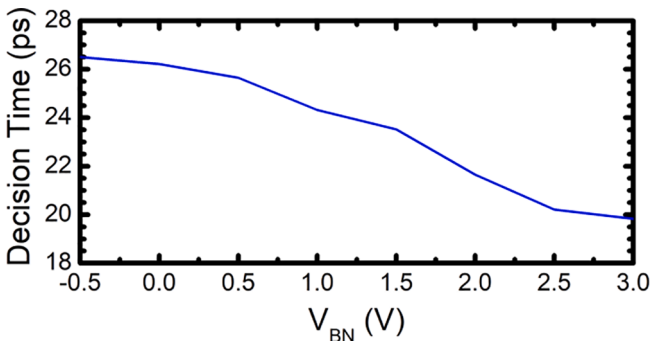


Fig. 30. Simulated comparator decision time vs. latch *n*-MOSFET backgate voltage for 2mVpp input voltage (approximately half an LSB for a 7-bit SAR ADC with 500 mVpp full-scale input voltage).

the source follower, CML Cherry-Hooper [9], CMOS-inverter Cherry-Hooper [35], g_m/g_m, and class AB CMOS source follower [36] topologies while maintaining their DC input and output voltages constant and equal to $V_{DD}/2$. In these circuits, the *n*-MOSFET and the *p*-MOSFET must be biased at J_{pfT} which would be otherwise difficult if not impossible for a supply voltage, V_{DD}, of 0.8 V or less without the back gate terminal or without ultra-low V_t (less than 0.2 V) transistors. This technique was applied in the design of *p*-MOSFET and *n*-MOSFET versions of the CML Cherry-Hooper buffer whose schematics are shown in Fig. 31. These circuits were used as the first and second level buffers, respectively, in the ADC front-end depicted in Fig. 2b. The Cherry-Hooper amplifier topology offers several distinct advantages over traditional source-follower buffers: (i) very high 3-dB bandwidth even when loaded by a large capacitor and long interconnect, facilitating sampled signal distribution over long distances across the chip, (ii) the low output impedance of the CMOS TIA at the output of the amplifier mitigates cross-talk between time-interleaved samplers (relevant in the highest bandwidth time-interleaved ADC needed in fibreoptic receivers), and (iii) eliminates the need for shunt peaking inductors leading to a small layout footprint which further improves bandwidth. Additionally, in FDSOI, gain mismatch control can be implemented by changing the back gate voltage. A DC voltage drop of 0.4 V was selected for the load resistors of the input differential pair to optimally bias the following CMOS inverter TIA stage for the maximum linear output voltage swing. In the case of the *p*-MOSFET CML Cherry-Hooper buffer in Fig. 31a used as the

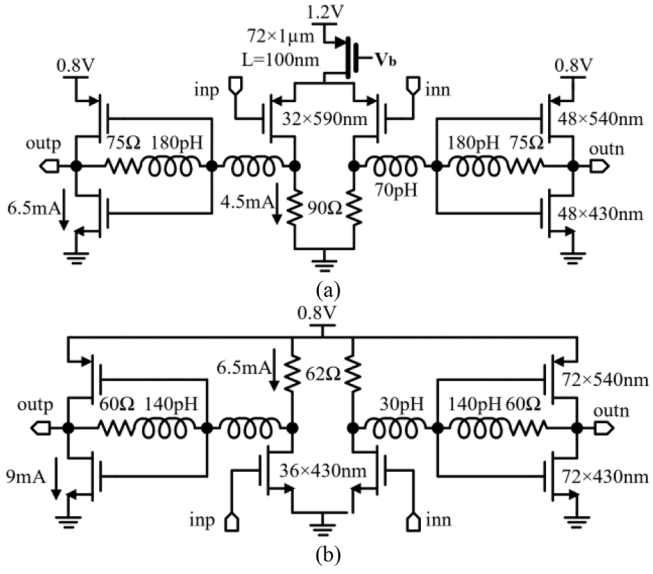


Fig. 31. Schematics of the a) *p*-MOSFET and b) *n*-MOSFET CML Cherry-Hooper stages used in the ADC front-end in Fig. 2b.

first level input buffer, the *p*-MOSFET differential pair with resistive loads is biased at ~ 0.24 mA/μm for peak gain and minimum noise figure and utilizes a 1.2-V supply to allow for a current tail to improve supply and common-mode rejection. Since the CML *n*-MOSFET Cherry-Hooper amplifier in Fig. 31b is placed after the first buffer, it determines the linearity of the ADC front-end. Therefore, the *n*-MOSFETs in the differential pair are biased at ~ 0.42 mA/μm for improved linearity.

As illustrated in Fig. 2b, to facilitate testing of the interleaver bandwidth to the output of the first level switches and to the output of the second level switches from S-parameter measurements, a 50-Ω output buffer was added to one of the first level sampler outputs and one of the 32 interleaver outputs. To mimic the load of the sub-ADC input capacitance, a 30-fF MOM capacitor was added to the output of each inter-leaver lane, including the one with the 50-Ω output buffer. As seen in Fig. 32a, the ADC front-end has measured 3-dB bandwidths of 61 GHz and 55 GHz, respectively, from the analog input to the first level sampler output and to the second level sampler outputs, respectively. The track and hold function of the first level sampler is sufficient for input signals up to 61 GHz, while the bandwidth from the analog input of the ADC front end to each sample-and-hold outputs exceeds the requirements for transferring the sampled signal to the sub-ADCs. As seen from Fig. 32b, the ADC front-end gain can be adjusted from the *n*- and *p*-MOSFET back gate voltages of the CMOS TIAs used in the second stage of the CML Cherry-Hooper buffers. Fig. 32c shows the measured output power and signal-to-distortion ratio (SDR) at different input signal frequencies as a function of signal amplitude. The measured input compression point for 1-GHz and 56-GHz input sinusoidal signals is −0.5 dBm and −2.5 dBm, respectively. The SDR remains better than 30 dB at an input power of −2-dBm (500-mV$_{pp}$) per side up to 22 GHz, the highest frequency at which the 3rd harmonic can be captured with the 50-GHz bandwidth spectrum analyzer used for testing the ADC front-end.

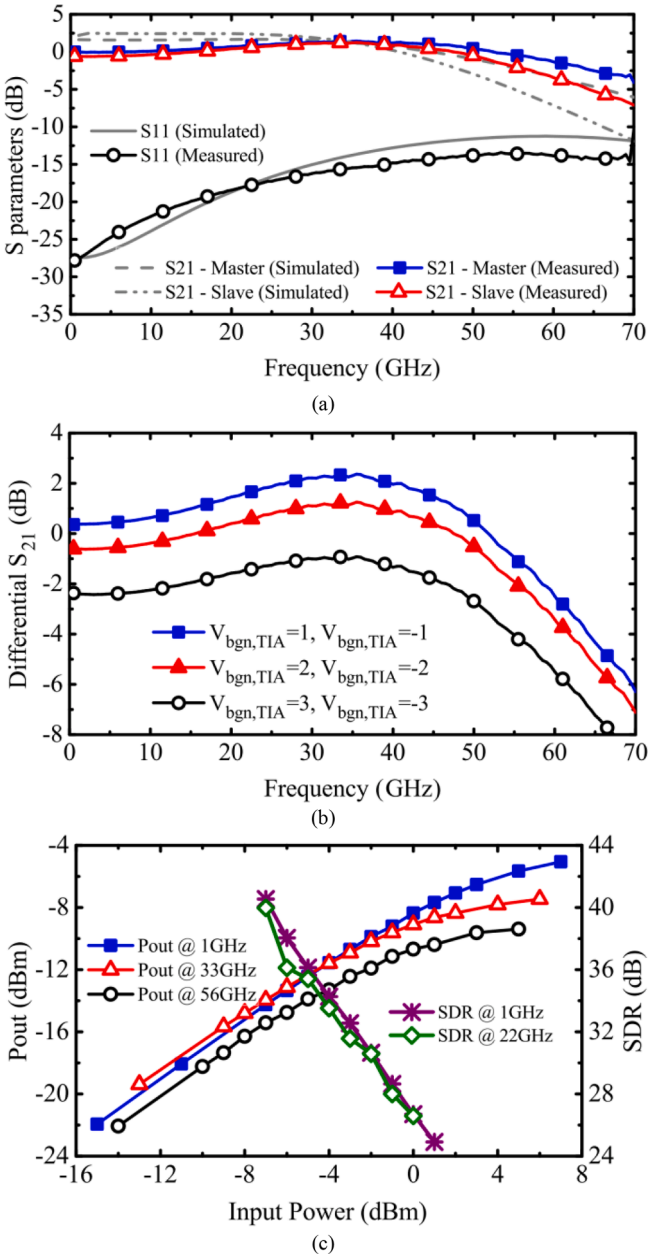


Fig. 32. Performance of the 32× interleaver analog front-end. a) Measured and simulated S-parameters of the 32× interleaver taken at the master and slave T&H outputs. b) Measured differential gain of an individual analog lane in the interleaver as a function of the backgate voltages of the TIA stages in the *n*-MOS Cherry-Hooper buffers. c) Measured input compression point and SDR of the interleaver at different input frequencies.

3.5. *Low-noise broadband CMOS-inverter TIAs for fibreoptic and quantum computing applications*

The back gate bias technique discussed in Section 3.1 was also applied to the design of two different CMOS inverter-based TIAs intended for operation at 2 K as a test vehicle towards the development of a monolithically integrated QPU such as that in Fig. 4. In this application, the TIA must amplify the small tunneling current of the capacitively-coupled SET/SHT quantum dots in the range of 10 pA to 10nA onto a 50-Ω load with at least a few mV of voltage swing. This range of currents matches the tunneling peak currents measured in Figs. 16 and 17. This requires a transimpedance gain of 100–140 dBΩ and less than 10-pA$_{rms}$ input-referred noise current at the intended 2-K operating temperature for detection of narrowband signals. The integration bandwidth over which this noise level is achieved dictates the speed of the qubit readout operation: the larger the integration bandwidth, the faster the readout and therefore, the lower the input equivalent noise that must be achieved. The TIA schematics are shown in Fig. 33. They feature a number of cascaded CMOS inverters with and without transimpedance feedback in a chain formed by an input TIA stage followed by a CMOS-inverter based Cherry-Hooper stage. Ensuring that all CMOS inverters in the chain have input and output DC voltages of precisely $V_{DD}/2$ is critical to maintain all stages biased in the active region, with low offset voltage,

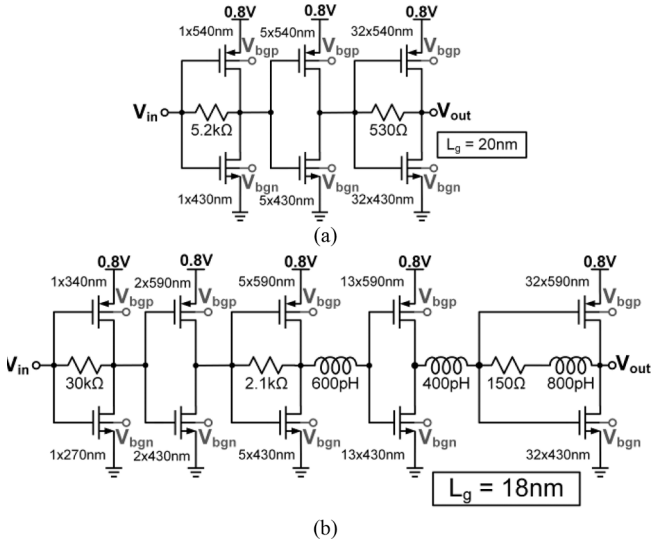


Fig. 33. Schematic of a) 3-stage TIA with 2 CMOS Cherry-Hooper stages and 1 CMOS buffer and b) 5-stage TIA with 3 CMOS Cherry-Hooper stages and 2 CMOS buffers.

low noise, high gain, and good linearity. The 3-stage TIA of Fig. 33a is a design which minimizes the layout area by using only MOSFETs and feedback polysilicon resistors, which were chosen due to their resistance invariance from 300 K to 2 K [2,16]. Fig. 34a and 34b show that the TIA is output matched to 50 Ω up to 70 GHz with better than −10 dB return loss and peak transimpedance gain of 80 dBΩ at 2 K. Since this early design did not meet the target gain specifications, an improved 5-stage TIA with inductive peaking techniques was designed, as illustrated in Fig. 33b. The measured small signal performance is shown in Fig. 34c through e. The peak transimpedance gain of 108 dBΩ was measured at room temperature when the *n*-MOSFETs in all CMOS inverters were biased at 0.25 mA/μm. Simulation predicts the gain increases to 112 dBΩ at 12 K. The simulated room temperature input-referred noise of 0.83 pA/$\sqrt{Hz}$ agrees well with measurements and improves to 0.19 pA/$\sqrt{Hz}$ at 12 K, the lowest temperature at which the circuit simulator still converges.

$$F_{TIA} = 1 + \frac{T_0}{T}\left(R_S W_{FET}\omega_a^2 G_{FET} + \frac{R_S R_F}{|Z_F|^2} + \frac{R_S R_{FET}}{W_{FET}}\left|Y_S + \frac{1}{Z_F} + W_{FET}\omega_a\left(G_{C,FET} + jB_{C,FET}\right)\right|^2\right) \quad (8)$$

The gate widths of the MOSFETs in the first CMOS inverter of the 5-stage TIA were chosen not only to provide a smaller load capacitance for the $W_f = 70$ nm SHT, but also to optimize the input-referred noise of the TIA at 2 – 4 K to get the performance shown in Fig. 34d. Assuming that the TIA noise is dominated by the contributions of the *n*- and *p*-MOSFETs in the first stage and by the feedback resistance R_F ($Z_F = R_F + jX_F$), the optimal MOSFET widths that minimize the input-referred noise current can be derived as a function of the output admittance of the SHT, acting as the signal source whose current is being amplified ($Y_S = 1/Z_S = 1/R_S + jB_S$), the 3-dB bandwidth of the first TIA stage ($2\pi f_a = \omega_a$), and the MOSFET or CMOS inverter noise parameters at the operation temperature of 2 – 4 K [37]. The optimal effective width (W_{FET}) of the CMOS inverter as a composite transistor in the shunt feedback TIA is derived using the measured width-normalized small signal parameters in Table 2 for the *n*- and *p*-MOSFET at three temperatures (3.3 K, 300 K, 400 K) when they are biased at the minimum noise figure current density, J_{OPT}, of 0.2 mA/μm by adjusting the back gate voltage. The noise factor of the TIA is given by [37]:

$$R_{FET} = \frac{P}{g_m'} + R_s' + R_g' \quad (9)$$

$$G_{FET} = \frac{PR_s'\left(C_{gs}' + C_{gd}'\right)^2}{P + g_m'\left(R_s' + R_g'\right)} \quad (10)$$

$$G_{C,FET} = 0 \quad (11)$$

$$B_{C,FET} = \frac{P\left(C_{gs}' + C_{gd}'\right)}{P + g_m'\left(R_s' + R_g'\right)} \quad (12)$$

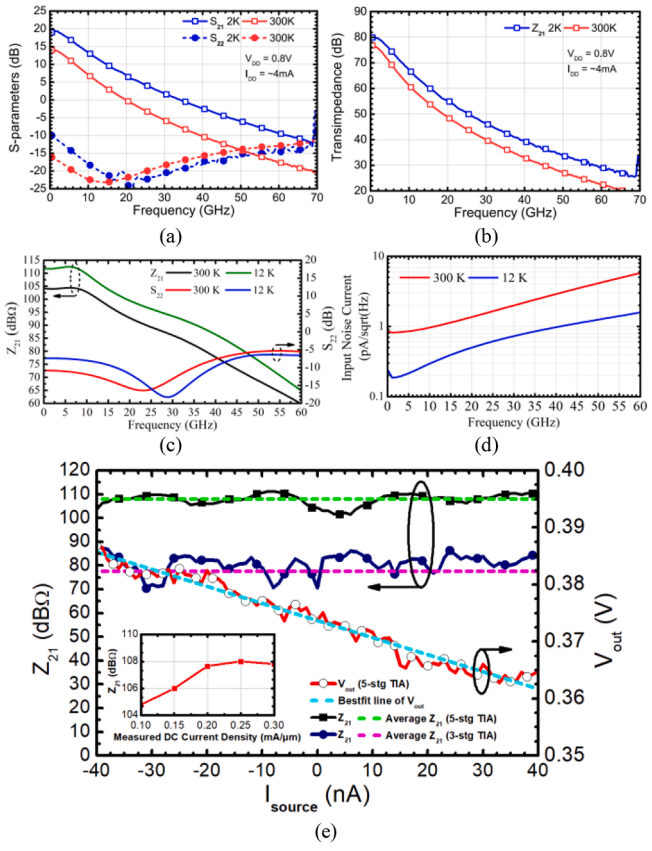


Fig. 34. Performance of the qubit readout TIAs. Measured a) S_{21} and S_{22} and b) Z_{21} of the 3-stage TIA at 2 K and 300 K when biased at $V_{DD} = 0.8$ V and $I_{DD} = 4$ mA (*n*-MOSFET current density of 250 μA/μm) [16]. Simulated c) Z_{21} and S_{22} and d) equivalent input referred noise current of the 5-stage TIA at 12 K and 300 K when biased at $V_{DD} = 0.8$ V and $I_{DD} = 5.7$ mA (*n*-MOSFET current density of 250 μA/μm). e) Measured Z_{21} and output voltage as a function of input current at 300 K for both TIAs at peak Z_{21} current density bias [2].

Table 2
Small-signal parameters for CMOS TIAs.

Device & Bias Condition	Parameter*	3.3 K	300 K	400 K
n-MOSFET @	g_m'(mS/μm)	1.86	1.36	1.15
$V_{DS} = 0.4$ V	R_g'(kΩ·μm/finger)	2.68	2.85	3.38
$V_{GS} = 0.4$ V	R_s'(Ω·μm)	227	213	274
$I_{DS}/W = 0.2$ mA/μm	C_{gs}'(fF/μm)	0.603	0.668	0.528
	C_{gd}'(fF/μm)	0.431	0.436	0.398
	$W_{FET,opt}'$(μm·kΩ·GHz)	303	255	305
p-MOSFET @	g_m'(mS/μm)	1.48	1.16	0.987
$V_{DS} = -0.4$ V	R_g'(kΩ·μm/finger)	2.28	2.60	3.14
$V_{GS} = -0.4$ V	R_s'(Ω·μm)	374	214	292
$I_{DS}/W = 0.2$ mA/μm	C_{gs}'(fF/μm)	0.726	0.893	0.612
	C_{gd}'(fF/μm)	0.500	0.482	0.492
	$W_{FET,opt}'$(μm·kΩ·GHz)	227	187	237
CMOS @	g_m'(mS/μm)	3.34	2.52	2.14
$V_{DS} = \pm 0.4$ V	R_g'(kΩ·μm/finger)	1.23	1.36	1.63
$V_{GS} = \pm 0.4$ V	R_s'(Ω·μm)	141	107	141
$I_{DS}/W = 0.2$ mA/μm	C_{gs}'(fF/μm)	1.33	1.56	1.14
	C_{gd}'(fF/μm)	0.931	0.918	0.89
	$W_{FET,opt}'$(μm·kΩ·GHz)	130	109	134

*Measured for fully metallized 1× pitch 40 × 20 nm × 430nm *n*-/*p*-MOSFETs with single-side gate contact.

$$P = T_d/(2T) \tag{13}$$

where T_d is the elevated temperature due to the large electric field in the MOSFET channel at the drain end, as described in the Pospieszalski noise model [38], $T_0 = 290$ K, and T is the local physical temperature at the source end. P (or T_d) must be extracted from transistor noise measurements [38]. In the absence of measurements, a reasonable approximation in most nanoscale CMOS technologies is $P \sim 1$ [37]. Setting the derivative of (8) with respect to the composite CMOS transistor gate width to zero, the optimal width which minimizes the noise factor and the equivalent input-referred noise current of the TIA is found to be:

$$W_{FET,opt} = \frac{1}{f_a}\left|Y_S + \frac{1}{Z_F}\right| \sqrt{\frac{1}{4\pi^2\left(\frac{G_{EET}}{R_{FET}} + G_{C,FET}^2 + B_{C,FET}^2\right)}} = \frac{1}{f_a}\left|Y_S + \frac{1}{Z_F}\right| W'_{FET,opt} \tag{14}$$

Note that $W_{FET,opt}$ predicted by (14) is a function of the small signal and noise parameters of the technology through $W'_{FET,opt}$ which is in units of μm·Ω·GHz, the SET/SHT (or signal source) output admittance, Y_S, and TIA feedback impedance, Z_F. It can be simulated or calculated by hand using (9) to (13) for a given technology, temperature, and bias current density for quick hand design of TIAs.

Assuming the SET (or SHT) output resistance is $R_S = 50$ kΩ (as shown in Section 2.3) and the first TIA stage has $R_F = 30$ kΩ and $f_a = 19$ GHz, the optimal equivalent CMOS transistor width given by (14) for 3.3-K operation is 360 nm. With a negligible increase in noise, a slightly smaller composite CMOS transistor width of 300 nm was selected in the final design to reduce the fanout between the SET and the CMOS TIA and maximize bandwidth. The TIA stage bandwidth of 19 GHz was chosen to allow for the significant bandwidth reduction when 5 TIA and CMOS inverter stages are cascaded to increase the transimpedance gain and match the output impedance to 50 Ω.

The gate widths of the *n*- and *p*-MOSFETs that form the composite CMOS transistor with an equivalent width of 300 nm, can be obtained from:

$$W_{(n/p)FET,opt} = \frac{g'_{m,CMOS}}{2g'_{m,(n/p)MOS}} W_{FET,opt} \tag{15}$$

Using the 3.3 K $g'_{m,n}$, $g'_{m,p}$, and $g'_{m,CMOS} = g'_{m,n} + g'_{m,p}$ from Table 2, (15) gives $W_n = 270$ nm and $W_p = 340$ nm. Fig. 35 plots the main noise contributors to the input-referred noise current simulated in Fig. 34d. The noise current contribution due to $R_F \sim$ sqrt(T) while the MOSFET drain current noise does not change much with temperature [38]. As a result, as it can be observed from Fig. 35 based on the frequency at which the transistor noise contribution becomes larger than the R_F noise contribution, the optimal W_n and W_p values are different at 300 K than

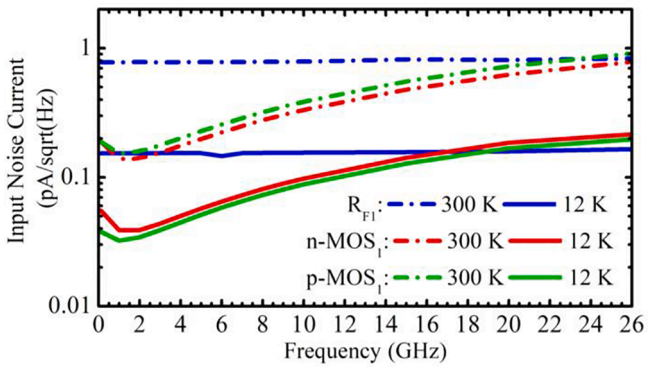


Fig. 35. Simulated equivalent input referred noise current contributions of the MOSFETs and feedback resistor in the first CMOS TIA stage of the 5-stage TIA at 12 K and 300 K when biased at $V_{DD} = 0.8$ V and $I_{DD} = 4.6$ mA (*n*-MOSFET current density of 200 μA/μm).

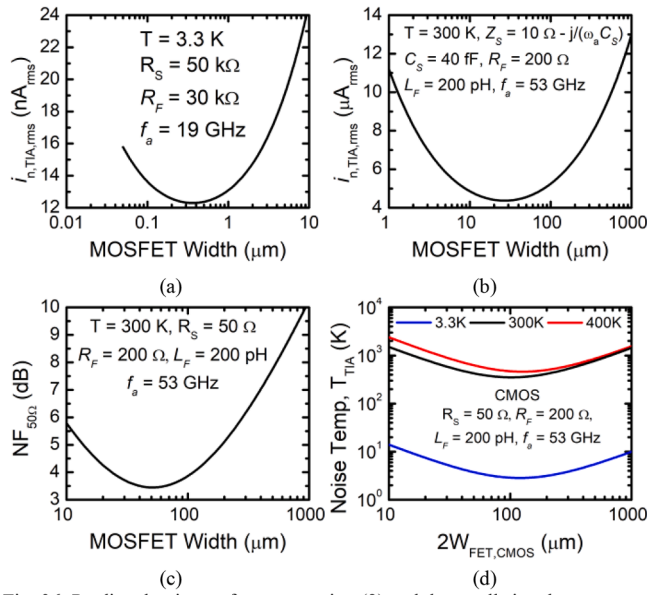


Fig. 36. Predicted noise performance using (8) and the small signal parameters in Table 2. for CMOS TIAs ($V_{DD} = 0.8$ V, $I_{DD} = W_{FET} \times 0.2$ mA/μm) vs. W_{FET} for different application scenarios: a) SET readout TIA in a monolithically integrated QPU operating at 3.3 K; b) 300-K 64-GBaud TIA in a fibreoptic receiver; 50-Ω noise figure for c) broadband 50-Ω input matched CMOS TIA operating at 300 K and d) broadband 50-Ω input matched CMOS TIA operating at 3.3 K, 300 K, and 400 K.

at 12 K. It is clear from these simulations that the process of minimizing the noise figure or total input-referred noise current of the TIA for a given bandwidth and temperature is equivalent to making the input-referred noise current due to the MOSFETs equal to the input-referred noise contribution of the feedback resistor at the intended 3-dB bandwidth, f_a, of the TIA.

Next, we apply the TIA noise-optimization design methodology in three different application scenarios and compare the noise performance achieved for those applications. Fig. 36a through 36c plot the noise figure of CMOS TIA stages vs. *n*-MOSFET gate width for each application scenario. Fig. 36a describes the scenario of a 3.3-K TIA designed for high-bandwidth readout of the SETs/SHTs in a monolithically integrated QPU with $R_S = 50$ kΩ, $R_F = 30$ kΩ, and $f_a = 19$ GHz. In Fig. 36b, it is assumed that the TIA was designed for 64-GBaud PAM-4 operation in a fibreoptic receiver operating at 300 K. The TIA is driven by a generic 50-GHz bandwidth photodiode, modeled as a 40-fF capacitance in series with a 10-Ω resistor ($Z_S = 10\ \Omega - j/\omega_a C_D$, $C_D = 40$ fF) while $R_F = 200$ Ω, $X_F = \omega L_F$, $L_F = 200$ pH and $f_a = 53$ GHz. Finally, the application scenario in Fig. 36c assumes that the CMOS TIA was designed as a generic low-noise, broadband input buffer matched to 50-Ω for ICs operating at 300 K. In all three application scenarios, the noise penalty for selecting a different W_{FET} than the optimal value can clearly be observed.

Fig. 36d compares the noise temperature of the 50-Ω input matched CMOS TIA at 3.3 K, 300 K, and 400 K to illustrate how to optimize the MOSFET sizes over temperature. As expected, the noise temperature is proportional to temperature. The interesting finding is that the optimal MOSFET width is 20% larger at 3.3 K and 400 K than at 300 K. This is an example where designing a circuit specifically for operation at cryogenic temperature will lead to a different transistor size and power consumption than at room temperature. Altogether, the FDSOI CMOS inverter provides a robust building block for low-noise, broadband TIAs where the desired bias current is constant over temperature and process by the backgate voltage bias and the noise/bandwidth performance optimized by the MOSFET width.

3.6. Broadband mm-Wave FDSOI switch for quantum computing applications

Unlike other CMOS technologies, FDSOI switches benefit from the low parasitic capacitance to the substrate due to the isolation provided by the buried oxide layer. Also unique to FDSOI, the time constant, $\tau = R_{on} \times C_{off}$, of the MOSFET switch can be tuned using the back gate voltage. For switches designed for qubit control, such as those in Fig. 4, the input signal is on the order of a few mV or smaller [39] and linearity can be sacrificed in favor of the on/off isolation. The latter must be better than −40 dB to keep the error rates due to idle operation on the order of or smaller than $\sim 10^{-4}$ for idle times on the order of a π-rotation gate. Since the *n*-MOSFET parasitics are lower than those of either the *p*-MOSFET or the CMOS switch, only the small signal equivalent circuit parameters of the *n*-MOSFET switch are shown in Table 3 to guide the design of a broadband single-pole single-throw, SPST, shunt switch with low insertion loss and high isolation up to 220 GHz [40]. This switch is incorporated in a quantum processor test vehicle needed to characterize the spin resonance and Rabi frequencies of FDSOI hole-spin spin qubits as a function of the applied DC magnetic field. The switch schematic is shown in Fig. 37a. It features four *n*-MOSFETs connected by series inductors to form an artificial transmission line of characteristic impedance:

$$Z_0 = \sqrt{\frac{L_d}{C_{off} + 2C_d}} \tag{16}$$

where C_d models half of the parasitic capacitance of the inductor to ground on each side of the inductor. The 12.5 kΩ resistors added in series with the MOSFET gate reduce the off capacitance between the drain and ground at $V_{GS} = 0$ V to:

$$C_{off} = N_f W_f \left(C_{ds}^{'} + \frac{C_{gs}^{'} C_{gd}^{'}}{C_{gs}^{'} + C_{gd}^{'}} \right) \tag{17}$$

The switch layout depicted in Fig. 37b was used. To minimize the layout footprint and maximize bandwidth, the inductors are formed as microstrip line sections placed directly above the 4 MOSFETs whose drain connections are tapped off from the microstrip line while their source contact stripes are embedded into the microstrip line ground plane.

The measured performance of the standalone switch is summarized in Fig. 38. The insertion loss (Fig. 38a), lower than 3.2 dB up to 220 GHz, is generally best at $V_{BG} = -0.5$ V due to the increased *n*-MOSFET OFF-impedance. However, by tuning C_{off} from the back gate voltage, the characteristic impedance of the artificial transmission line is closest to 50 Ω at $V_{BG} = 0$ V, where the best insertion loss is observed. The isolation (Fig. 38b) improves as the ON-resistance decreases and is best at $V_{BG} = 4$ V. Assuming V_{BG} is held constant during operation of the switch, the best on/off isolation shown in Fig. 38c is achieved at $V_{BG} = 1.5$ V. Fig. 38d compiles the switch performance at 60 GHz and 200 GHz vs. back gate voltage. The switch achieves at least −30 dB of on/off isolation from 35 GHz to 220 GHz with the best on/off isolation of −46 dB at 200 GHz.

The noise floor in the VNA setups above 110 GHz prevented accurate measurement of the on/off isolation in the switch breakout. To overcome this problem, a variable gain LNA, VGLNA, with 10–12 dB gain at 196 GHz was added to improve the dynamic range of the measurement setup around 200 GHz.

Table 3
Measured 40 × 18 nm × 590nm *n*-MOSFET at $V_{DS} = 1$ mV.

Description	@ $V_{BG} = -0.5$ V	@ $V_{BG} = 4$ V
$C_{gs}^{'}$(fF/μm) @ $V_{GS} = 0$ V	0.40	0.49
$C_{gd}^{'}$(fF/μm) @ $V_{GS} = 0$ V	0.38	0.47
$C_{ds}^{'}$(fF/μm) @ $V_{GS} = 0$ V	0.33	0.15
$R_S^{'} = R_D^{'}$(Ω·μm) @ $V_{GS} = 0.8$ V	167	122

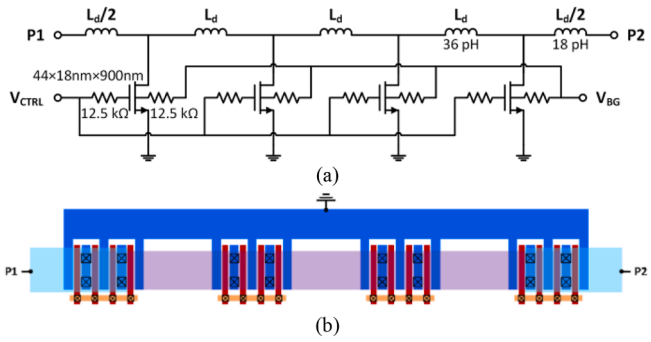


Fig. 37. Distributed SPST switch a) schematic and b) layout. The microstrip line metal (cyan and purple) spans across 4 shunt switch transistor drains [40]. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

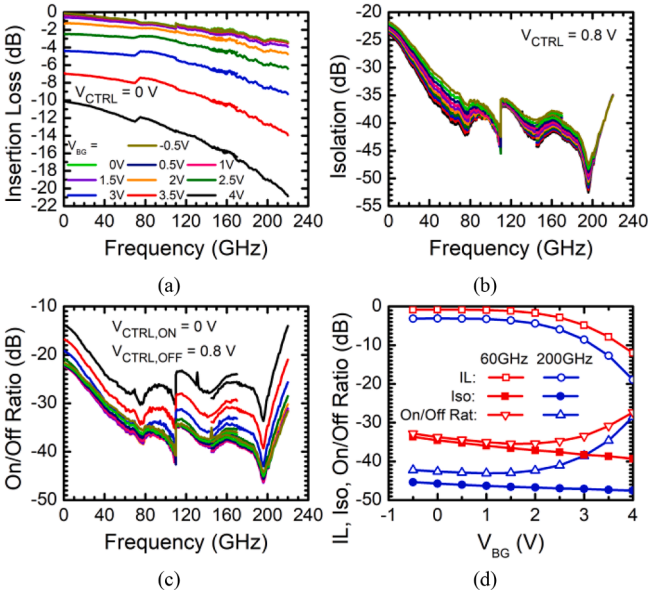


Fig. 38. Performance of the SPST switch measured from its standalone breakout. 300 K measurements of a) insertion loss, b) off isolation, and c) on/off isolation for different backgate voltages using the legend in (a). d) Switch performance at 60 GHz and 200 GHz vs. V_{BG} at 300 K.

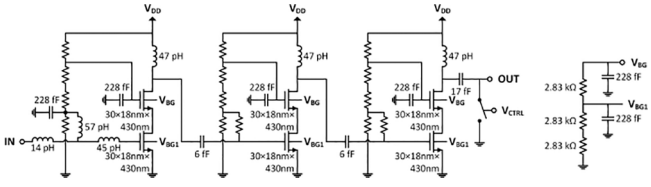


Fig. 39. Schematic of VGLNA. SPST switch at the output has the same schematic as in Fig. 37 [40].

The schematic of the VGLNA (Fig. 39) consists of the 3-stage cascode LNA followed by the same broadband switch of Fig. 37a. Together, the LNA and the switch form a spin manipulation circuit at 200 GHz. The measured performance of the VGLNA at room temperature is shown in Fig. 40, revealing that the switch on/off ratio reaches a maximum of −55 dB at ∼ 200 GHz. The 9-dB improvement in on/off isolation compared to the standalone switch matches the gain of the 3-stage LNA, suggesting that measurement of the on/off ratio is still noise floor

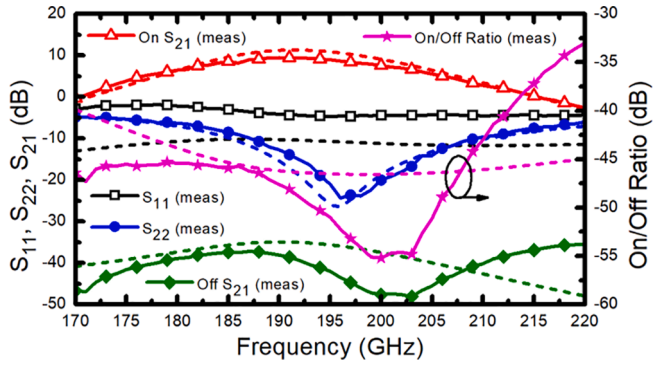


Fig. 40. Measured (lines and symbols) vs. simulated (dashed lines) S-parameters of the VGLNA. Switch controls variable gain through isolation [40].

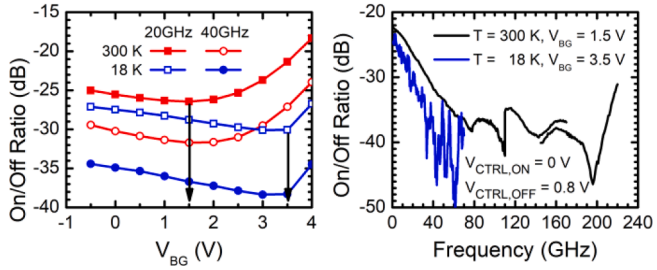


Fig. 41. a) Measured on/off ratio of the SPST switch vs. V_{BG} at 20 GHz and 40 GHz and at 18 K and 300 K with the optimal V_{BG} value indicated for each temperature by arrows. b) Measured on/off ratio of the SPST switch vs. frequency at the optimal V_{BG} bias.

limited and that the on/off isolation might be better than −55 dB.

Finally, the standalone switch was also measured at 18 K to verify its performance at cryogenic temperatures. Fig. 41a shows that the best on/off isolation occurs at V_{BG} = 3.5 V, corresponding to a 2 V increase relative to the room temperature optimal value for V_{BG}. This 2-V increase matches exactly with the 192 mV *n*-MOSFET V_t shift from 300 K to 2 K (Fig. 19b) and the 95 mV/V dependence of V_t on V_{BG} observed at both room and cryogenic temperatures in Fig. 21. It suggests that the optimal V_{BG} for maximizing the switch on/off ratio at any given temperature in the 2 K to 400 K range can easily be determined from the measured MOSFET V_t variation with temperature and V_{BG}. Fig. 41b compares the measured on/off ratio at 18 K at the optimal V_{BG} value to the best room temperature on/off isolation, showing approximately 5 dB improvement at 18 K up to 70 GHz, the upper frequency limit of the cryogenic probe station. If the 5 dB improvement extends up to 200 GHz, this would translate to an on/off ratio of at least −60 dB, making the switch performance suitable for implementing single qubit rotation gates with ~ 10^{-6} error in a quantum processor with qubits operating at that frequency [39].

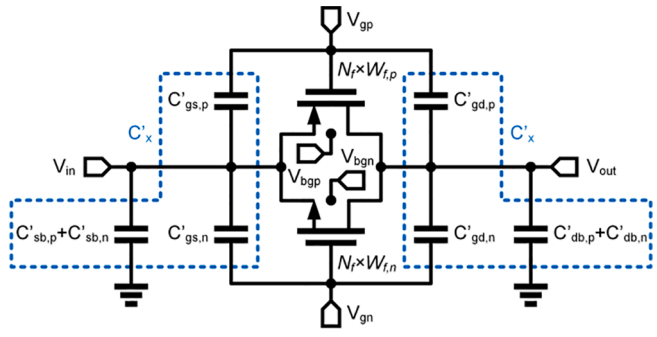


Fig. 42. FDSOI CMOS switch schematic. Transistor capacitances per unit gate width are indicated.

3.7. Linear CMOS switches for fibreoptic ADC front-ends

For applications which require high linearity, such as the high-speed fibreoptic ADC front-end in Fig. 2b, CMOS pass-gate switches, like that depicted in Fig. 42, are preferred over *n*-MOSFET only switches. Because of the symmetric characteristics and nonlinearities of the matched *p*-and *n*-MOSFETs, CMOS pass-gate switches exhibit improved linearity for rail-to-rail input signals and reduced charge injection and clock feedthrough, without the need for complex boot-strapped topologies whose extra parasitics lead to bandwidth degradation. In addition to the requirements for linear operation with large input signals, ideally rail-to-rail, an ADC front-end sampling switch must operate with the highest possible bandwidth, clock frequency, and isolation and low insertion loss. Therefore, its design considerations and requirements are quite different from those used in antenna switches and for the broadband switch in Section 3.6 which operate at moderate sub-GHz switching speeds. In FDSOI, the back gate voltages of the *n*-MOSFET and *p*-MOSFET can be separately controlled to further optimize the performance of the CMOS pass-gate switch as a sampler.

The width-normalized gate-source (C'_{gs}), gate-drain (C'_{gd}), and source/drain-bulk (C'_{db}) capacitances and the ON-resistance (R'_{ON}) were measured at different back gate voltage biases for fully-wired 40 × 18 nm × 430nm *p*- and *n*-channel MOSFETs with 2× minimum gate-to-gate pitch and one-sided gate contact (Fig. 43). The smaller 430 nm MOSFET finger width (compared to the 900 nm one in the 220-GHz bandwidth *n*-MOSFET switch) was selected to maximize f_{MAX} and the switching speed, needed for operation with 32-GHz, 25% duty-cycle clock signal. The measured R'_{ON} of 300 Ω × μm, obtained at V_{DS} = 0 V and V_{GS} = ±0.6 V, is identical for both *n*- and *p*-channel MOSFETs. The capacitance characteristics are also almost identical, with the *p*-MOSFET showing ~ 0.1 fF/μm larger gate-source and gate-drain capacitances. As can be seen in Fig. 43a, apart from C'_{gs} in the subthreshold region at low V_{GS}, there is little variation of the switch capacitances with respect to the back gate voltage. In contrast, the simulation results in Fig. 43d show a strong

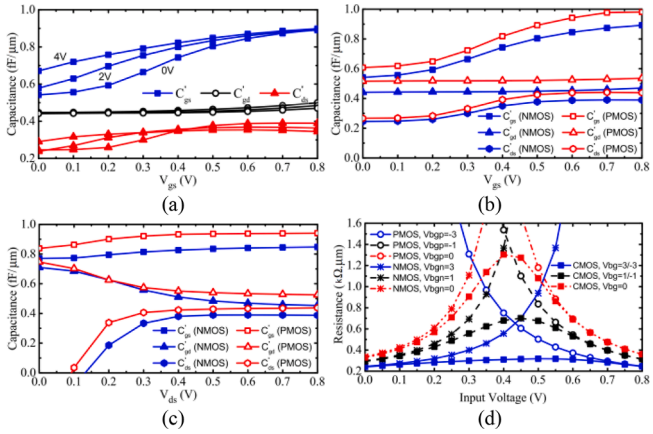


Fig. 43. MOSFET small signal parameters relevant for CMOS switch design. a) Measured 2× pitch 40 × 18 nm × 430nm single gate contact *n*-MOSFET capacitances per unit gate width as a function of V_{GS} for different backgate voltages at V_{DS} = 0.8 V. Comparison of the measured capacitances per unit gate width for 2× pitch single gate contact *n*- and *p*-MOSFETs b) as a function of V_{GS} at V_{DS} = ±0.8 V and c) as a function of V_{DS} at V_{GS} = ±0.6 V. d) Simulated gate width-normalized ON-resistance of *n*-MOSFET ($W_{f,n}$ = 430 nm), *p*-MOSFET ($W_{f,p}$ = 540 nm), and CMOS ($W_{f,n}$ = 430 nm, $W_{f,p}$ = 540 nm) switches as a function of the input signal level for different backgate voltages.

Table 4
Technology parameters for *n*-mos, *p*-mos and cmos switches.

Description	*N*-MOS	*P*-MOS	CMOS
$C'_{gs,ON} = C'_{gd,ON}$(fF/μm)	0.7	0.8	1.7*
$C'_{gs,OFF} = C'_{gd,OFF}$(fF/μm)	0.55	0.6	1.3*
$C'_{sb,ON} = C'_{db,ON}$(fF/μm)	0.35	0.35	0.79*
$C'_{sb,OFF} = C'_{db,OFF}$(fF/μm)	0.25	0.25	0.56*
$C'_{x,ON}$(fF/μm)	1.05	1.15	2.5*
$C'_{x,OFF}$(fF/μm)	0.8	0.85	1.87*
R'_{ON}(Ω·μm) @ V_{bgn} = 3 V, V_{bgp} = −3V	550	880	300*

*Value for $W_{f,n}$ = 430 nm and $W_{f,p}$ = 540 nm.

dependence of R'_{ON} on the backgate voltage, allowing for its tunability. Moreover, unlike *n*-MOSFET or *p*-MOSFET switches, the CMOS switch resistance remains practically constant as the input signal is changed from 0 to 0.8 V, suggesting much better linearity. Table 4 summarizes the average gate width-normalized capacitances and ON-resistance of the *n*-MOSFET, *p*-MOSFET, and CMOS switches when the source and drain nodes are biased at $V_{DD}/2 = 0.4$ V (i.e $V_{DS} = 0$ V) and $V_{GS} = \pm 0.4$ V and when $C_{gs} = C_{gd}$ which will be used in the equation-based design of the ADC interleaver (or sampling) front end with *m* first-level (master) track-and-hold (TH) circuits each driving *n* second-level (slave) TH circuits, each loaded by a hold capacitor, C_H, and performing an overall sample and hold (SH) function, as in the ADC front-end of Fig. 2b, where $m = 4$ and $n = 8$.

The simplified block diagram and equivalent circuit in Fig. 44 can be used to analyze the performance of the sampling front end and to find the best sizes for the first-level and second-level CMOS TH switches which maximize the analog front-end bandwidth. In this analysis, the output resistance of the buffer (R_{out}) which drives the TH switches and hold capacitance (C_H) are assumed given. In the case of the first-level TH circuits, R_{out} is given by the output resistance of the master buffer, the CML *p*-MOSFET Cherry-Hooper amplifier discussed in Section 3.4 and depicted in Fig. 31a and C_H is the input capacitance of the slave buffer. For the second-level TH switches, R_{out} is the output resistance of the slave buffer, the CML *n*-MOSFET Cherry-Hooper amplifier (Fig. 31b) and C_H is the capacitance of the hold capacitor. In the analysis, only one switch is ON at any given time. The transfer function of this second order

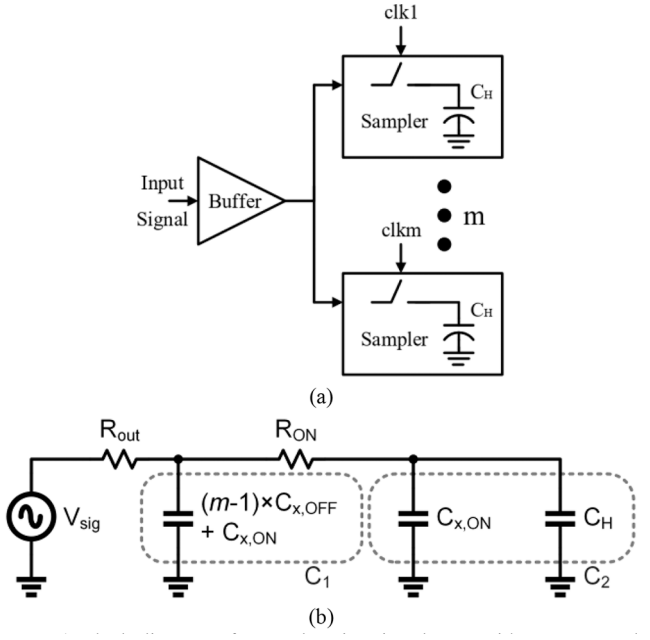


Fig. 44. a) Block diagram of an analog time interleaver with *m* TH samplers and b) equivalent circuit model.

circuit is expressed as:

$$H(s) = \frac{1}{R_{ON}R_{out}C_1C_2s^2 + [R_{out}(C_1 + C_2) + R_{ON}C_2]s + 1} \tag{18}$$

where R_{ON}, C_1, and C_2 are the CMOS switch ON-resistance, and the total capacitance at the input and output of the switch, respectively, and can be cast as a function of the MOSFET layout geometry:

$$R_{ON} = \frac{R'_{ON}}{N_f W_f} \tag{19}$$

$$C_1 = (m-1)\left(C_{x,OFF,n} + C_{x,OFF,p}\right) + C_{x,ON,n} + C_{x,ON,p} \tag{20}$$

$$C_2 = C_H + C_{x,ON,n} + C_{x,ON,p} \tag{21}$$

$$C_x = N_f W_f \left(C'_{gs} + C'_{sb}\right) = N_f W_f \left(C'_{gd} + C'_{db}\right) \tag{22}$$

where N_f and W_f are the number of gate fingers and gate finger width of the identically sized *n*-MOSFET and *p*-MOSFET in the CMOS switch and $C_{x,ON}$ and $C_{x,OFF}$ are the per-side capacitances of the CMOS switch when ON and OFF. The *n* and *p* subscripts denote the capacitance of the *n*- or *p*-

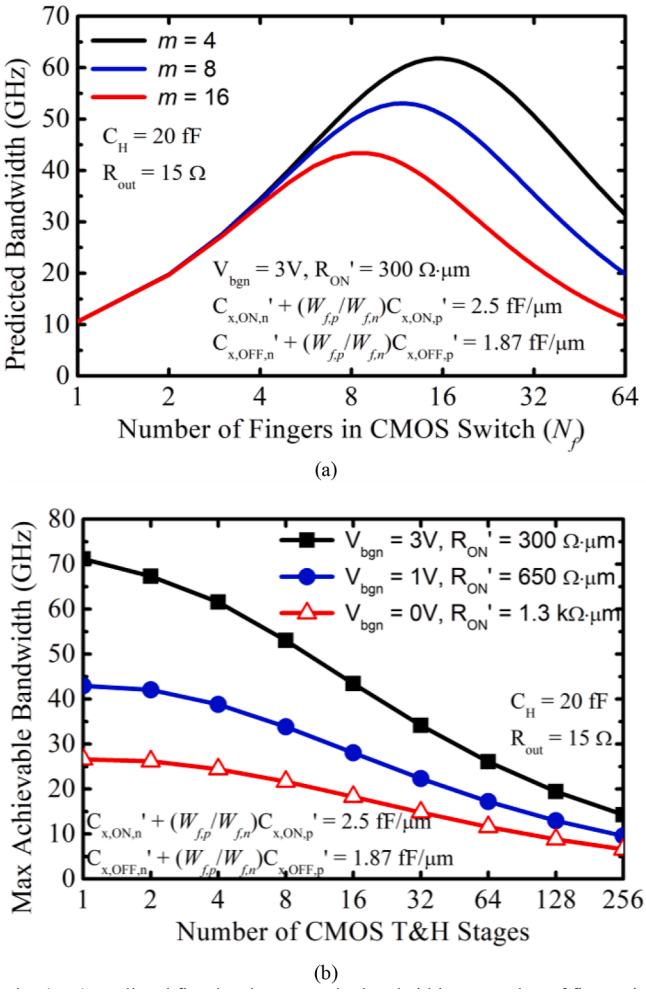


Fig. 45. a) Predicted first-level TH sampler bandwidth vs. number of fingers in the CMOS switch for an interleaver with 4, 8, and 16 CMOS TH switches b) Predicted maximum first-level time-interleaver bandwidth vs. number of CMOS TH swicthes, assuming the CMOS switches are optimally sized for peak bandwidth at each different back gate voltage. The MOSFET small signal parameters in Table IV have been used.

MOSFET, respectively. The 3-dB bandwidth can be found from the following expression:

$$BW = \frac{1}{2\pi\sqrt{A_1}}\sqrt{1-\frac{A_2^2}{2A_1}+\sqrt{\left(1-\frac{A_2^2}{2A_1}\right)^2+1}}$$
$$A_1 = R_{out}R_{ON}C_1C_2 \quad (23)$$
$$A_2 = C_1R_{out} + C_2(R_{out}+R_{ON})$$

For the first level time-interleaver ($R_{out} = 15\ \Omega$ and $C_H = 25$ fF), the bandwidth is plotted vs. the number of gate fingers in the CMOS TH switches for $m = 4$, $m = 8$, and $m = 16$ in Fig. 45a. As expected, the peak bandwidth decreases as the number of time-interleaved sub-ADC lanes increases. To understand the dependence of the optimal N_f on the technology parameters, a special case is considered where the parasitic capacitance of the second-level switch, C_{SW} is absorbed in the hold capacitor (i.e. $C_2 = C_H$). This case also applies when C_H is much larger than the parasitic capacitance at the output of the switch. In this case, A_1 is independent of N_f and the bandwidth is maximized when A_2 is minimized. The optimal N_f which maximizes the bandwidth is obtained by setting the derivative of A_2 with respect to N_f to zero:

$$N_{f,opt} = \frac{1}{W_{f,n}}\sqrt{\frac{\dot{R_{ON}}C_H}{R_{out}\left((m-1)\left(\dot{C}_{x,OFF,n}+\frac{W_{f,p}}{W_{f,n}}\dot{C}_{x,OFF,p}\right)+\dot{C}_{x,ON,n}+\frac{W_{f,p}}{W_{f,n}}\dot{C}_{x,ON,p}\right)}} \quad (24)$$

Several observations can be made. First, $N_{f,opt}$ is approximately proportional to the square root of the ratio of the ON-resistance to the capacitance of each gate finger. In FDSOI CMOS technology, the back gate voltage can be used to tweak this ratio. Increasing the forward body-bias of the back gate results in smaller switch resistance while the capacitance remains almost unchanged. Therefore, to maximize the bandwidth, the sampler should be sized for the MOSFET parasitics at a specific back gate voltage. Second, for larger load capacitances and smaller buffer output resistance, the number of gate fingers in the CMOS switch should be increased. When the buffer size is increased to improve the bandwidth, N_f should be adjusted based on (24). Finally, an ADC architecture with a larger number of time-interleaved sub-ADCs results in a smaller optimal size for the CMOS switches. However, the best possible bandwidth that can be achieved is also smaller. Fig. 45b plots the maximum achievable bandwidth vs. number of switches for this 22-nm FDSOI CMOS technology at different CMOS switch back gate voltages, assuming the switches are sized according to (24). It shows that the highest bandwidth is achieved when the switches are more forward biased ($V_{BG} = 3$ V, $V_{BGP} = -3$V).

While (24) gives the CMOS switch size for the best bandwidth, it is best to use a slightly smaller switch size than the optimal to reduce clock feed-through due to the capacitive divider formed by the MOSFET switch parasitic capacitances and the load capacitor C_H. In the case of the first-level time-interleaver in the ADC front-end of Fig. 2b (where $m = 4$), the CMOS switches have $N_f = 8$ (half of $N_{f,opt} = 16$) for this reason and the bandwidth was compensated using series inductive peaking between the first-level buffer and the input of the first-level CMOS TH switches.

3.8. Series-stacked cascode amplifiers and drivers

Unlike other CMOS technologies, in SOI CMOS the source and drain nodes of the transistor are DC isolated from the substrate by the BOX layer. Due to this feature, designers can create an artificial device with larger effective voltage swing and breakdown voltage by stacking a relatively large number of *n*-MOSFETs [41] or complementary *n*- and *p*-MOSFETs [42] as in Fig. 46, while achieving very high maximum available gain from DC to 160 GHz, Fig. 47. In FDSOI, unlike, PDSOI and other CMOS technologies, the back gate terminal provides an extra

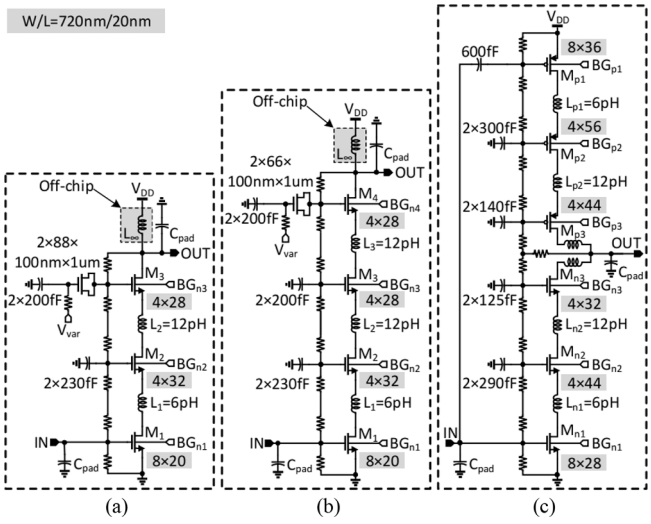


Fig. 46. Schematics of a) 3-stack *n*-MOSFET, b) 4-stack *n*-MOSFET, and c) 3-stack CMOS cascodes in 22-nm FDSOI CMOS technology [48]. The *n*-MOSFET cascodes use a varactor for the top gate capacitor in order to tune the output impedance. All MOSFETs have 20 nm gate length, 720 nm gate finger width, and 2× minimum CPP. The MOSFET sizes are denoted using the convention (multiplicity)x(number of gate fingers).

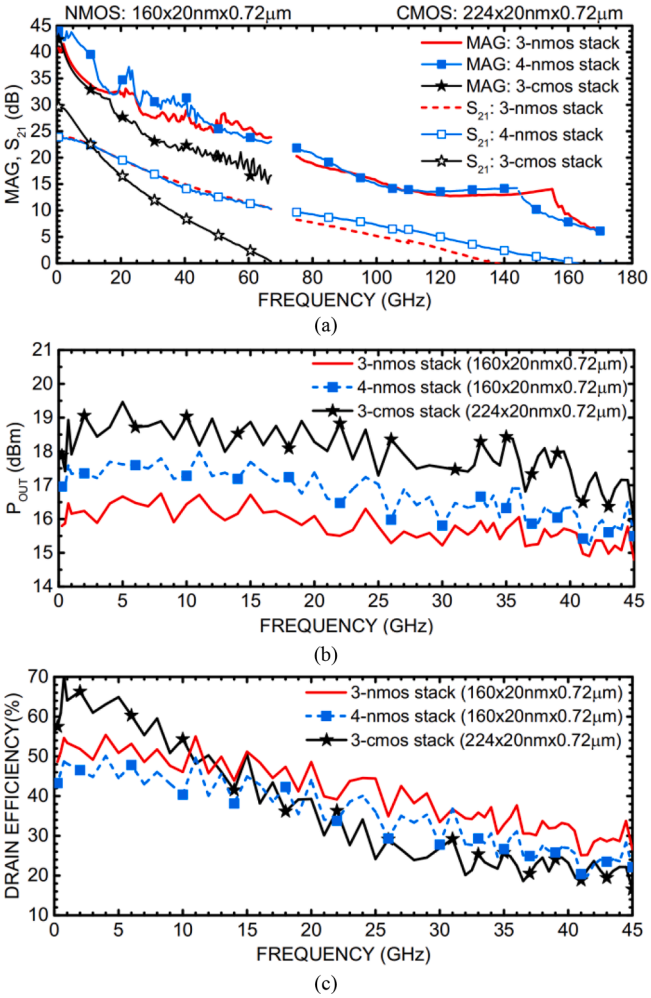


Fig. 47. Measured a) MAG and S_{21}, b) saturated output power, and c) drain efficiency vs. frequency of the stacked cascodes in Fig. 48 at room temperature [48].

degree of freedom which allows the designer to bias these large-swing series-stacked cascodes with equal DC voltage drops between the gate and source and between the drain and source terminals, for maximum swing and linearity, at any current density in the 0.1 mA/μm and 0.4 mA/μm range, as needed for the optimal design of any power amplifier (PA) class: A, AB, B, C, D, D^{-1}, E, F, F^{-1}, etc. In general, for maximum output voltage swing, we want to set the DC value of the drain source voltage, V_{DS}, of all the transistors in the stack equal to the nominal supply voltage, V_{DD}, of the technology. $V_{DD} = 0.8$ V in the case of 22-nm FDSOI technology [21]. The chosen V_{DS} value does depend on the class of PA we wish to implement since the peak-to-peak voltage swing per transistor can be larger than $3V_{DS}$ in F^{-1} and in some class E PAs and may exceed the maximum safe instantaneous voltage of the transistor. In 22-nm FDSOI, the latter is larger than $2.4V_{pp}$ [43].

Fig. 48 shows the simplified schematics of representative cascode stages with 3 and 4 series-stacked *n*-MOSFETs and 3-stacked cascode CMOS inverter which can be used in the derivation of the analysis and design equations for these stages [44,45]. A resistor ladder sets the appropriate DC voltages at the gates of all transistors in the stack, while the back gate voltages are set to produce the desired current density in the stack at the desired V_{GS} values, e.g. $V_{GS} = V_{DS,max}/2$ and $V_{DS} = V_{DS,max}$ for every transistor in the stack [42,46,47], where $V_{DS,max}$ is the maximum safe DC voltage per transistor for the given PA class. This must be smaller than or equal to $V_{DD} = 0.8$ V. The value of the resistance R in this ladder must be chosen sufficiently large to ensure that the high frequency performance of the circuit is minimally impacted. In the case of the series-stacked CMOS cascode, we must also provide some sort of feedback loop (such as resistor R_F) to ensure the DC voltage at the output remains balanced.

If the same width were used for every same-type transistor in the stack, the designer would first determine which back gate voltage gives the desired current density for the common-source transistor at the bottom of the stack ($V_{BG(n/p),1}$) when $V_{GSi} = V_{DS,max}/2$ and $V_{DS} = V_{DS,max}$ and then use (25) below to find all the other back gate voltages:

$$V_{BG(n/p),i} = V_{BG(n/p),1} + (i-1)V_{DS,max} \tag{25}$$

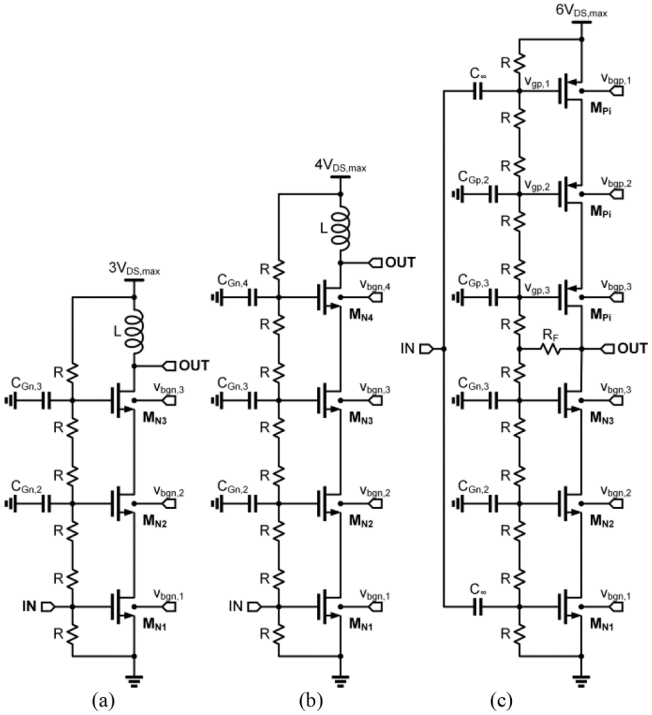


Fig. 48. Example a) 3-stack *n*-MOSFET, b) 4-stack *n*-MOSFET, and c) 3-stack CMOS cascode stages.

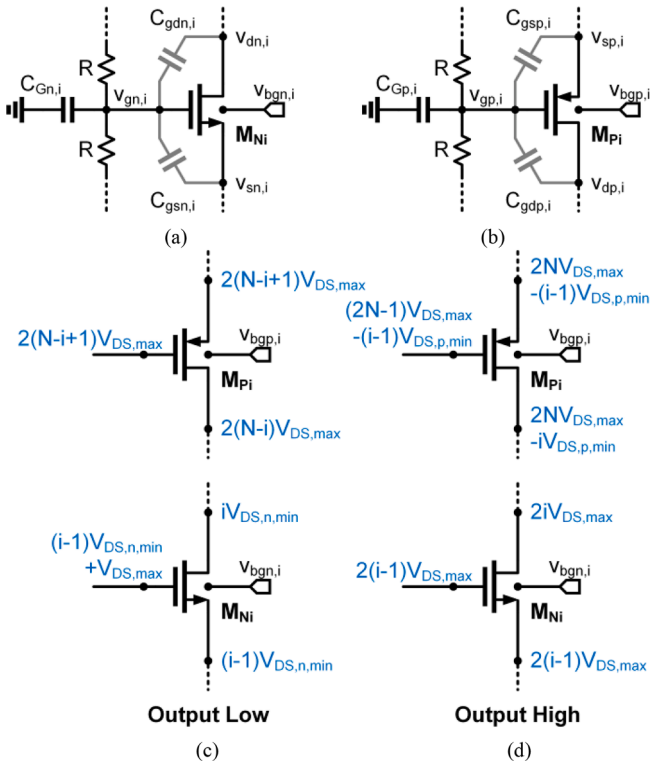


Fig. 49. Equivalent circuit for the *i*th a) *n*-MOSFET or b) *p*-MOSFET in a stacked cascode used to calculate the size of capacitors $C_{Gn,i}$ and $C_{Gp,i}$ to ensure the voltage swing across each transistor in the stack sums in phase at the output. Desired instantaneous voltages at the gate, drain, and source of the *i*th *n*- and *p*-MOSFETs in the stack when the output is c) low and d) high voltage.

Note that (25) and its benefits can only be used in FDSOI technologies. If progressively smaller MOSFET widths were used for each transistor moving up the stack to minimize the output capacitance and maximize bandwidth [42], then a more forward body-biased back gate would be required than that predicted by (25) to bias that MOSFET at a higher current density such that its total drain-source current, V_{GS} and V_{DS} are equal to those of the other transistors in the stack.

To analyze and design the artificial *n*- or *p*-MOSFET device with larger than nominal signal voltages, consider the equivalent circuits depicted in Fig. 49a and b [45]. The size of the capacitors $C_{Gn,i}$ and $C_{Gp,i}$ added from the gate of the *i*th transistor in an *N* stack cascode ($N \geq i \geq 2$) to ground must be determined to ensure the amplitude of the voltage across each pair of terminals (gate, source, drain) remains less than or equal to V_{DD}. We consider also the situation where the instantaneous $|v_{DS}(t)|$ across each *n*- and *p*-MOSFET must never be lower than $V_{DS,n,min}$ and $|V_{DS,p,min}|$ respectively, where these minimum V_{DS} values are chosen to ensure the output impedance of the artificial transistor is sufficiently large for the intended PA class (i.e. transistor stays out of triode region for all output voltage states) and must be greater than or equal to 0 V. When the *n*-MOSFETs in either the *n*-MOSFET or CMOS stacked cascodes are all switched on (output low) we have the situation depicted in Fig. 49c where the output voltage becomes $NV_{DS,n,min}$. When the *n*-MOSFETs are all switched off (output high) we have the situation depicted in Fig. 49d where the output voltage becomes $2NV_{DS,max}$ for the *n*-MOSFET only cascode, and $2NV_{DS,max}$ - $NV_{DS,p,min}$ for the CMOS cascode. The signal amplitude at each node is found by halving the difference between the instantaneous voltages between the two switched output states, resulting in:

$$v_{g(n/p),i} = \frac{2i-3}{2}V_{DS,max} - \frac{i-1}{2}V_{DS,(n/p),min} \tag{26}$$

$$v_{s(n/p),i} = (i-1)V_{DS,max} - \frac{i-1}{2}V_{DS,(n/p),min} \tag{27}$$

$$v_{d(n/p),i} = iV_{DS,max} - \frac{i-1}{2}V_{DS,(n/p),min} \tag{28}$$

These voltages must satisfy the charge-conservation condition across the capacitors connected to each gate node:

$$v_{g(n/p),i}C_{G(n/p),i} + \left(v_{g(n/p),i} - v_{s(n/p),i}\right)C_{gs(n/p),i} + \left(v_{g(n/p),i} - v_{d(n/p),i}\right)C_{gd(n/p),i} = 0 \tag{29}$$

Substituting (26)-(28) into (29) and solving for $C_{G(n/p),i}$ yields [45]:

$$C_{G(n/p),i} = \frac{C_{gs(n/p),i} + 3C_{gd(n/p),i}}{2i - 3 - (i-1)\left(V_{DS,(n/p),min}/V_{DS,max}\right)} \tag{30}$$

A few things can be inferred from (30). First, the added gate capacitance must be progressively smaller up the stack to facilitate larger voltage swing. Second, the swing can be controlled to maintain a minimum instantaneous $v_{DS}(t)$ across each transistor by using a slightly larger capacitance than would be required when $V_{DS,(n/p),min} = 0$ V. Finally, the output voltage swing is reduced if the gate capacitors are made larger (e.g. as would be the case for a typical cascode amplifier with *N*-1 common-gate stages). Note that as $V_{DS,max}$ nears the nominal V_{DD} of the technology, it is only possible to use (30) with $V_{DS,(n/p),min} = 0$ V since there will not be enough swing on the lower transistors in the stack to ensure the voltage swing on the transistor nearest the output is within the safe operating range.

This design methodology was applied to the 3-stack and 4-stack *n*-MOSFET cascodes and 3-stack CMOS cascode whose schematics are shown in Fig. 46. The measured S_{21} and MAG of the cascodes are shown in Fig. 47a up to 170 GHz for the *n*-MOSFET cascodes and up to 67 GHz for the CMOS cascode. The MAG of the 3- and 4-stack *n*-MOSFET cascodes, both larger than that of the CMOS cascode, are largely the same across frequency, with the exception that the unity Rollet stability factor frequency (indicated by the kink in the MAG curve) is higher in the 3-stack (155 GHz) compared to the 4-stack (145 GHz). This indicates that there is a limit to the number of MOSFETs which can be effectively stacked for operation at higher frequencies since the parasitic capacitance at internal nodes starts to reduce the gain even with some series inductors between stacked MOSFETs to cancel some of the capacitance. Fig. 47b shows that the 3-stack CMOS inverter cascode, which also has the largest transistor sizes, has the largest saturated output power, followed by the 4-stack *n*-MOSFET cascode, delivering nearly 20 dBm directly in a 50 Ω load without any matching network. The drain efficiency in Fig. 47c reveals that the CMOS cascode stack is most power efficient up to 10 GHz, but the higher f_T and f_{MAX} of the *n*-MOSFET compared to the *p*-MOSFET make the *n*-MOSFET cascodes more efficient above that frequency.

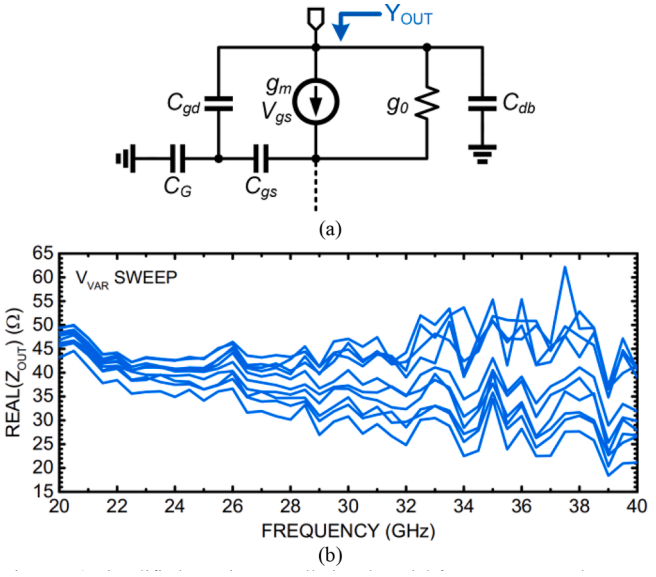


Fig. 50. a) Simplified transistor small-signal model for MOSFET at the output of a stacked cascode and b) measured output impedance of the 4-stack *n*-MOSFET cascode vs. varactor bias voltage [48].

For wireless applications, where the series-stacked cascode stage is used in the PA output stage to drive an antenna, the load impedance can vary depending on the surrounding environment. In this scenario, the stacked cascode stage drives a variable load and the top gate capacitor can be replaced by a varactor to enable voltage tuning of the PA output resistance to reduce reflections. Using the small-signal circuit model in Fig. 50a for the *n*-MOSFET at the output of a cascode stage, it can be shown that the output admittance is given by [48]:

$$Y_{OUT} = g_0\frac{C_{Gn,N}}{C_{Gn,N} + C_{gdn,N}} + j\omega\left(C_{gdn,N} + C_{dbn,N}\right) \tag{31}$$

The top *n*-MOSFET in the *n*-MOSFET cascodes uses a varactor as its added gate capacitance for this reason. The measurements in Fig. 50b show that the output resistance can be tuned between 30 and 46 Ω at 28 GHz, and from 27 to 53 Ω at 38 GHz while the output susceptance remains constant.

The 3-stack *n*-MOSFET cascode was modified and used in the design of the class A D-band power amplifier in the 151 – 160 GHz sensor shown in Fig. 3 [14]. The PA schematic, shown in Fig. 51, is composed of the 3-stack *n*-MOSFET cascode with transformer-coupled connection at the output and a ~ 1.5× smaller pre-driver 3-stack cascode used to increase the gain. Fig. 52a and b show the PA has 11 dB peak gain and 9 dBm saturated output power at a nominal V_{DD} of 2.4 V ($V_{DS,max} = 0.8$ V) and is well matched at the output from 150 to 170 GHz with better than −10 dB return loss. The gain and saturated output power increase to 12 dB and 11 dBm respectively when the V_{DD} is increased to 3.2 V ($V_{DS,max}$ ~= 1.1 V) with no change in output matching. While 0.8 V is the nominal V_{DD} in the technology, PAs which can sustain $V_{DS,max} = 1.2$ V while passing stress-testing with different loads have been reported in this technology [43]. The PA output compression point was measured from room temperature up to 125 °C. Fig. 52c shows that the measured gain and saturated output power reduce by approximately 2 dB and 1 dB, respectively, for every 25 °C increase in ambient temperature. The temperatures used in simulations to match measurement are shown in the legend of Fig. 52c.

The back gate voltage can also act as a tuning knob in variable gain amplifiers without adding any parasitic capacitance on the signal path. Such an example is provided by the LNA in the receivers of the D-band sensor of Fig. 3 and whose schematic is shown in Fig. 53. It features 3 cascode stages whose gain is tuned from 12 dB to 20 dB from V_{BG2} while S_{11} remains better than −15 dB over most of the D-band as depicted in Fig. 54a [14]. The gain peaks at $V_{BG2} = 2.5$ V, when the transistors in the LNA are biased at 0.25 mA/μm and the saturated output power is 5 dBm, Fig. 54b. The simulated LNA noise figure (black dotted lines in Fig. 54a) in the 9.5–10 dB range, is about 0.5–1 dB larger than the measured

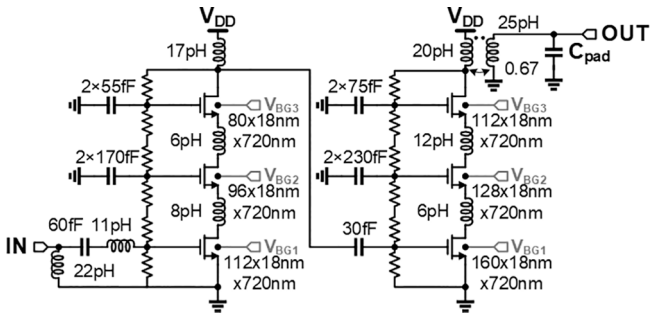


Fig. 51. Schematic of D-band PA [14].

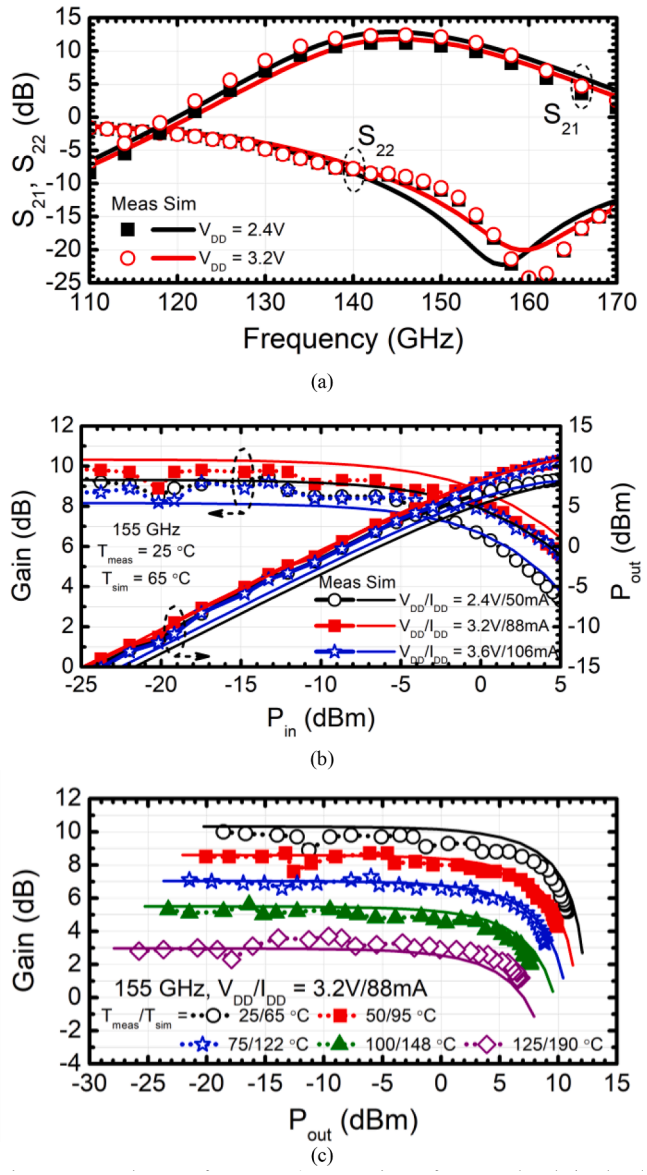


Fig. 52. D-Band PA performance. a) Comparison of measured and simulated S_{21} and S_{22} at nominal (2.4 V) and overdrive (3.2 V) V_{DD} bias at 25 °C. b) Comparison of measured and simulated gain and output power at 155 GHz for different V_{DD} biases at 25 °C. c) Measured gain vs. output power at 155 GHz at different ambient temperatures (T_{meas}) compared to the simulated junction temperature (T_{sim}) required to match the measurements.

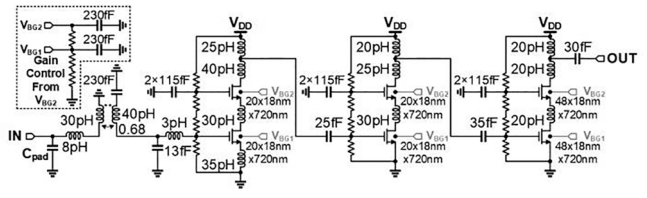


Fig. 53. Schematics of D-band LNA [14].

single-sideband noise figure of the entire receiver chain in the D-band sensor.

The previously discussed stacked cascode amplifiers were all operated in class A or class AB. Class D switching versions can be useful for implementing the large-swing DAC in the fibreoptic system of Fig. 1. The pseudo-differential 3-stack cascode CMOS DAC output stage in Fig. 55

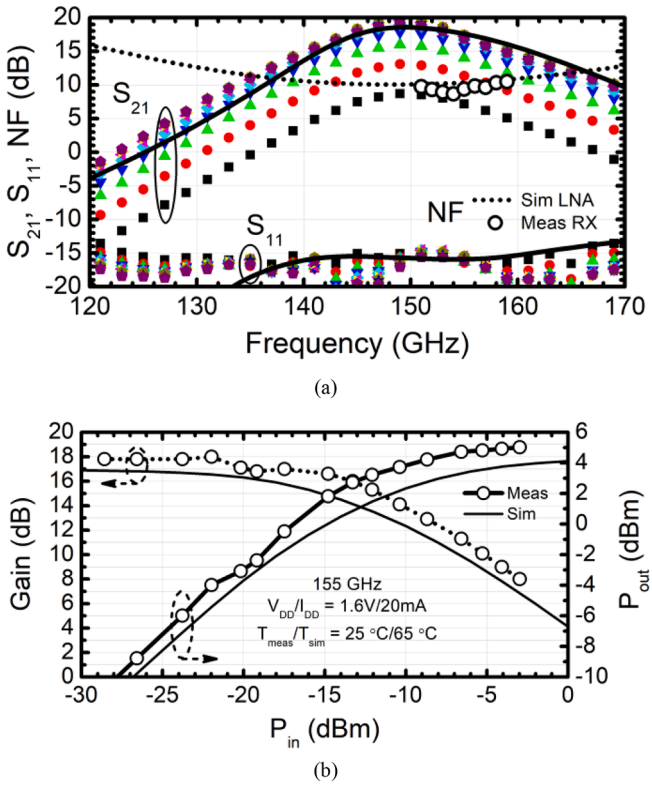


Fig. 54. D-Band LNA performance. a) Comparison of measured and simulated S_{21}, S_{11}, and NF at $V_{DD} = 1.6$ V for different $V_{BG2} = -0.5$ V to 4 V bias at 25 °C. b) Comparison of measured and simulated gain and output power at 155 GHz for different V_{DD} biases at 25 °C.

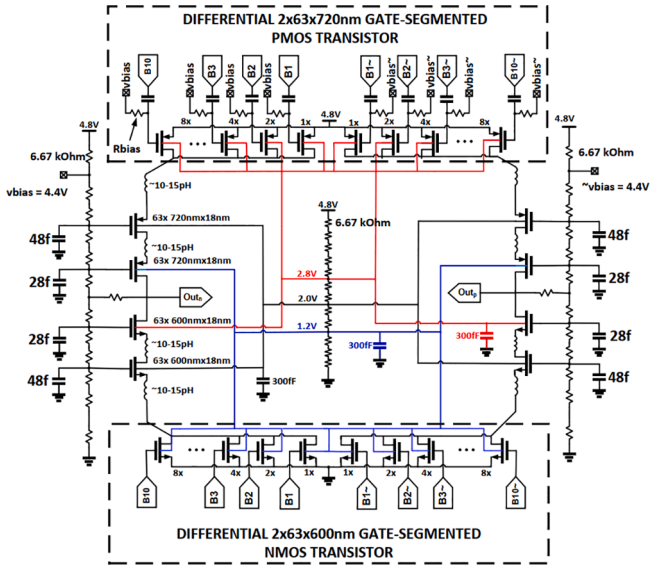


Fig. 55. Schematic of 6-bit large-swing DAC output stage. The 6-bit complementary data is encoded using 3 binary-weighted LSBs and 7 thermometer-coded MSBs.

was designed for maximum voltage swing ($V_{DS,min} = 0$ V) using the previously described methodology to drive either 50-Ω or capacitive loads, representative of Si photonics optical modulators [6]. The common-source *n*- and *p*-MOSFET gate fingers were segmented and grouped to form the 3 thermometer-coded MSBs and 3 binary weighted LSBs of a 6-bit large swing DAC. The first LSB has $N_f = 1$, the second LSB has $N_f = 2$, etc. while the thermometer coded MSBs feature 8 gate fingers

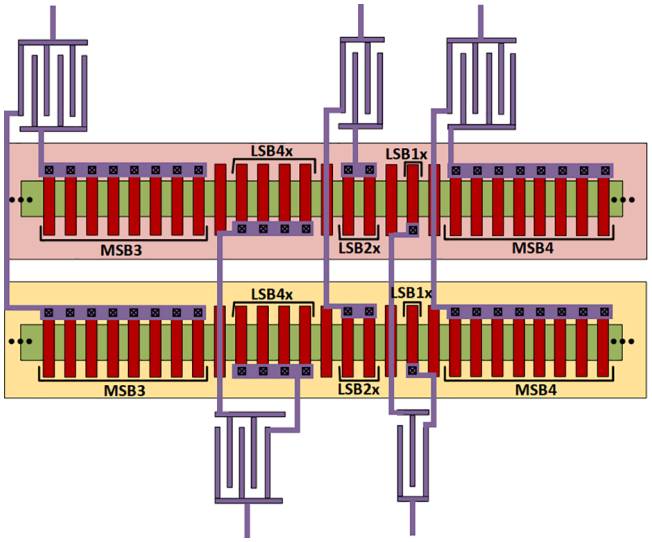


Fig. 56. Layout of single-ended gate-connections to input gate-segmented *p*-MOSFET (top) and *n*-MOSFET (bottom) transistors.

each. The segmented *n*-MOSFETs are driven directly by CMOS inverters, but a series capacitor must be placed between the CMOS inverter and segmented *p*-MOSFET gates for level shifting and to enable proper DC biasing. Fig. 56 illustrates how custom MOM capacitors can be combined with the common-source *n*- and *p*-MOSFETs in a compact layout. The series capacitors are scaled according to the size of the *p*-MOSFET gate they must drive to ensure that the low-frequency cut-off of the data paths to the DAC output stage is below 100 MHz. This passive level-shifting scheme consumes no power and does not require capacitive decoupling of intermediate level power supplies.

Simulations of the DAC integral and differential non-linearity (INL and DNL) were conducted for 2-, 3-, and 4-stack CMOS cascode output stages, each designed with maximum output swing of at least $4V_{ppd}$ (i.e. $V_{DS,min} = 0$ V) in order to determine the optimal number of transistors in the CMOS inverter stack. Fig. 57a shows the linear ramp response of the

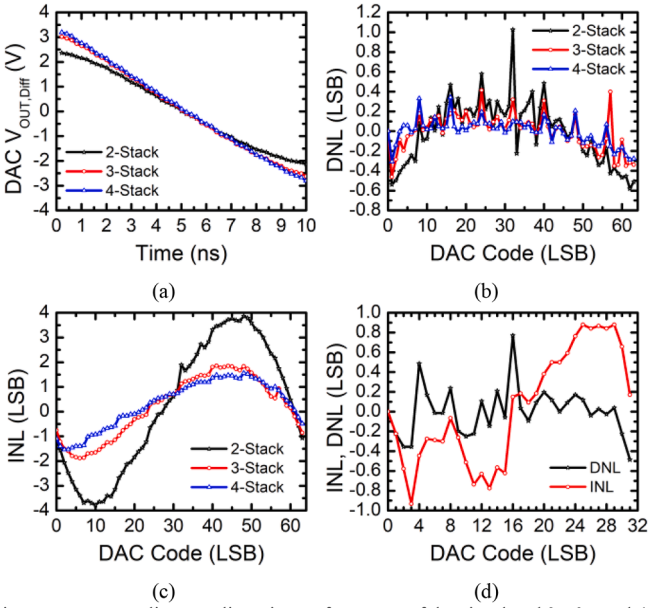


Fig. 57. Low sampling rate linearity performance of the simulated 2-, 3-, and 4-stack CMOS cascodes showing a) 6-bit linear ramp response, b) 6-bit DNL, and c) 6-bit INL. d) Measured 5-bit INL and DNL of the 3-stack CMOS cascode DAC at 2.35 V_{pp} output swing per side and 2.7 GS/s using the most significant bits.

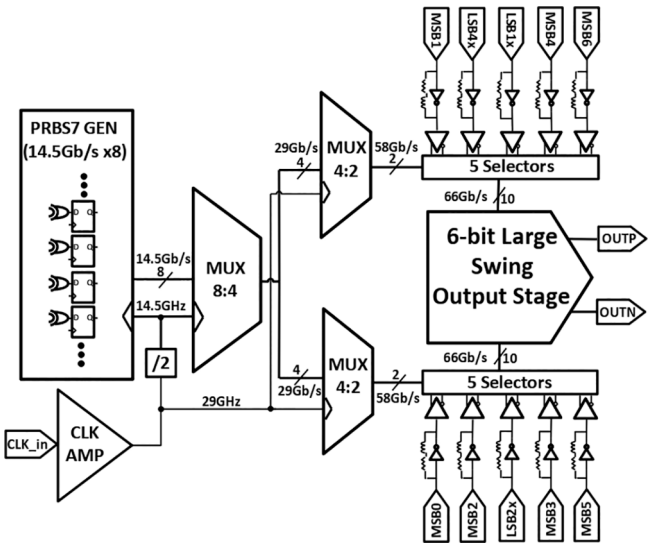


Fig. 58. Block diagram of fibreoptic transmitter front-end including large swing DAC output stage, on-chip PRBS7 pattern generator with two levels of multiplexors to serialize the pattern to higher speeds, and selectors to switch the DAC input between the serialized PRBS7 pattern and a pattern provided from off-chip [6].

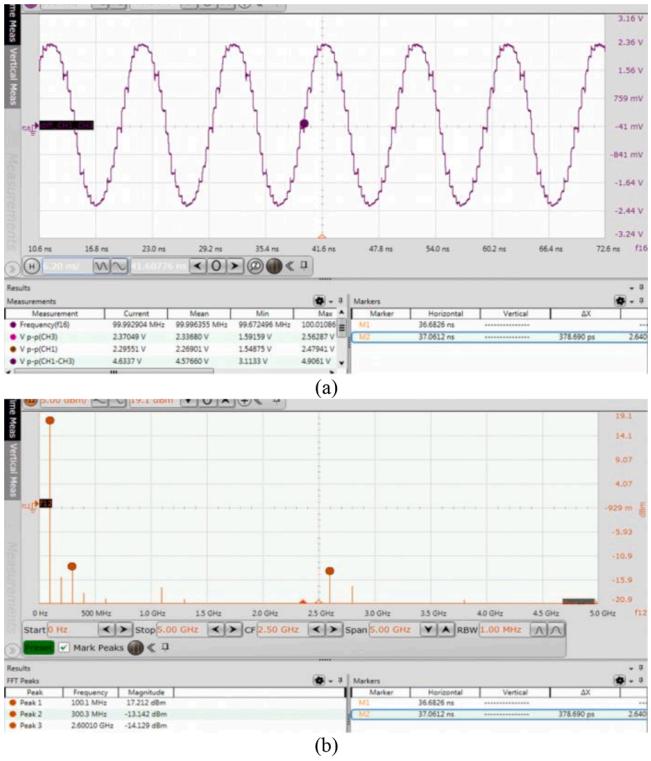
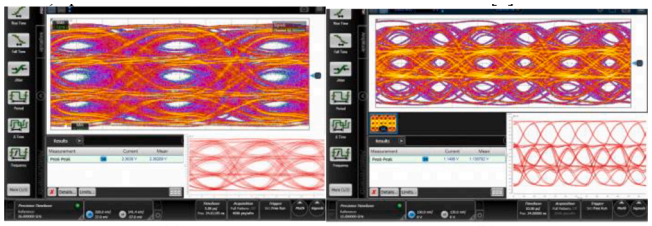


Fig. 59. Measured DAC performance for a 4.6-V_{pp} differential, 100-MHz sinusoid synthesized with all 6 bits switching at 2.7 GS/s showing a) transient and b) spectrum with SFDR = 30 dB and SNDR = 25.6 dB [6].

differential output stage for the 2-, 3-, and 4-stack CMOS cascodes to a full swing 10-ns input ramp. As expected, the output swing increases with the number of transistors in the stack. Fig. 57b and 57c compare the simulated DNL and INL between the different CMOS stacked cascodes vs. input code, showing a major improvement in linearity between the 2- and 3-stack cascodes but only a marginal improvement between the 3- and 4-stack cascodes. Since the required V_{DD} (and therefore the power



(a) (b)

Fig. 60. Measured vs. simulated (inset at bottom right) eye diagrams output from the DAC showing a) 52-GBaud 2.3 V_{pp} per side PAM-4 using on-die PRBS 2^7-1 generator and b) 60-GBaud 1.14 V_{pp} per side PAM-4 PRBS 2^7-1 pattern created using three external data lanes (i.e. two running at 60 Gb/s and one at 30 Gb/s) driving 3 MSB DAC cells [6].

consumption) is linearly proportional to the number of devices in the stack, it was determined that the 3-stack cascode offered the best trade-off between N_f power consumption and linearity for the 3 – 5 V_{ppd} output voltage swing required to drive MZMs [49].

To facilitate testing, the DAC output stage was integrated with an on-die PRBS generator, 10 broadband 50-Ω input matched data lanes and selectors to choose between external 60-Gb/s bit streams and the on-die PRBS generator (block diagram in Fig. 58). All circuit blocks operate in switching mode and use conventional CMOS logic at over 60 Gb/s. In measurement, the available pattern generators to test the low frequency linearity were too slow for the high-pass corner frequency of the *p*-MOSFET series capacitors (measured at less than 100 MHz) so only the 5-bit linearity using the most significant bits was tested at 2.7 GS/s with 2.35 V_{pp} per side output swing. This measurement in Fig. 57d showed that the 5-bit INL and DNL are better than 1 LSB and 0.8 LSB respectively. The full 6-bit DAC resolution is demonstrated in the generation of a 4.6 Vpp differential sinusoid at 100 MHz (Fig. 59a) with SFDR and SNDR of 30 dB and 25.6 dB (Fig. 59b), respectively. Among other eye diagrams reported in [6], the large-swing 6-bit DAC was able to generate PAM-4 eyes at 52-GBaud and 2.3 V_{pp} per side swing using the on-die PRBS 2^7-1 (Fig. 60a) and 60-GBaud 1.14 V_{pp} per side swing using an external PRBS 2^7-1 generator from off-chip driving only 3 MSB DAC cells (Fig. 60b). In the latter case, the output swing is limited by the fact that only 3 synchronized external 60-Gb/s bit streams were available to drive 3 of the 7 thermometer coded MSB cells while the other 4 MSB cells and all 3 binary cells are idle.

4. Conclusion

In this paper we have reviewed the measured dc and high frequency characteristics and the analog mixed-signal FoMs of production 22-nm FDSOI CMOS technology over a wide temperature range from 2 K to 400 K. Many of the measurement results presented are new and demonstrate that all device and circuit FoMs improve at cryogenic temperatures compared to room temperature. Importantly, minimum size MOSFETs exhibit Coulomb Blockade signatures and QD behaviour at cryogenic temperatures up to 50 K, stronger in *p*-MOSFETs than in *n*-MOSFETs, indicating that FDSOI can become an ideal platform to integrate semiconductor spin qubits with control and readout electronics on the same die.

In the second part of the paper we have demonstrated how the back gate terminal and the buried oxide features of FDSOI technology can be harnessed, along with the invariance of the characteristic peak g_m, peak f_T, peak f_{MAX} and minimum noise figure current densities over the entire range of temperatures, in the design of record performance circuits for applications ranging from mm-wave radar and radio, to fibreoptic transceivers and cryogenic quantum computing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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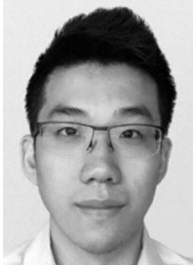

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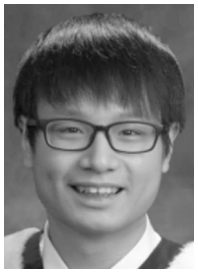

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