Design of a 55-nm SiGe BiCMOS 5-bit Time-Interleaved Flash ADC for 64-Gbd 16-QAM Fiberoptics Applications

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***Abstract*— We present the architectural, circuit topology, transistor-level schematics, and layout design considerations for the highest sampling-rate single-chip ADC reported to date in any semiconductor technology. The circuit uses a 2× time-interleaved architecture integrating two track-and-hold amplifiers, each driving a 5-bit flash sub-ADC sampled at 64 GHz in antiphase. For testing purposes, the chip also incorporates a time-interleaved 128-GS/s thermometer-coded 5-bit current steering DAC. The performance of the ADC-DAC combo, including the SFDR and the effective number of bits of 4 bits up to 32-GHz input signals, was characterized on die and includes the impact of the DAC. The power consumption and layout footprint of the ADC, critical for operation at 128 GS/s, were minimized by employing novel 1-mA Cherry-Hooper comparators and quasi-current-mode logic MOS-HBT latches with active peaking, which reduced the footprint of each of the 64 ADC-lanes to 10 μm × 70 μm. The total power consumption of the ADC is 1.25 W and the total die area of the ADC-DAC chip is 1.1 mm × 1.9 mm.**

***Index Terms*— Active inductor, comparator, current steering DAC, flash ADC, latch, quasi-current-mode logic (CML), segmented linear buffer, SiGe BiCMOS, time interleaving, track-and-hold amplifier.**

I. Introduction

THE block diagram of a state-of-the-art dual polarization fiber-optic system with 16-QAM modulation at symbol rates of 56–64 Gbd is shown in Fig. 1. It is partitioned in the following:

1) an electro-optical front end consisting of SiGe BiCMOS linear drivers, III–V laser, and III–V or silicon photonics optical modulators in the transmitter, and InGaAs or Ge photodiodes, SiGe BiCMOS linear transimpedance, and variable gain amplifiers in the receiver;
2) a CMOS analog-mixed signal block with four DACs in the transmitter and four ADCs in the receiver;
3) a DSP engine for equalization, and error correction.

Because of its complexity, power consumption, and digital nature, the latter is manufactured in the most aggressively scaled FinFET CMOS technology. This system partition is dictated by performance, power consumption, ease of interfacing between chips, and the need to avoid heating of the sensitive optical components by the electronic chips. Because of its large power consumption, the DSP engine cannot be integrated in or placed near the electro-optical front end. At the same time, the demanding low-noise, linearity, and bandwidth requirements of the electro-optical front end rule out its integration in FinFET technology. As in wireless transceivers, a single, high-bandwidth, analog signal interface between chips is preferred to a wide, multi-lane digital bus with an aggregate data rate of 400 Gb/s and, soon, 1 Tb/s. In the last few generations of fiber-optic systems, starting with the 65-nm CMOS node [2], this has naturally lead to the monolithic integration of the DACs with the transmitter DSP and of the ADCs with the receiver DSP, using the most advanced CMOS technology. Highly parallelized SAR

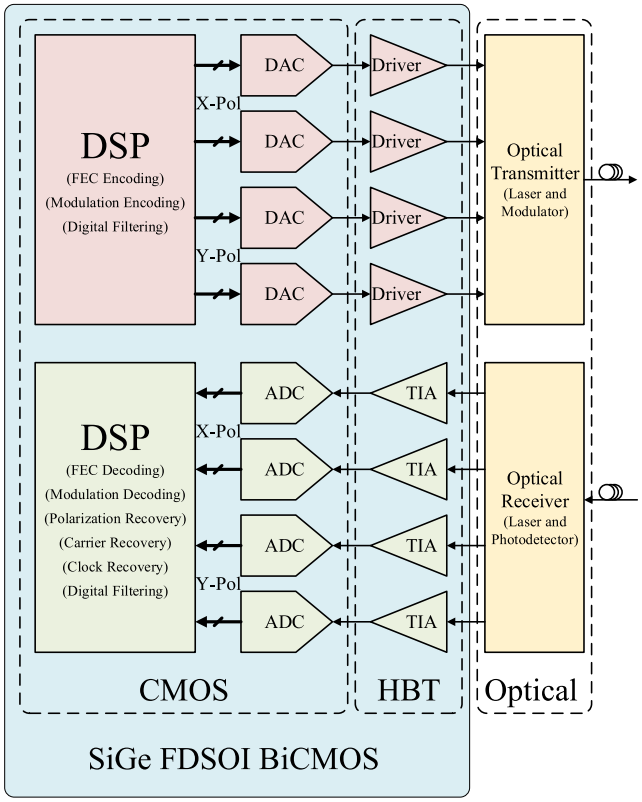

Fig. 1. Block diagram of a dual-polarization fiber-optic system with 16-QAM or higher order modulation.

Manuscript received January 14, 2019; revised March 30, 2019; accepted April 30, 2019. Date of publication June 11, 2019; date of current version August 23, 2019. This paper was approved by Guest Editor Shahriar Shahramian. This work was supported by MITACS and Ciena Corporation. *(Corresponding author: Alireza Zandieh.)*

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Digital Object Identifier 10.1109/JSSC.2019.2917155

architectures have been favored in the ADC because of the low power consumption and small layout footprint facilitated by the continued shrinkage of the minimum feature size of MOSFETs. The power consumption and layout overhead needed to calibrate and compensate for the gain and timing skew mismatch between the large number of ADC lanes have increasingly been transferred to the DSP engine whose layout size and power consumption greatly benefit from continued MOSFET feature size scaling.

Unfortunately, the large analog signal bandwidth of at least 32 GHz for 64-Gbd systems and 50 GHz for 96-Gbd systems has proven a challenge even in 14-nm FinFET technology [3], which, despite the high SNDR that has been achieved, has not exceeded 26.5 GHz [4]. Like 14-nm FinFETs [5], despite higher g_m, intrinsic voltage gain, and maximum stable gain (MSG) [6], 7-nm FinFETs suffer from poor f_{MAX} and large parasitic metal capacitance and resistance [7], which limit the ADC bandwidth [3], [4], [8].

Unlike FinFET, SiGe HBT noise and analog-mixed-signal circuit performance continue to improve with scaling [9], [10]. Because of their low noise, better high-frequency performance, and reduced device mismatch compared to MOSFETs, using SiGe-HBT-friendly architectures and circuit topologies in the ADC relaxes the complexity of the DSP engine. However, because of the larger supply voltage requirements and the use of current-mode-logic (CML), ADCs based on SiGe HBTs have suffered from much larger power consumption than their CMOS counterparts. It is hoped that by adapting the ADC architecture to take advantage of the best features of SiGe HBTs in a BiCMOS technology with aggressively scaled MOSFETs and by combining it with a simpler analog equalizer, potentially a fiber-optic receiver with lower overall power consumption can be achieved. Since even the intrinsic g_m and f_T of FinFETs and FDSOI MOSFETs are predicted to saturate and degrade due to surface scattering at physical gate lengths below 10 nm [10], HBT-based ADCs may become a viable option for future generations of fiber-optic systems operating at symbol rates beyond 128 Gbd.

Toward that end, in this paper, we investigate and demonstrate a time-interleaved 5-bit flash ADC architecture in 55-nm SiGe BiCMOS technology which takes advantage of the strengths of the SiGe HBT (larger bandwidth and lower thermal noise than the most advanced FinFETs) and of novel minimum-power SiGe HBT and MOS-HBT topologies to achieve the highest bandwidth and sampling-rate ADC in silicon with better energy-per-bit than all previously reported SiGe BiCMOS ADCs. This paper, which is an expansion of [11], is organized as follows. Section II discusses the strengths and limitations of the chosen 55-nm SiGe BiCMOS technology and how these dictate the ADC architecture and circuit topology choices. The transistor-level design of the ADC is covered in Section III, with the detailed experimental results and comparison with other state-of-the-art CMOS and SiGe BiCMOS high sampling-rate ADCs being described in Section IV. Finally, Section V looks ahead at the scaling prospects of the ADC in the future SiGe BiCMOS technology generations for higher symbol rate fiber-optic systems beyond 128 Gbd.

II. ADC Architecture and SiGe BiCMOS Circuit Topology Options

The most intriguing question is whether a hypothetical SiGe BiCMOS technology [12] featuring 22-nm or 7-nm FDSOI MOSFETs would lead to different ADC architectures with higher bandwidth and lower power consumption than would otherwise be possible in an FDSOI CMOS process alone [13] or in a 55-nm SiGe BiCMOS technology with identical SiGe HBT performance. At the very least, adding a fast SiGe HBT to a 7-nm CMOS platform allows for lower noise, higher bandwidth, linear input signal distribution, and low-phase noise clock distribution networks. This alone can improve the highest achievable resolution of a given ADC by at least one bit. For example, a clock path jitter of 100 fs_{rms} limits the maximum achievable SNR for 32-GHz and 48-GHz sinusoidal input signals to $-20\log_{10}(2\pi f_{\mathrm{in}} \times \mathrm{jitter}) =$ 34 and 30.4 dB, respectively, which renders ADC architectures with more than 7 bits of resolution ineffective, unless rms jitter is reduced below 50 $\mathrm{fs}_{\mathrm{rms}}$. However, a typical fiber-optic system works with Gaussian signals with less than half rms power compared to sinusoidal signals; therefore, the clock jitter would not limit the SNR to 5 bits of resolution at 32 GHz. Nevertheless, the SNDR of the highest reported resolution bandwidth FinFET ADC is limited by clock jitter [4].

The 55-nm SiGe BiCMOS process used in this paper features SiGe HBTs with 330- and 370-GHz f_T and f_{MAX}, respectively [14], and 55-nm planar bulk n-MOSFETs with f_{MAX} of 300 GHz. These values for SiGe HBTs, comparable to those reported for the most advanced FinFET and FDSOI MOSFETs after removing parasitics down to metal 1, correspond to fully wired transistors, up to the top metal, and therefore reflect the true circuit performance. Quasi-CML 55-nm nMOSFET latches with inductive peaking have been demonstrated at clock frequencies as high as 80 GHz using 1.2-V supplies and 4-mA tail currents [15]. However, the 55-nm planar pMOSFET is significantly slower than those available in 22-nm FDSOI or 7-nm FinFET technologies, limiting the use of fan-out-of-2 CMOS logic gates to clock frequencies of 20 GHz or less. For comparison, 22-nm FDSOI fan-out-of-2 CMOS inverter chains operating off 0.8-V supply at up to 50-GHz clock frequencies have been reported [13].

These practical, technology-related considerations point to an ADC architecture which takes advantage of the fast HBT CML and MOS-HBT quasi-CML gates capable of operation with sampling clocks beyond 100 GHz [16], [17]. However, to save power and to minimize the layout footprint, only circuits with the minimum feature size HBT and without inductors must be used. The chosen minimum value of the tail current of the CML circuits, 1 mA, was dictated by the requirement that the fan-out-of-2 CML gates operate at clock frequencies, 65 GHz in this case, much higher than the fastest reported for CMOS logic in any technology [13].

Both SAR and flash ADC architectures come in contention to realize 5- or 6-bit ADCs in the chosen 55-nm SiGe BiCMOS technology, resulting in similar numbers of latches, comparators, and buffers for clock and input signal distribution. However, given the same set of comparators and latches, the delay around the comparator-SAR-DAC loop limits the

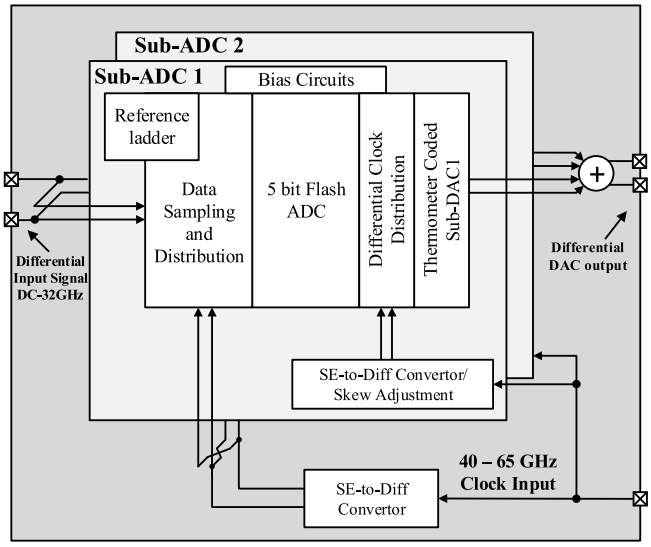


Fig. 2. ADC block diagram.

clock frequency of the comparator latch to lower values than those in the flash-ADC comparator latch. Therefore, all other things being equal, the overall sampling rate of the SAR ADC will be lower, unless the number of time-interleaved sub-ADCs is doubled, than that of the flash ADC.

A 2× time-interleaved 5-bit, rather than a 6-bit, flash architecture with a total of 64 latched comparators was chosen as a test vehicle because of its simplicity and layout footprint. With the same set of latches and comparators, and a quadrature 25% duty-cycle clock generator [17], it also allows 4× time-interleaving to 200 GS/s which corresponds to over 2 oversampling for 96-Gbd applications using the same technology. Increasing the resolution to 6 bits provides extra performance margin for other impairments, but must be accompanied by a doubling of the ADC input full-scale range and increased power consumption if the thermal noise of the analog front end of the ADC is to remain the same as in a 5-bit version. The 2× time-interleaving enables a higher oversampling ratio than the minimum required to digitize the 32-GHz bandwidth and thus partially compensates for the lower nominal resolution. It should be emphasized that the effective number of bits (ENOB) of the high-speed SAR ADCs reported to date is typically 2–3 bits lower at Nyquist than the nominal resolution [2]–[4], [18].

III. ADC Design

The block diagram of the ADC-DAC chip is shown in Fig. 2. Time-interleaving of two 5-bit flash sub-ADCs is employed to double the sampling rate. This scheme maximizes the bandwidth of the data path, minimizes power consumption, and requires a relatively simple and low-power 65-GHz clock distribution network. The digital outputs of the 32 lanes of one sub-ADC act as the thermometer-coded data inputs for each half of a 2× time-interleaved 128-GS/s 5-bit current-steering DAC also integrated on the ADC die. The DAC eliminates the need for an on-chip memory to store the digital outputs and test the ADC, but makes it difficult to resolve its performance from that of the DAC and to post-process the digital outputs of

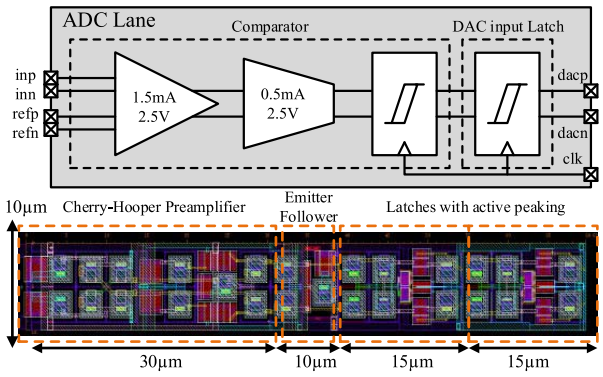


Fig. 3. Latched comparator lane schematic and layout.

the ADC for calibration, should that be necessary. The external single-ended clock signal is applied between the differential DAC outputs and is converted on-chip to differential format and distributed to the two sub-ADCs and the DAC. Two delay tuning cells are added on the clock path of each sub-ADC to ensure the correct input signal sampling by all sub-ADC comparators over process variation. However, both delay cells are controlled by the same external current; therefore, the delay setting is global and is not adjusted per comparator lane or per sub-ADC.

The full scale at the input of the ADC was set to 300 mV_{pp} per side to match the output voltage range of the TIA-VGA in the electro-optical module. Thus, the value of the LSB is 9.4 mV_{pp} per side and 18.8-mV_{pp} differential.

A. Lane Implementation

The schematic and layout implementation of the latched comparator lanes in each flash sub-ADC dictate the overall performance of the entire ADC and the design solution for the input analog signal distribution and clock signal distribution networks. The latched comparator lanes were designed to switch at the highest possible clock frequency using the minimum size HBTs available in the technology and whose performance is not limited by emitter periphery effects. This dictates an HBT emitter length of 1 μm and a tail current of 1 mA in the latch cells. Although the minimum HBT size available in the technology is 0.35 μm, it shows worse performance at all currents than the 1-μm HBT. The larger size also improves the matching and noise performance of the comparator.

At 1-mA tail current, classic inductive peaking cannot be applied because the corresponding inductors would occupy prohibitively large area and would exhibit a self-resonance frequency lower than 100 GHz. Therefore, new, low-power high-speed circuits with minimum layout footprint had to be designed, as shown in Fig. 3, where the width of each of the 64 comparator lanes is only 10 μm, as in a 28-nm FDSOI CMOS 10-GS/s SAR ADC [19]. To improve the speed and gain of the comparator, a preamplifier is placed before the latch. In the absence of inductive peaking, a Cherry-Hooper topology with emitter-followers (EFs) in the feedback loop is employed in the preamplifier [20], as shown in Fig. 4(a). The stage consumes 1.5 mA from 2.5-V supply. The output

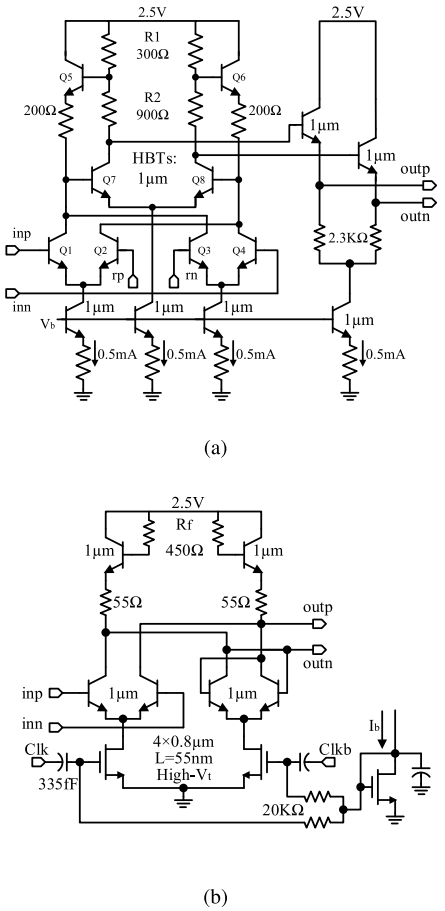


Fig. 4. Schematic of building blocks in ADC comparator lanes. (a) Cherry-Hooper preamplifier followed by EF stage. (b) Quasi-CML latch with active peaking.

voltage swing and gain are dictated by the amount of necessary peaking and also by the required voltage drop on the load resistor (R_2) to avoid breakdown of the HBTs in the feedback path. The Cherry-Hooper stage is followed by the 0.5-mA EF stage needed for dc level shifting.

The new, compact, high-speed, and low-power latch, shown in Fig. 4(b), features a quasi-CML MOS-HBT topology with an HBT-based active inductor [21] for broadbanding. The active inductor results in a higher inductance, which occupies a smaller layout area and exhibits a higher self-resonance frequency (SRF) compared to conventional passive inductors. It also eliminates magnetic coupling between adjacent sub-ADC lanes. The inductance and SRF of the HBT active inductor can be obtained from the following expressions:

$$L = -\frac{C_{\text{be}}}{g_m}\left(R_f - \frac{1}{g_m}\right) \approx \tau_F R_f \left(R_f \gg \frac{1}{g_m},\, J_c \approx J_{pfT},\, J_{\text{pfMAX}}\right) \quad (1)$$

$$\text{SRF} = \frac{\sqrt{R_f g_m - 1}}{2\pi R_f C_{bc}} \quad (2)$$

where τ_F is the total transit time of the HBT, approximately 0.2 ps in this technology. C_{be}, C_{bc}, R_f, and g_m are the base–emitter capacitance, base–collector capacitance, feedback resistance, and the HBT transconductance, respectively.

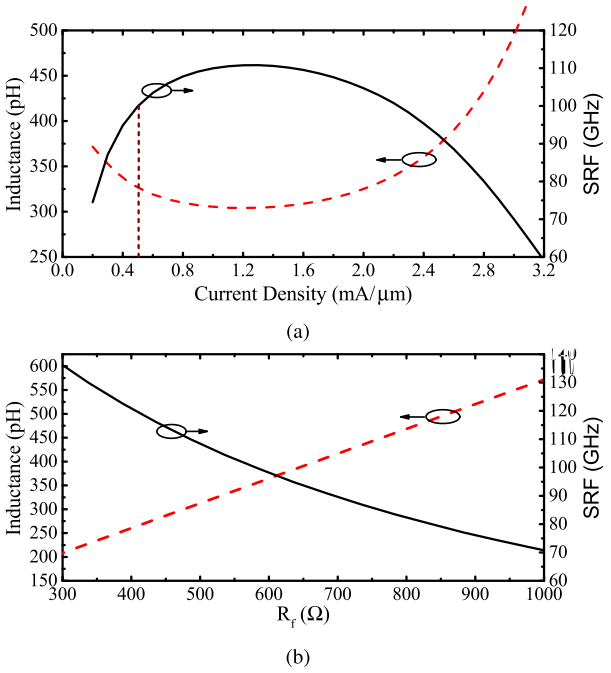


Fig. 5. Simulation of the active inductor design space: inductance and self-resonance frequency as a function of (a) HBT current density per emitter width and (b) peaking resistor value, R_f.

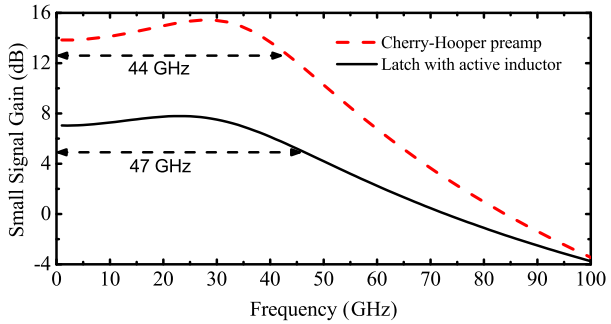


Fig. 6. Small-signal simulation of the preamplifier and comparator latch bandwidths.

As these equations suggest, when the transistor is biased at current densities close to J_{pfT}, the inductance is linearly proportional to the feedback resistor. Also, there exists a range of HBT bias current density values at which the SRF of the active inductor is maximized. The simulation results for inductance and SRF versus current density and feedback resistor values are reproduced in Fig. 5(a) and (b), respectively. In the proposed latch, the active-inductor HBT is biased at the minimum possible current density at which the SRF is not degraded by more than 10% from its peak value. To maximize the bandwidth and switching speed, the load resistor in the latch is sized for a CML voltage swing of 250 mV_{pp} per side. The simulated small signal gain and bandwidth of the preamplifier and latch are shown in Fig. 6. The preamplifier achieves 15-dB gain with over 45-GHz bandwidth and the latch provides 7-dB gain in the track mode with over 47-GHz bandwidth. The large gain of the preamplifier also reduces the differential input referred noise of the comparator to 1mV_{rms},

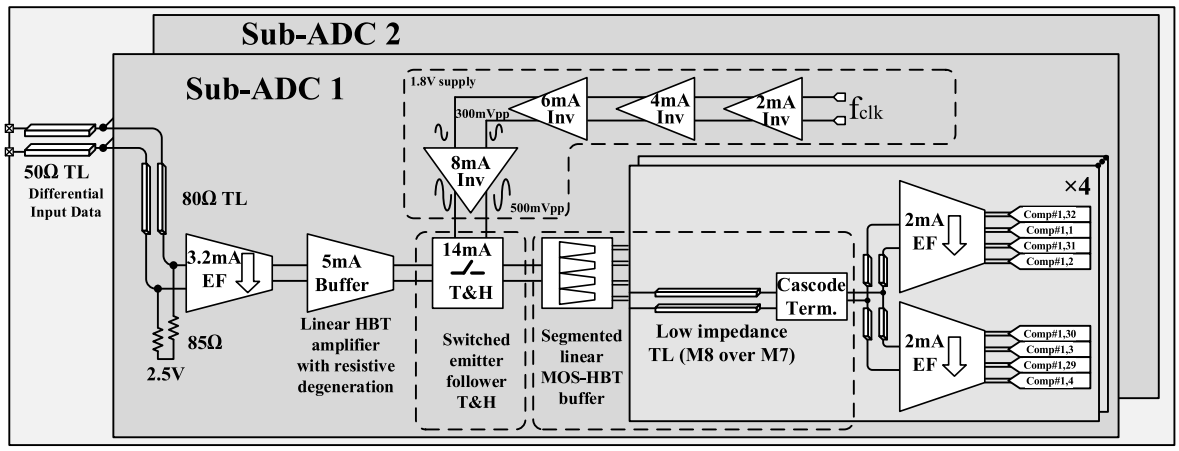


Fig. 7. Block diagram of the analog input signal sampling and distribution network in each sub-ADC.

which is significantly less than the differential LSB/$\sqrt{12} \approx$ 5.4 mV_{pp}.

As a result, the entire sub-ADC latched comparator lane with two cascaded latches can switch at up to 70 GHz while consuming 10 mW and is only 10-μm wide. The small lane width is critical for reducing the length and power consumption of the input analog signal and clock distribution paths.

The differential reference resistor ladder in each sub-ADC and the differential comparator connections to it follow the approach first proposed in [22]. Due to the large resistor size needed for good matching, the reference resistor ladder is placed relatively far from the sub-ADC lanes. The dc reference voltages are provided to each comparator using capacitive lower level metal lines with a surrounding ground shield. Additionally, to avoid any voltage drop on the interconnect due to the HBT base currents, the dc current through the resistors in the ladder is set to 5 mA and, as shown in [22], the differential sampled signal inputs to comparators in adjacent sub-ADC lanes have opposite sign, with identical differential reference voltage connection to cancel the dynamic current and to prevent fluctuations of the reference voltages.

B. Analog Input Signal Sampling and Distribution Network

The block diagram of the linear, broadband, input signal sampling, and distribution network in each sub-ADC is shown in Fig. 7. It operates from a supply of 2.5 V. To ensure high input bandwidth and good linearity, the differential analog input signal is applied directly to the two sub-ADCs in parallel through 80-Ω differential transmission lines terminated on 85-Ω resistors at the sub-ADC input, thus providing 40–45-Ω impedance at the input pad. Every circuit block was designed for a full-scale input signal of 300 mV_{pp} per side and a fan-out-of-2 load. The input buffer schematic is reproduced in Fig. 8(a). It employs a 3.2-mA EF stage followed by a 5-mA HBT differential pair with resistive degeneration. One of its roles is to reduce the input capacitance of the entire ADC and thus maximize its analog bandwidth. Another role is to improve the isolation between the two sub-ADCs, reducing

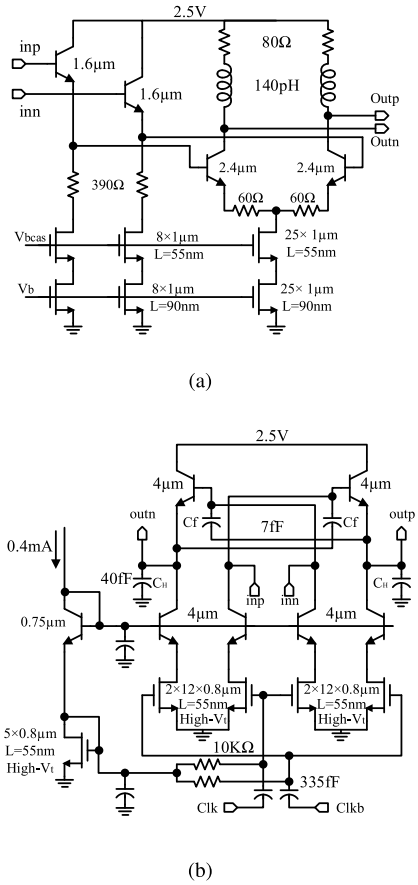


Fig. 8. Schematic of building blocks in signal sampling and distribution network. (a) Input buffer. (b) Track and hold amplifier.

the clock signal kick-back from the following track-and-hold amplifier (THA) stage. The latter, shown in Fig. 8(b), is based on [16] and uses the switched-EF topology, consuming 14 mA. The size and bias current of the differential HBT pair with resistive degeneration in the linear input buffer are designed to completely turn off the THA switched-EF stage during the HOLD phase. For best THA performance, the buffer fan-out should be larger than 2, but further increasing the fan-out reduces the bandwidth considerably.

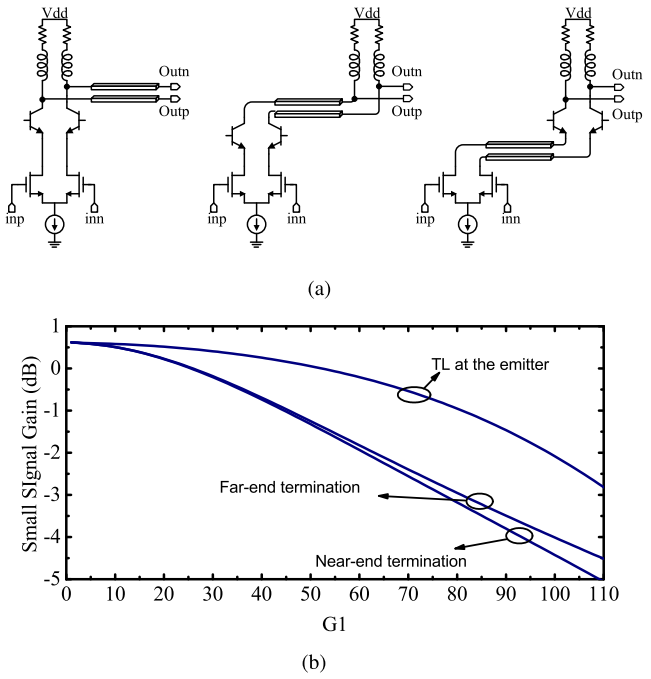


Fig. 9. Performance comparison for the different MOS-HBT buffer configurations. (a) Schematics. (b) Small-signal simulation.

Since 50% duty cycle clock signals are used, the clock is ac-coupled to the THA which allows for transistors in the quasi-CML switch to be biased in class AB with a current mirror. This improves the robustness of the quasi-CML switch to process and temperature variation. In addition, unlike a dc-coupled quasi-CML stage, the ac-coupled version is not sensitive to the dc voltage at the output of the clock buffer driving it. Therefore, the performance of the THA can be optimized by simply increasing the dc voltage drop on the load resistors in the preceding clock buffer and thus creating larger swing at the gates of the MOSFETs in the quasi-CML switch.

As described in [23], for the THA sampling function to be effective, the large signal bandwidth from the output of the THA to the input of each comparator in the 32 lanes of a sub-ADC must be larger than $0.8 \times f_{\text{clk}}$. This bandwidth, along with the linearity requirement, makes the design of the sampled analog input signal distribution network very challenging. In this paper, to keep the load capacitance small, minimum size comparators are employed. To minimize linearity degradation, only one buffer is placed between the THA and the 32 comparators. An MOS-HBT cascode buffer topology with the MOSFETs and HBTs biased at their respective peak-f_T current density results in high linearity and good bandwidth.

The interconnect can substantially reduce the bandwidth when the sampled analog signal must be distributed from the THA to so many sub-ADC lanes. The problem is compounded when the signal is distributed differentially over a large layout area as is the case here. To find the best solution, the interconnect lines were placed at different nodes in the MOS-HBT buffer and the simulated bandwidth in each case was compared. As shown in Fig. 9, when the long interconnect is inserted between the drain of the MOSFET

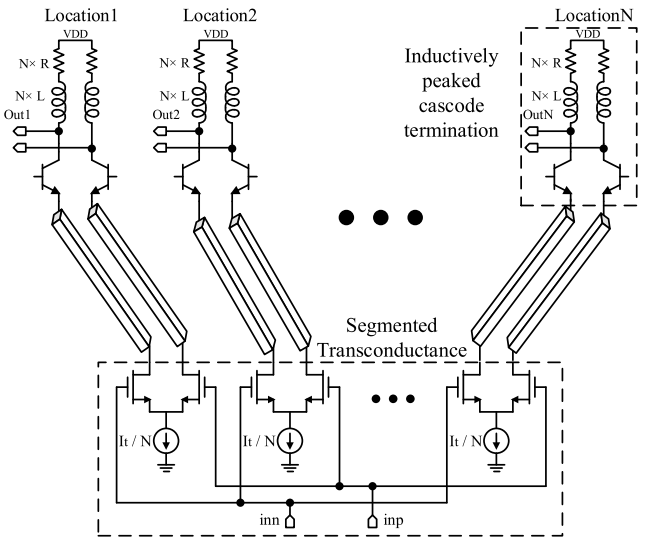


Fig. 10. Sampled analog input signal distribution buffer with segmented transconductance.

and the emitter of the HBT, its impact is minimized leading to significantly larger bandwidth. The resulting new sampled signal distribution buffer is shown in Fig. 10. It features a segmented MOSFET transconductor which distributes the sampled analog input signal in current form to many (4 in this case) equally spaced distant locations in the sub-ADC close to the latched-comparator lanes. It is very critical that the transconductor segments are very well matched. Any mismatch produces output spectrum spurs similar to those due to timing skew mismatch in the interleaver. To prevent unwanted peaking in the sampled input signal transfer function, the long interconnect lines at the outputs of the segmented transconductor should be capacitive rather than inductive. This is the opposite to the situation encountered in the traditional signal distribution solution where the interconnect lines must be as inductive as possible to improve the bandwidth. Therefore, the top two thick metals are used as signal and ground, respectively, to distribute the current. This arrangement allows for the lower metals to be allocated for shielded supply and bias current distribution and also improves the comparator and segmented transconductor matching by providing lower resistance and lower inductance ground and supply planes. The proposed buffer with four segments consumes 20 mA. Every segment drives two 2-mA EF stages, each loaded by four comparators with 1-mA tail current.

C. Clock Distribution Network

The block diagram of the clock distribution network is sketched in Fig. 11. Because of the sparse layout, it features passive rather than active inductive peaking. It converts the single-ended external clock signal to differential format at frequencies up to 65 GHz and then distributes it to the flip-flops in the sub-ADC comparators and also to the two THAs. The single-ended external clock signal is first applied to a 50-Ω microstrip line which is terminated on two 240-Ω input-impedance single-ended-to-differential converters, one for each sub-ADC, connected in parallel with a long

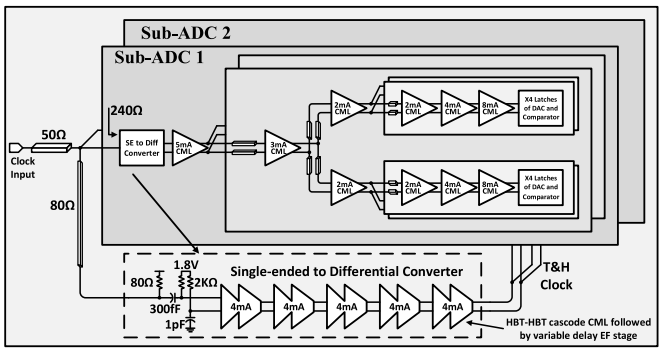


Fig. 11. Block diagram of the clock distribution network.

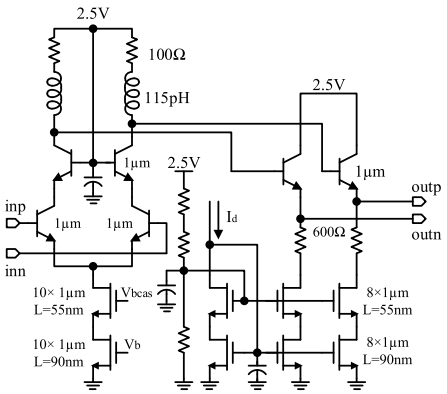


Fig. 12. Schematic of the cells in single-ended-to-differential converter. The current in the EF stage is varied externally to adjust the delay.

80-Ω microstrip line terminated on an 80-Ω input-impedance single-ended-to-differential converter at the far end. The clock signal is ac-coupled to the three single-ended-to-differential converters in order to reduce the power consumption, achieve good broadband input matching to 50 Ω, and also to match the common-mode dc voltage at the input of all three single-ended-to-differential converter blocks detailed in the inset and which are physically far from each other.

Unlike the rest of the clock distribution network which operates from a supply of 1.8 V, the single-ended-to-differential converter blocks require a 2.5-V supply and feature five cascaded identical differential amplifiers consisting of a 2-mA HBT-HBT cascode with 250-mV_{pp} swing and cascode tail current source, followed by an EF stage with variable bias current, as shown in Fig. 12. The five cascaded amplifiers provide enough gain and common-mode rejection up to 65 GHz. The variable-current EF stages provide adjustable delay between the clock signals arriving at the two THAs and those reaching the flip-flops in each of the 64 comparator lanes. Considering the fact that the THAs are significantly more sensitive to the clock jitter than the latched comparators (where the signal is held for half a clock period), the delay matching is achieved by changing the current only in the EF stages placed on the comparator clock path, while the bias current in the EF stages in THA path is kept constant. Delay adjustment by varying the current in the EF stage does not change the clock amplitude in the comparator latches. Only at very low EF currents, the amplitude drops slightly at the output of the single-ended-to-differential converter block, but it is later recovered to full swing by the following CML limiting buffers in the clock distribution network. The five-cascade EF stages provide a total of ∼3-ps delay adjustment. The clock delay is set such that the comparator decision is made only 2 ps before the end of the HOLD phase of the THA, irrespective of the sampling rate. Section IV describes how, at the highest sampling rate, this delay adjustment helps to push the decision at the very end of the HOLD phase and thus improves the bandwidth significantly by increasing the time available for the comparator to make a decision.

Following the single-ended-to-differential converter block, the differential clock signal is distributed using 1.8-V differential common-emitter HBT inverters with MOSFET cascode current sources with a fan-out of 2 or less than 2, where the interconnect is very long. The clock signal swing is 300 mV_{pp} up to the last clock amplifier stage in the chain where it is increased to 500 mV_{pp} per side to properly switch the MOSFETs in the quasi-CML latches.

The simulated large signal voltage transfer functions from the analog signal input of the ADC to different points along the analog signal sampling and distribution path up to the input of one of the 64 comparators are compiled in Fig. 13. The simulations were conducted for an input signal swing of 300 mV_{pp} per side at 128 GS/s (i.e., the clock signal is 64 GHz for all analog input signal frequencies). As can be seen in Fig. 13(a), the large signal bandwidth from the input of the ADC to the output of the THA and also to the input of the comparator is over 40 GHz. The large signal bandwidth from the output of the THA to the input of the comparator (not shown in the figure) is 55 GHz.

The impact of nonlinearities and noise was investigated by conducting a large signal transient noise simulation of the ENOB and SNR at different locations in the path and is shown in Fig. 13(b) and (c), respectively. To calculate the ENOB and SNR, the noise and the harmonics were integrated up to 40 GHz. At the input of the THA, the third-order nonlinearity is dominant at low frequencies and the ENOB remains better than 7 bits. When the analog input signal frequency is larger than 13.3 GHz, the third harmonic falls out of the integration bandwidth and, therefore, the ENOB improves significantly to almost 9.5 bits. At even higher analog input frequencies, the ENOB drops due to signal compression but remains higher than 6.5 bits. At the output of THA, the situation is similar up to the frequency where the third harmonic falls out of the integration bandwidth because the EF stage adds only minor nonlinearities to the sampled signal. However, in contrast to the behavior at the input of the THA, there is no significant improvement in ENOB beyond 13.3 GHz because the performance is limited by the clock path jitter. Similarly, the ENOB drops at much higher frequencies due to gain compression. Finally, since the sampled analog signal goes through more buffers, the ENOB at the input of the comparator is degraded further to slightly better than 5.5 bit below 13.3 GHz. Above 13.3 GHz, the ENOB improves but is still limited by the jitter on the clock path. It remains better than 4.5 bit over the entire 40-GHz bandwidth.

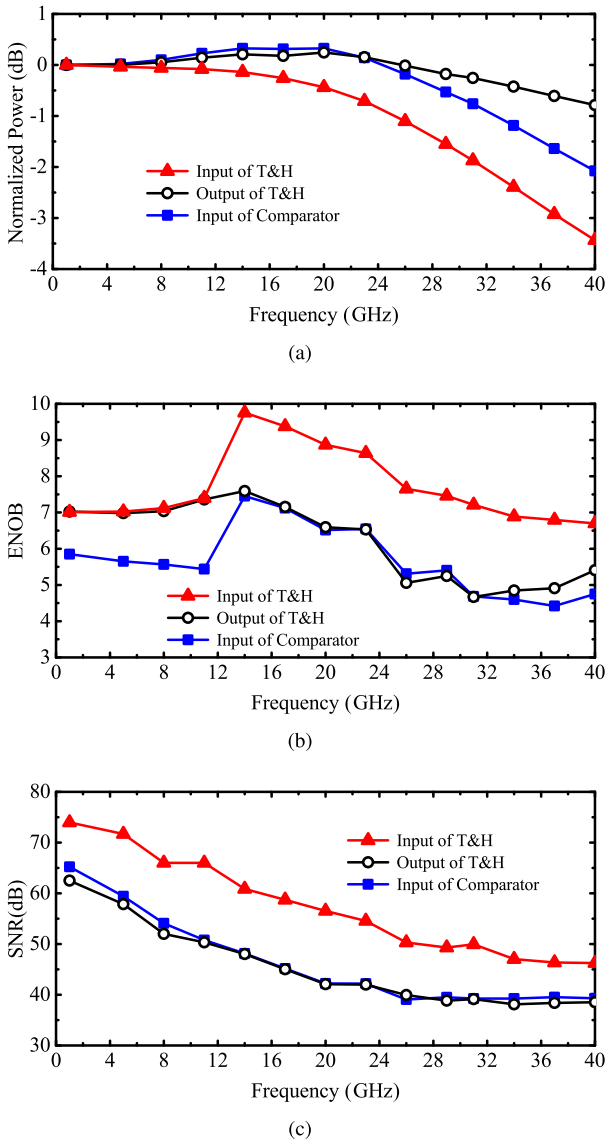


Fig. 13. Simulation of the input analog signal sampling and distribution tree. (a) Normalized power. (b) ENOB. (c) SNR.

D. DAC Implementation

To eliminate the need for on-chip memory and to simplify on-die testing of the ADC, an on-chip 128-GS/s, 5-bit thermometer-coded current-steering DAC was implemented to time-interleave and re-convert the 64 digital bit streams at the output of the ADC to an analog signal. The DAC schematic is shown in Fig. 14. The data input signals to the two sub-DACs have already been retimed with the 180° out-of-phase clocks in the ADC comparator lanes. Therefore, the 0.5-mA tail currents of the 32 current-steering cells of each of the two sub-DACs are time-interleaved by the same complementary 64-GHz clock signals used in each sub-ADC and converted to voltage using 50-Ω load resistors which also provide output matching. Each current-steering unit cell consists of an HBT–HBT cascode with HBT tail current source with resistive degeneration for best matching. The current-steering HBTs are biased at 0.25 mA/μm. The cascode topology improves isolation between adjacent cells. The currents from 16 adjacent cells are

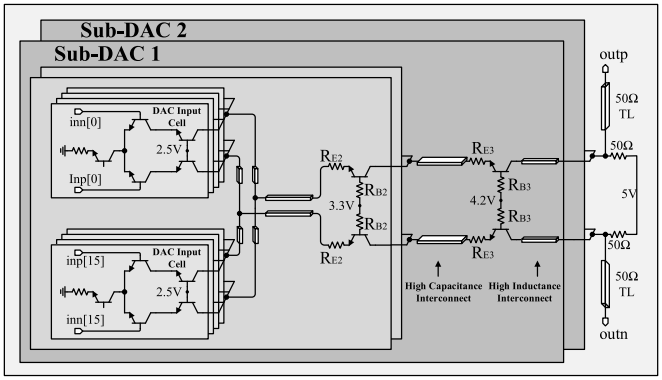


Fig. 14. DAC schematic.

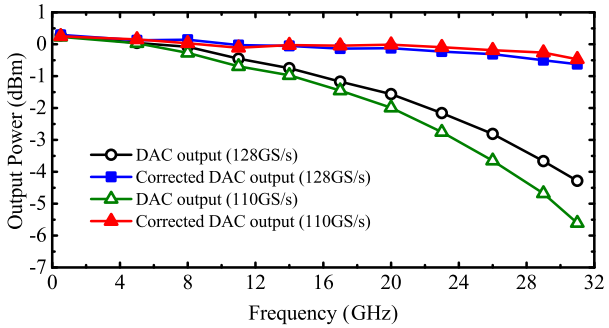


Fig. 15. Simulated large signal DAC bandwidth.

summed at the emitter node of the second common-base HBT in the stack. Resistors R_{E2} and R_{B2} are added to the emitter and base of this second common-base device which carries 8 mA to prevent oscillation. Next, the currents of two such adjacent groupings of 16 current steering cells are combined at the emitter of the third common-base HBT, higher up in the stack. The interconnect lines to the emitter of the third common-base HBT are intentionally designed to be highly capacitive to avoid any extra peaking. Similarly, R_{E3} and R_{B3} are added to lower f_T of the third common-base HBT, which carries 16 mA, to stabilize the DAC. Because of the large number of SiGe HBTs stacked vertically, the DAC uses a supply of 5 V and consumes 400 mW, including the second latch in each sub-ADC comparator lane. The output spectrum of the 2× time-interleaved DAC is shaped by a sinc function with the first null at $f_s/2 = 64$ GHz [24] and must be corrected. The simulated output power of the DAC with and without the sinc-function correction is reproduced in Fig. 15 at 110 and 128 GS/s. The corrected output power decreases by less than 0.5 dB from dc to 32 GHz for both sampling rates.

IV. Experiment

The ADC-DAC chip was manufactured in a commercial 55-nm SiGe BiCMOS process with mm-wave back-end-of-line (BEOL) with eight Cu layers and Alucap, MIM and MOM capacitors, and several flavours of 55-nm MOSFETs, and SiGe HBTs. The highest speed HBTs have 330- and 370-GHz f_T and f_{MAX}, respectively [14]. The top Cu layer and the Alucap layer are more than 2-μm thick. The die microphotograph is

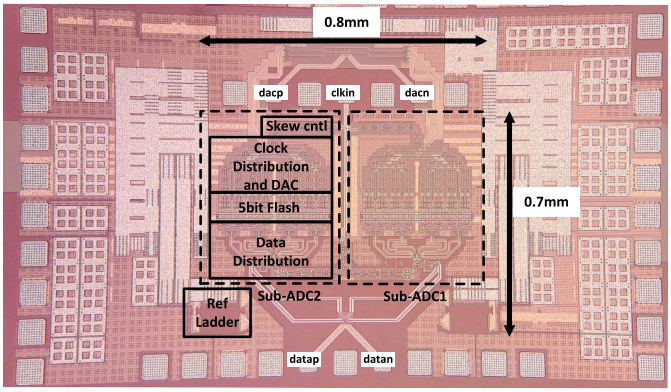


Fig. 16. ADC chip microphotograph showing the layout of the sub-ADC in the inset.

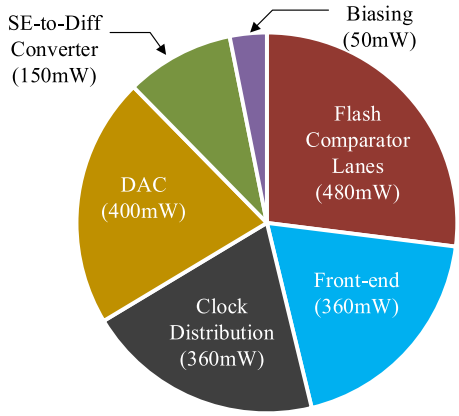


Fig. 17. Breakdown of the power consumption of the ADC-DAC chip.

shown in Fig. 16. Its dimensions are 1.1 mm × 1.9 mm of which the ADC occupies 0.7 mm × 0.8 mm.

The ADC-DAC chip consumes a total of 1.8 W. The breakdown of the power consumption per block is shown in Fig. 17. Assigning the second latch in each lane as part of the DAC, and excluding the 65-GHz single-ended-to-differential input clock buffer (which would eventually be part of the PLL), but including the differential input analog signal and clock signal distribution networks, the power consumption of the ADC is 1.25 W. Each 5-bit flash sub-ADC core, consisting of 32 latched comparator lanes and the resistive ladder, consumes 247.5 mW. It should be noted that, in a typical fiber-optic system application, the DAC would be removed and the second latch in each sub-ADC comparator lane would be assigned to the bubble logic. The second latch in each of the 32 comparators adds another 160 mW to the power consumption of the ADC.

All reported measurements were performed on die. The large signal measurements were carried out with differential inputs and outputs. At the input, the differential drive helps to overcome the reduced common-mode rejection at mm-wave frequencies. At the output, it eliminates the even-order harmonics of the DAC. A four-port Keysight VNA with two locked signal sources was used to calibrate cable losses and provide a fully differential signal at the input of the ADC. The output of the DAC was measured with a 110-GHz bandwidth real-time oscilloscope (RTOS) capable of reading the signal differentially and calculating its spectrum. Therefore, it was also used as a differential spectrum analyzer. The clock signal was provided single endedly from a low-jitter (100 fs_{rms}) 67-GHz Agilent PSG. The large number of cascaded buffers on the clock path provides adequate common-mode rejection even at 65 GHz.

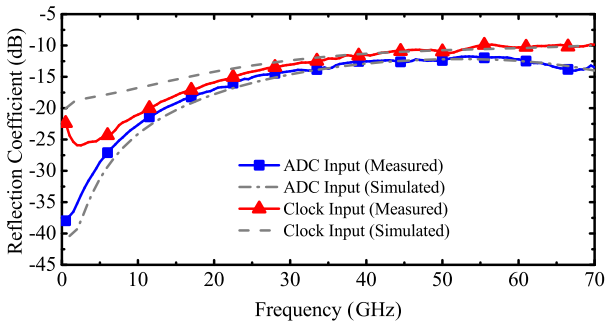


Fig. 18. Reflection coefficient of the ADC analog signal and clock inputs.

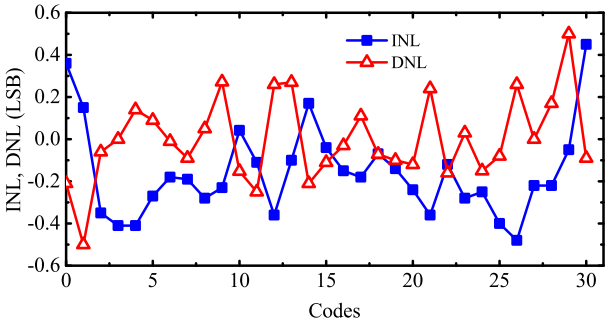


Fig. 19. INL and DNL.

No mismatch correction has been performed. The simulated gain mismatch for the entire front end is less than 0.15 dB which is equivalent to 5-mV mismatch at full swing. The simulated clock skew between the two THAs is 55 fs, less than the clock jitter. The sampling time skew between comparator lanes has a negligible impact as a result of employing THAs in front of each sub-ADC. The simulated comparator offset voltage is 1 mV, significantly lower than the LSB (9 mV) and is one major advantage of SiGe HBT over CMOS comparators. The resistors in the resistive ladder are very wide (50 μm), which ensures less than 0.3% mismatch in the generated reference voltages.

First, small signal S-parameter measurements were performed to obtain the return loss at the analog signal input and at the clock input of the ADC. As demonstrated in Fig. 18, both inputs are very well matched, with the refection coefficients smaller than -10 dB over the entire 67-GHz measurement bandwidth, in excellent agreement with simulations.

Next, the integral nonlinearity (INL) and differential nonlinearity (DNL) of the full ADC-DAC combo were measured with a sampling rate of 128 GS/s for a 100-MHz triangular input signal generated by an arbitrary waveform generator (AWG). As shown in Fig. 19, both INL and DNL are less than 0.5 LSB.

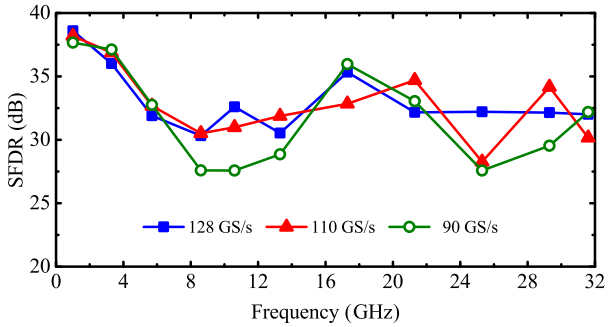


Fig. 20. SFDR measurements for different sampling rates and input signals up to 32 GHz.

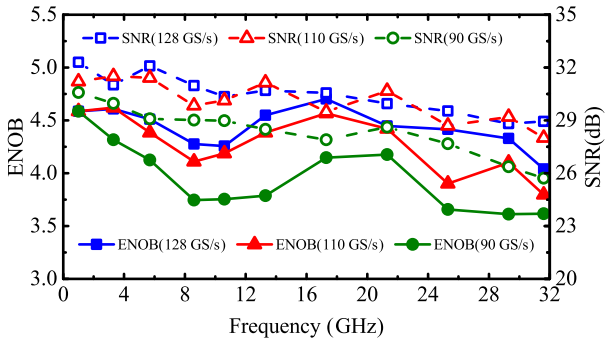


Fig. 21. ENOB and SNR measurements for different sampling rates and input signals up to 32 GHz.

SFDR and ENOB (and SNR) measurements are compiled in Figs. 20 and 21, respectively, for clock frequencies of 45, 55, and 64 GHz corresponding to 90-, 110-, and 128-GS/s sampling rates. No calibration of the ADC and no postprocessing of the measured data were performed beyond integrating the spectrum over the intended 32-GHz input signal bandwidth which is required for 64-Gbd fiber-optic applications. In order to determine the exact output power of the harmonics at the circuit pads, the setup losses due to cables and the 67-GHz probes were measured using a two-tier VNA calibration and then removed. The ADC performance is mainly limited by the third-harmonic distortion at lower frequencies and improves when the third harmonic of the input frequency falls beyond 32 GHz. Measurements show an ENOB better than 4 bits up to 32-GHz input frequencies at 128 GS/s. The ENOB degradation is less than 1 bit over the entire bandwidth of interest. Oversampling the input signal helps to improve the quantization noise and, consequently, the SNDR and the ENOB of the ADC. This is confirmed by the performance degradation observed at 90-GS/s sampling rate. The comparison of the simulated and measured ENOB is shown in Fig. 22. There is good agreement, as the simulation results predict the trend but are slightly better than the measurements. The impact of the RTOS and of impedance mismatches on the setup was not removed in these plots.

To investigate the performance of the ADC for different input signal levels, the measured ENOB is plotted as a function of the input voltage swing in Fig. 23. The measurements were performed for 1- and 31.6-GHz input signals at 128 GS/s. Since thermal noise and quantization noise are independent of

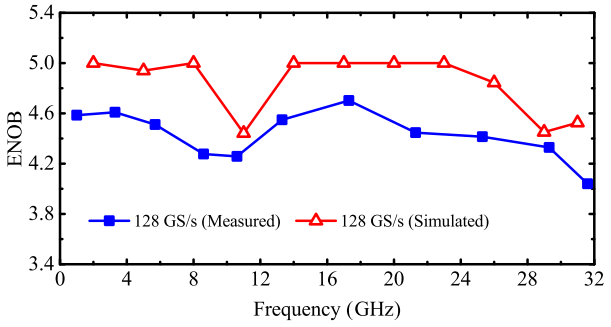


Fig. 22. Comparison of simulated and measured ENOB at 128 GS/s for input signals up to 32 GHz.

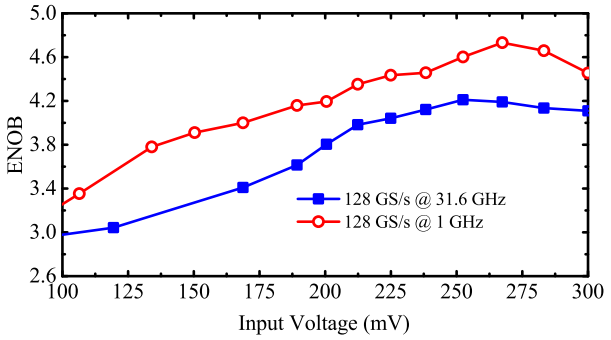


Fig. 23. Measured ENOB at 128 GS/s as a function of the input signal peak-to-peak voltage per side at 1 and 31.6 GHz.

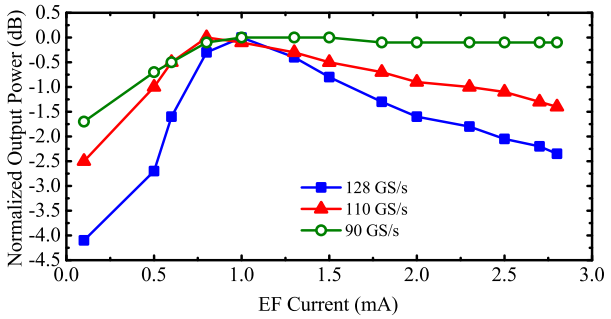


Fig. 24. Impact of the bias current in the EF delay cell on the normalized output power of the ADC for a 31.6-GHz input signal for different sampling rates.

the input signal amplitude when the ADC front end operates in the linear mode, the ENOB improves with increasing input voltage swing. However, as a result of nonlinear behavior, the ENOB starts to decrease for input voltages larger than 270 mV_{pp} per side. The impact is more significant at 1 GHz.

As explained in Section III-C, the delay of the comparator clock signal can be adjusted to increase the time available to the comparator to make a decision. Fig. 24 shows the impact of the delay adjustment obtained by varying the bias current in the EF stages of the single-ended-to-differential-converter block on the normalized DAC output signal power for a 31.6-GHz analog signal applied at the input of the ADC. At lower sampling rates (90 GS/s), where the comparator already has ample time to decide, moving the decision time to the edge of the HOLD phase does not improve the gain/output power. At low bias current, when the delay is too large,

TABLE I
COMPARISON WITH THE STATE OF THE ART

	This work	**[25]**	**[26]**	**[23]**	**[22]**	**[27]**	**[18]**	**[3]**	**[4]**	**[28]**
Technology	**55-nm SiGe BiCMOS**	180-nm SiGe BiCMOS	130-nm SiGe BiCMOS	180-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	32nm CMOS	14nm FinFET	16nm FinFET	20nm CMOS
Architecture	**Flash, 2x**	Flash, 2x	Flash	Flash	Flash	Folding, 4x	SAR, 64x	SAR, 64x	SAR, 64x	SAR, 128x
Resolution (bit)	**5**	5	4	4	6	6	8	8	7	8
Sampling Rate (GS/s)	**90 – 128**	50	40	35	20	30	70/90	72	53	64
Bandwidth (GHz)	**32**	>20	-	-	-	18	22	21	-	-
ENOB (bit) @ fin(GHz)	**4.6 @ 1** **4.4 @ 21** **4 @ 32**	4 @ 1 3.7 @ 12 3.4 @ 22	3.7 @ 1 3 @ 12 2.8 @ 20	3.7 @ 1 3 @ 11 1.6 @ 15	5 @ 2 4.4 @ 6 3.7 @ 10	5.1 @ 1 3.9 @ 10 3.5 @ 16	5.7 @ 1 5.5 @ 10 5.2 @ 20	6.5 @ 1 5.9 @ 21 4.9 @ 32	5.4 @ 1 5.2 @ 21 4.9 @ 26.5	6.3 @ 1 6 @ 8 5.2 @ 19
Area (mm^2)	**0.56**	10.2	1.3	8	0.56	13.6	0.45	0.15	-	-
Power (W)	**1.25/1.8***	5.4	2.3/3.5*	4.5/5*	1	6.5/8.5*	0.35/0.67	0.235	-	0.95
FOM† (mW/bit/GHz)	**1.22**	11.65	8.25	49	3.85	18	0.12/0.2	0.12	-	0.68

* With DAC and/or input clock amplifier †FOM=power/2^ENOB/min(sampling rate, $2\times f_{3dB}$)

the decision occurs after the HOLD time and a sudden drop in the output power can be observed. However, at higher sampling rates, the comparator does not have enough time to make the decision and, therefore, moving the decision time to the edge of the HOLD phase increases the output power. A considerable improvement is observed for the 128-GS/s curve, where the output power increases by 2 dB when the bias current is 1 mA and the delay is optimized. Therefore, it can be concluded that the large-signal bandwidth of the ADC is limited at higher sampling rates by the speed of the comparator when the decision cannot be made within the short available time. The measurements were conducted with the analog input signal at 31.6 GHz. The delay adjustment has a diminishing impact, as the input signal frequency is reduced. It has to be mentioned that once the optimal clock delay for the highest input bandwidth is found, the ADC shows consistent performance during the measurement; therefore, the EF current does not need to be changed afterward.

A comparison of the measured and simulated large signal transfer function of the ADC-DAC combo at 128 and 110 GS/s is shown in Fig. 25. The EF delay was optimized for the highest bandwidth. The measured bandwidths for 128- and 110-GS/s sampling rates are 34 and 32 GHz, respectively, and show excellent agreement with simulation results. The output power was corrected for the DAC sinc function.

Fig. 26 reproduces the spectrum measured at the DAC output for a 31.3-GHz input signal sampled at 128 GS/s. An intentional gain/offset mismatch was introduced in Fig. 26(a) between the two sub-ADCs. It is apparent that the sub-ADC mismatch leads to only partial image cancellation. However, as shown in Fig. 26(b), when the two sub-ADCs are matched, the time-interleaving function effectively removes the image signals.

Table I summarizes the performance of the ADC-DAC chip and compares it with other state-of-the-art SiGe BiCMOS and the highest performance and most recent CMOS ADCs in planar bulk and FinFET technologies. This design achieves the best bandwidth and sampling rate with much better energy efficiency than all other SiGe BiCMOS ADCs, but its power consumption and figure of merit are worse than those of the best 14- and 16-nm FinFET CMOS ADCs. However, the latter have only 26.5 GHz or lower effective resolution bandwidth. At this time, CMOS ADCs also achieve better ENOB at 32 GHz, starting with a 3-bit higher resolution architecture, than the SiGe BiCMOS ADC reported here. Nevertheless,

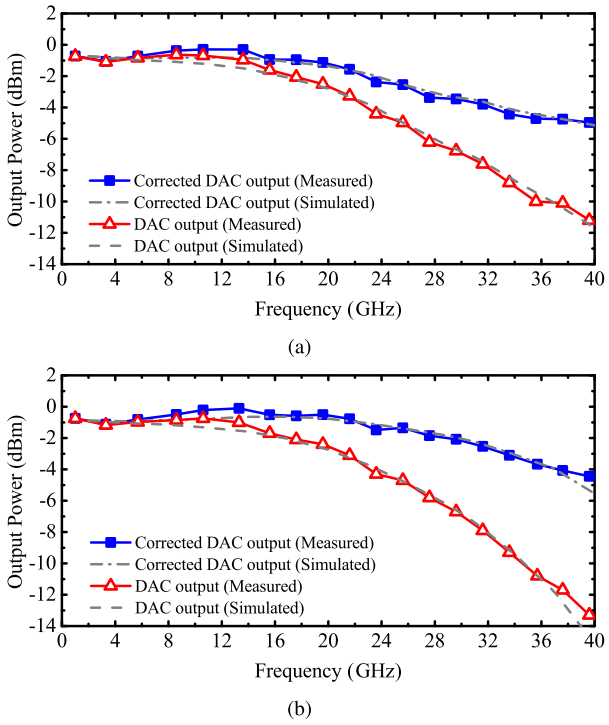
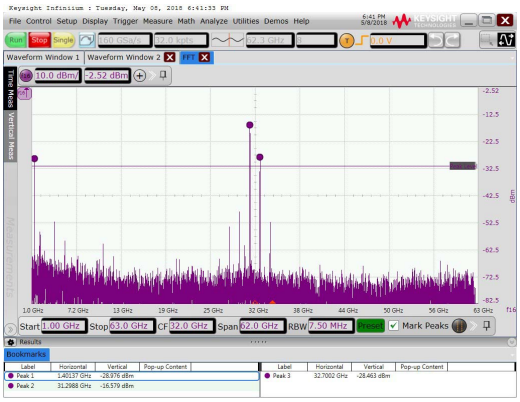


Fig. 25. Comparison of the measured and simulated large signal output power of the ADC-DAC combo versus analog input signal frequency at (a) 128 and (b) 110 GS/s.



(a)

(b)

Fig. 26. DAC output spectrum for a 31.3-GHz input signal sampled at 128 GS/s (a) with and (b) without intentional mismatch between the two sub-ADCs.

while there is little bandwidth, sampling rate, and resolution improvement in the highest bandwidth CMOS ADCs over recent technology nodes [3], [4], the improvement reported in this paper over older SiGe BiCMOS technology ADCs is significant and is expected to continue in the future because, unlike CMOS for which the Dennard-rule scaling ended in the mid-2000s [29], the high-frequency performance of SiGe HBTs continues to improve according to "goldilocks" scaling rules [9], [30].

V. Conclusion

The highest bandwidth and sampling-rate ADC was demonstrated using a 55-nm SiGe BiCMOS technology. This performance was made possible by the use of a new 5-bit time-interleaved flash-ADC architecture with track and hold amplifiers and novel low-power and small layout-footprint comparator and latch topologies. Transient large-signal noise simulations suggest that the ENOB above 30 GHz is limited by jitter on the clock distribution path and not by quantization or thermal noise. Oversampling, which takes advantage of the high switching speed of the SiGe HBT, leads to less than 1-bit degradation in ENOB from the nominal resolution of the ADC.

The power consumption could be further reduced if the portion of the clock distribution network that performs single-ended-to-differential conversion was redesigned to operate from 1.8 V or if the whole clock distribution network was implemented to operate from 1.2-V supply using HBT CML clock buffers, as in the 60-GHz radio transceiver in [31]. In a 28-nm FDSOI SiGe BiCMOS process with the same SiGe HBT, the 65-GHz clock path could be implemented in CMOS CML from 0.8-V supply.

The 2× time-interleaved flash ADC is scalable to 4× time-interleaving using a quadrature clock generator with four 25% duty-cycle outputs at up to 62 GHz recently reported in the same technology. This would potentially allow for a bandwidth of 60 GHz to be digitized at 160–260-GS/s sampling rates by redesigning the analog front end for more bandwidth, which is currently limited to about 40 GHz.

The proposed latch and comparator circuit topologies with active inductors and the ADC architecture are scalable in terms of layout footprint and high-frequency performance for 128-Gbd fiber-optic systems in a SiGe BiCMOS process with HBT f_T/f_{MAX} larger than 450/600 GHz, currently under development at several foundries [30]. A 2-bit 128-Gbd DAC and multi-chip 256-GS/s ADCs have already been demonstrated using InP HBT technologies with $f_{MAX} > 450$ GHz [32].

Acknowledgment

The authors would like to thank Integrand Software Inc., for providing the EMX simulation software. They would also like to thank J. Pristupa and CMC for CAD tools and CAD support.

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