Predictive Modelling of Lateral Scaling in Bipolar Transistors

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ABSTRACT

A new approach for modelling the dependence of bipolar transistor characteristics on emitter width and length is presented. The new model, verified by device simulation and measurement, predicts device behavior accurately over a wide range of emitter aspect ratios.

1 Introduction

Silicon based bipolar transistors have been demonstrated to be well-suited for high-speed circuits required, e.g. in wireless and fiber-optic applications [1, 2]. Optimizing the performance of these circuits, which are often custom designed, requires the flexibility to vary emitter dimensions and transistor configuration. For high-speed applications, the option to vary emitter width b_E and length l_E is especially important, while for low-power applications transistors with the smallest possible emitter size, i.e. minimum b_E and $l_E(\rightarrow b_E)$, are required. While predictive transistor modelling for l_E variation is possible with present compact models for $l_E > 10b_E$, width dependence of important transistor parameters such as transit frequency and transit time cannot be accurately described at the required medium and high current densities by using a single model parameter set. Moreover, three dimensional (3D) effects occurring if l_E approaches b_E have not been taken into account yet.

The impact of 2D and 3D effects on transistor characteristics is shown in Figure 1 for the transit frequency f_T vs. collector current I_C, normalized to an effective emitter area A_E. Emitter periphery injection and collector current spreading are primarily responsible for the differences observed in f_T between the 1D, 2D and 3D cases. For circuit design and optimization, predictive modelling of such characteristics is desirable. As a consequence, (semi-) physical relations suited for application in a compact model are required which permit a calculation of the equivalent circuit elements as a function of transistor and, in particular, emitter dimensions.

This paper describes an approach for modelling the influence of emitter width and length variation (including 3D effects) on transistor behavior, which is suited for compact models. The respective analytical relations are derived and verified first based on 2D and 3D device simulation in order to ensure well-defined conditions. Afterwards, the model is applied to measurements as well.

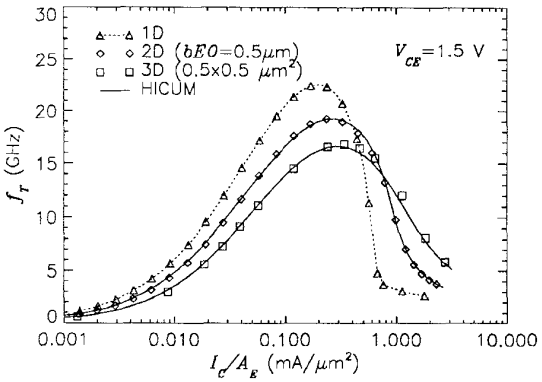

Figure 1: Transit frequency vs. collector current density for 1D, 2D and 3D device simulations. The solid lines are the results of the compact model HICUM.

2 Theory

Generally, a bipolar transistor can be divided into an inactive (external) device and an active device. The latter consists of the internal transistor under the emitter window and the transistor at the emitter periphery. The equivalent circuit elements of the inactive device, like external series resistances and external capacitances, can be calculated in a simple way for given emitter dimensions from design rules and specific parameters, e.g. capacitances per area or sheet resistances, which can be determined from measurements of proper test structures. Any process variation in specific data and in design rules can then be easily included.

The calculation of the equivalent circuit element values for the active transistor region as a function of

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emitter dimensions is more complicated. This is particularly true for transistor operation at high current *densities*, which is required in high-speed applications. Therefore, the discussion below focuses on scaling issues of the active transistor. Two cases can be distinguished.

2.1 Low collector current densities

Emitter periphery injection is the 2D and 3D effect of interest in this operating region. The resulting additional peripheral current can be incorporated into the collector current source of an equivalent circuit by extending the idea of an effective emitter area [3] to the 3D case

$$A_E = b_E l_E = (b_{E0} + 2\gamma_C)(l_{E0} + 2\gamma_C) > A_{E0} \quad . \quad (1)$$

$A_{E0} = l_{E0} b_{E0}$ is the emitter window area. The technology parameter γ_C can be extracted from measurements of long (2D) transistors with different b_{E0} [3]. Using $\gamma_C = 0.051\mu$m as obtained from 2D device simulation, I_C/A_E in Figure 2 exhibits perfect agreement for all curves at low bias indicating that (1) can be employed for 3D scaling purposes. Note that no additional parameter is required for modelling the corner contribution. The differences at high current densities are caused by collector current spreading (see Section 2.2).

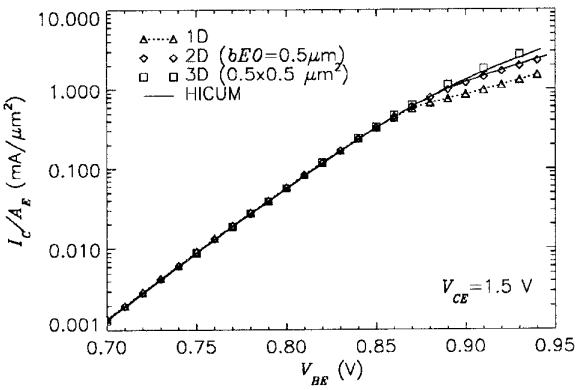

Figure 2: Collector current density vs. base-emitter voltage for 1D, 2D and 3D device simulations. The solid lines are the results of the compact model HICUM.

The impact of 3D emitter periphery injection (and collector current spreading) on the dynamic transistor behavior is clearly demonstrated by the f_T characteristics in Figure 1. A 1D model is obviously not adequate. The difference in peak f_T is roughly inversely proportional to a difference in the transit time τ_f. Since the transit time τ_{fp} of electrons injected at the periphery is larger than the component τ_{fi} of electrons injected under the emitter window, the low current transit time τ_{f0} is highest and peak f_T is lowest for the 3D case with $l_E/b_E = 1$. Both τ_{fi} and τ_{fp} can be determined from f_T of long (2D) transistors with different emitter widths. A simple derivation shows that the total (measured) low-current transit time can be "scaled" with emitter dimensions according to

$$\tau_{f0} = \frac{\tau_{fi} + \tau_{fp}\gamma_C L_E/A_{E0}}{1 + \gamma_C L_{E0}/A_{E0}} \quad (2)$$

with $L_{E0} = 2(b_{E0} + l_{E0})$, and $L_E = L_{E0} + 4\gamma_C$.

Multiplication of all area specific model parameters of the internal transistor, like saturation current density and capacitances per area, with A_E as well as using the effective emitter width and length for calculating the internal base resistance r_{Bi} according to [4] leads to a model parameter set for the 3D case.

2.2 Medium and high collector current densities

In this case, the parameters describing the internal and peripheral transistor cannot be separated due to the superposition of current spreading, mainly in the collector, emitter current crowding, and periphery injection, all of which are 2D (and 3D) effects. At higher current densities f_T in Figure 1 decreases least for the 3D case since collector current spreading, which reduces the Kirk effect, is most pronounced for large L_{E0}/A_{E0}. This effect could not be predicted by presently available bipolar compact models.

An important quantity indicating the decrease of f_T at high current densities is the critical current density J_{CK}, which describes the onset of high-injection into the collector, i.e. the strong increase of τ_f and, thus, the strong decrease of f_T at high current densities. J_{CK} can be expressed as a function of the internal collector-emitter voltage V_{CEi}, technological and physical parameters, and temperature as [5, 6, 7]

$$J_{CK} = \frac{V_c/r_{Ci0}}{\sqrt{1 + (V_c/V_{lim})^2}} \cdot \begin{cases} 1 & , V_c \le V_{lim} \\ 1 + \frac{V_c - V_{lim}}{V_{PT}} & , V_c > V_{lim} \end{cases} \quad (3)$$

using $V_c = V_{CEi} - V_{CES}$. The area-specific low-field resistance of the epitaxial collector $r_{Ci0} = w_C/(q\mu_{nC0}N_C)$, the voltage $V_{lim} = v_{sn}w_C/\mu_{nC0}$, and the CE saturation voltage V_{CES} are all model parameters. N_C,w_C and μ_{nC0} are the doping, width and mobility of the (epi) collector, respectively, and v_{sn} is the electron saturation velocity.

The critical current I_{CK} for a particular emitter size in the general 3D case is given by

$$I_{CK} = J_{CK} A_E f_{cs}(b_{E0}, l_{E0}) \quad (4)$$

assuming a certain angle δ_C for collector current spreading at $I_C = I_{CK}$. For the 3D case with $l_E > b_E$ the "current spreading" function f_{cs} reads

$$f_{cs} = \frac{\xi_b - \xi_l}{\ln[(1+\xi_b)/(1+\xi_l)]} > 1 \qquad (5)$$

and depends on technological data via the variables

$$\xi_b = 2\frac{w_C}{b_E}\tan(\delta_C) \quad \text{and} \quad \xi_l = 2\frac{w_C}{l_E}\tan(\delta_C) \quad . \qquad (6)$$

For $l_E \to b_E$ a series expansion can be used giving $f_{cs} = (1+\xi_b)$ for the special case $b_E = l_E$. Since the angle δ_C depends on various factors such as the encroachment of the external base profile into the internal transistor, the derivation of a useful physical analytical relation for δ_C is very difficult. Thus, δ_C is considered a model parameter.

Injection into the collector at high current densities leads to an additional charge storage and is strongly influenced by 2D and 3D collector current spreading. The following expression can be derived for the corresponding hole charge as a function of collector current and voltage

$$Q_{pC} = \tau_{20} I_C f_{ci}(I_C, V_{CEi}) \qquad (7)$$

with $\tau_{20} = {w_C}^2/(4\mu_{nC0}V_T)$. The "collector injection" function f_{ci} is given for the 2D case by

$$f_{ci}(I_C, V_{CEi}) = \frac{(1+\xi_i)^2 - 1 - 2\ln(1+\xi_i)}{2{\xi_b}^2} \qquad (8)$$

with

$$\xi_i(I_C, V_{CEi}) = 2(w_i/b_E)\tan(\delta_C) \qquad (9)$$

which depends on technological data. The width of the injection zone ($I_C > I_{CK}$) for the 2D case is

$$w_i(I_C, V_{CEi}) = \frac{w_C}{\xi_b}\left[(1+\xi_b)\exp\left(-\frac{I_{CK}\xi_b}{I_C f_{cs}}\right) - 1\right] \quad . \qquad (10)$$

For the general 3D case ($l_E > b_E$), the corresponding expression for f_{ci} is more complicated but can still be evaluated explicitly. For $b_E = l_E$, however, f_{ci} becomes quite simple.

3 Application and Results

The principle described above for low current densities can be applied to any compact model like, e.g. the SPICE Gummel-Poon model (SPGM). The complete set of formulas has been implemented into the compact transistor model HICUM [8, 9]. In the case of I_{CK}, which is directly used in HICUM for modelling the minority charge storage, only the model parameter r_{Ci0} needs to be modified for the respective emitter dimensions. The former expression for the collector hole charge Q_{pC} has been replaced by equations (7) to (10). The model parameters were obtained from test structures; γ_C, τ_{fi0} and τ_{fp0} were determined from transistors with different emitter widths $b_{E0} \ll l_{E0}$. Based on the resulting area and periphery specific data, the model parameters for arbitrary emitter dimensions have been calculated using the new 2D and 3D equations. The results presented below refer to a double-polysilicon technology. The minimum emitter window width is $b_{E0} = 0.5\mu$m, which is considered as the nominal width. Also, $b_{E0} = 1$ μm has been selected.

First, the model was verified by device simulation using an extended version of the simulator presented in [10]. In this case, δ_C was taken directly from current flow lines in order to verify the predictive capability and physical basis of the underlying equations. Figures 1, 2 and 3 show good agreement for the predicted characteristics of the 2D transistor with $b_{E0} = 1\mu$m and the 3D transistor with $b_{E0} = l_{E0}$.

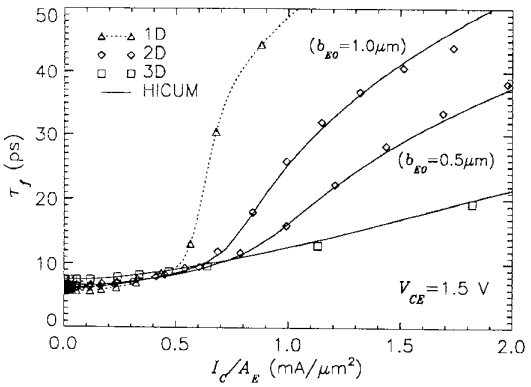

Figure 3: Transit time vs. collector current density for 1D, 2D and 3D (0.5x0.5 μm^2) device simulations. The solid lines are the results of the compact model HICUM.

Measured results are shown in Figure 4 and confirm those obtained for device simulation. The transit time for the larger emitter width is predicted by HICUM using the δ_C value determined from device simulation. δ_C can also be extracted from measurements of transistors with two different widths ($b_{E0} \ll l_{E0}$).

The switching behavior of a 3D structure with $l_{E0} = 2b_{E0}$ is compared to the HICUM prediction in Figure 5. The agreement for the collector current is quite good in this example of a switching off process for an inverter with zero generator and load resistance. This configuration has been chosen to make the com-

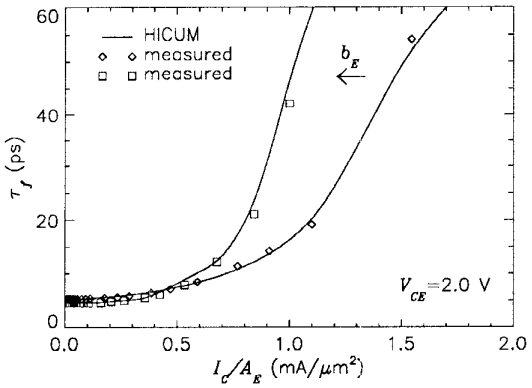

Figure 4: Transit time vs. collector current density for a self-aligned double-poly transistor with varying emitter width: measurement (symbols) and HICUM (lines).

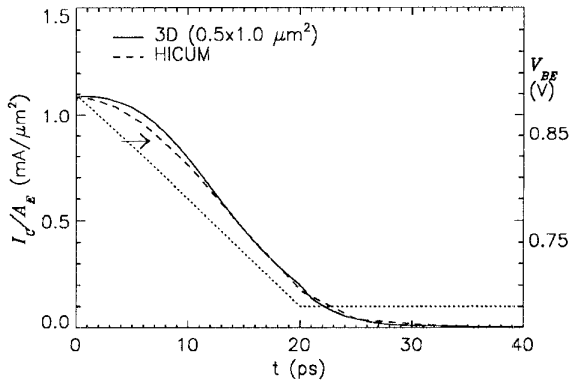

Figure 5: Collector current for a transistor inverter switching-off cycle (V_{CE}=1.5V).

parison sensitive to model errors in internal base resistance and minority charge storage.

4 Conclusions

Based on physical considerations, simple, explicit relations have been derived for predicting the emitter size dependence of key parameters and characteristics of bipolar transistors. The scaling methodology developed for low current densities as well as the expression for collector charge storage are applicable to other compact models as well. The new expression for the critical current is generally useful for designing high-speed circuits, regardless of the compact model employed.

As demonstrated by device simulation and measurements, combination of these relations with the compact model HICUM yields accurate description and prediction of the electrical behavior for both the 2D and 3D (short emitter) cases.

Acknowledgments:

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