A 60 mW per Lane, 4×23-Gb/s $2^7 - 1$ PRBS Generator

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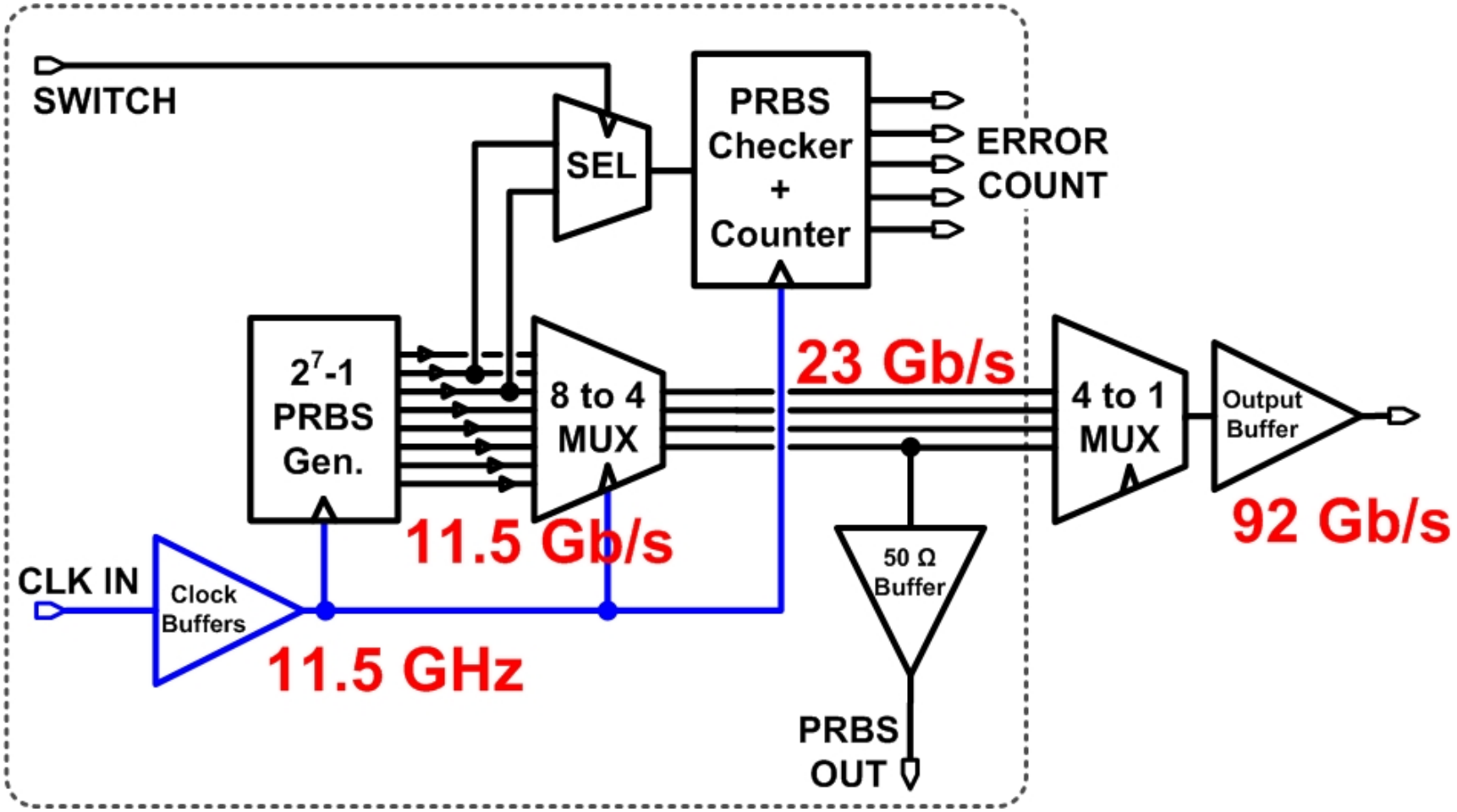
Outline

- Motivation
- System overview
- PRBS generator topology
- Latch design
- Measurement results
- Summary

Motivation

- On-chip BIST for 80-Gb/s transceiver
- Minimize power and area without compromising speed
  - At system level by topology choice
  - At transistor level
- Investigate techniques for further power reduction of high-speed digital blocks

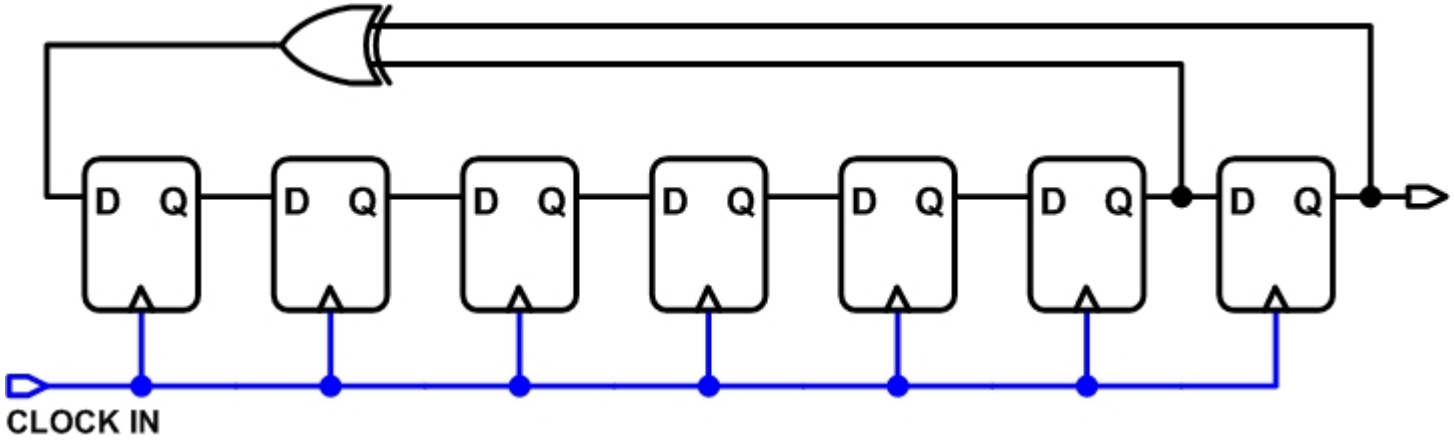
System Overview



PRBS Generator Topology

Series 2^7-1 PRBS Generator

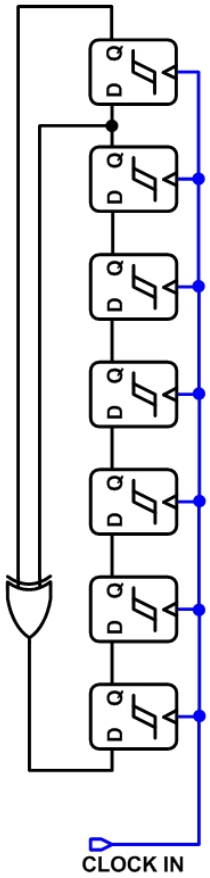
$$x^7 + x^6 + 1 = 0$$



Only 1 PRBS output but need 8

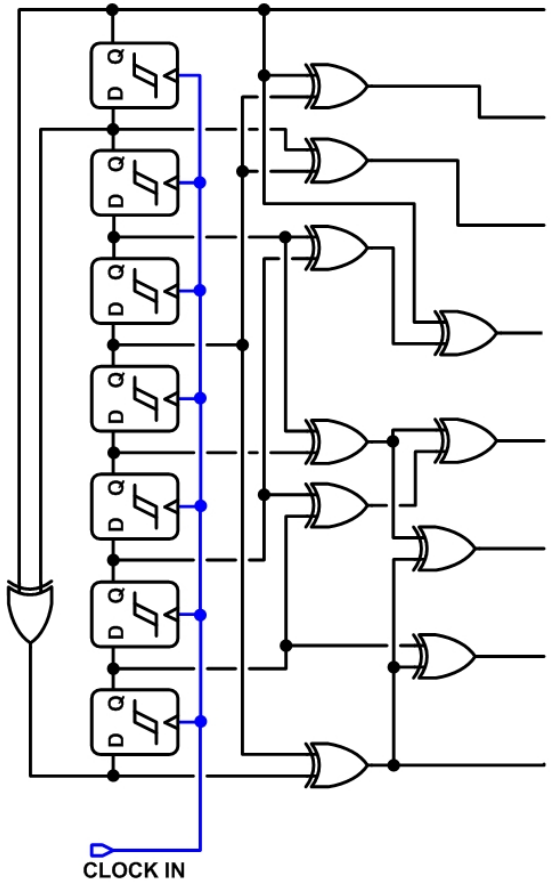
PRBS Generator Topology

Series Generator



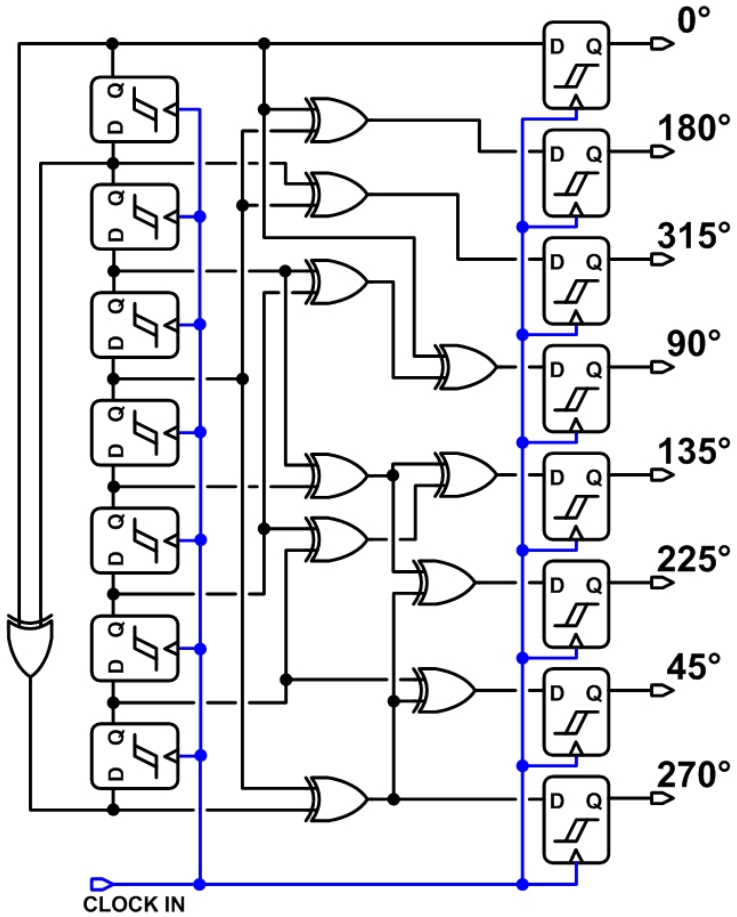
PRBS Generator Topology

Series Generator



PRBS Generator Topology

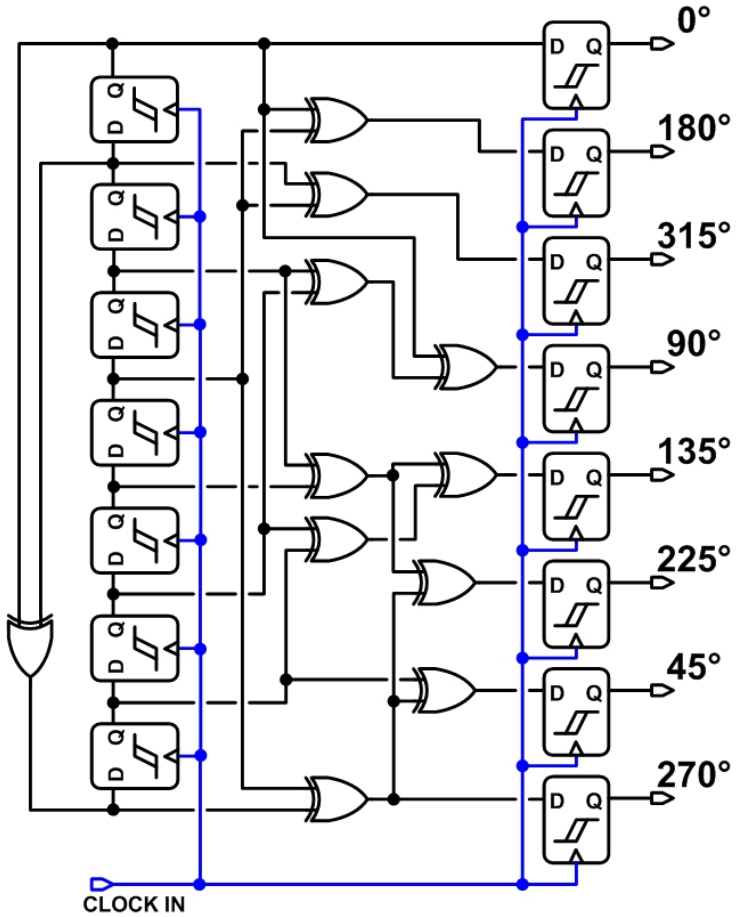
Series Generator



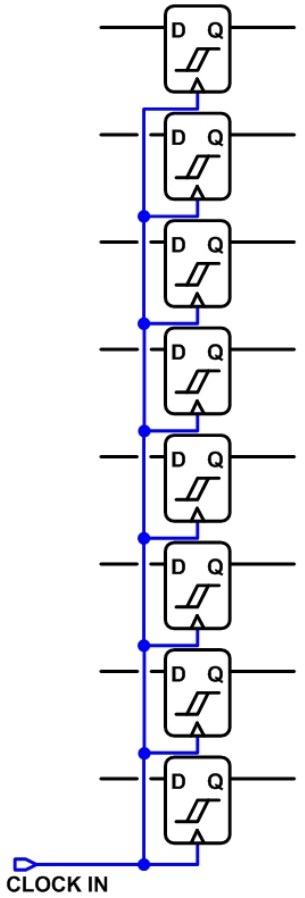
Inefficient due to phase - shifting and retiming overhead

PRBS Generator Topology

Series Generator

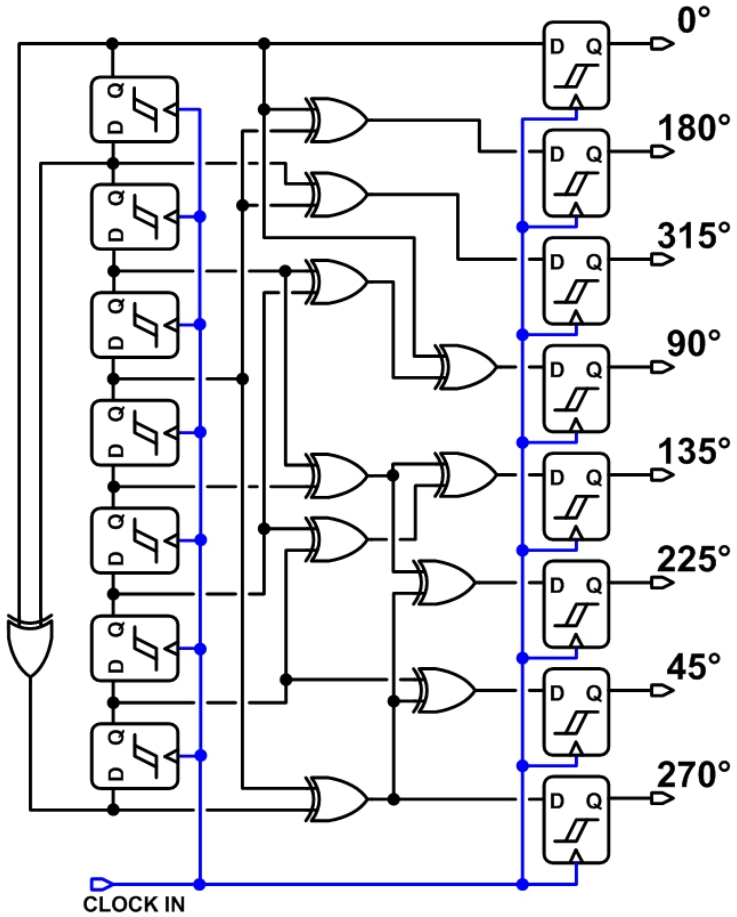


Parallel Generator [1]

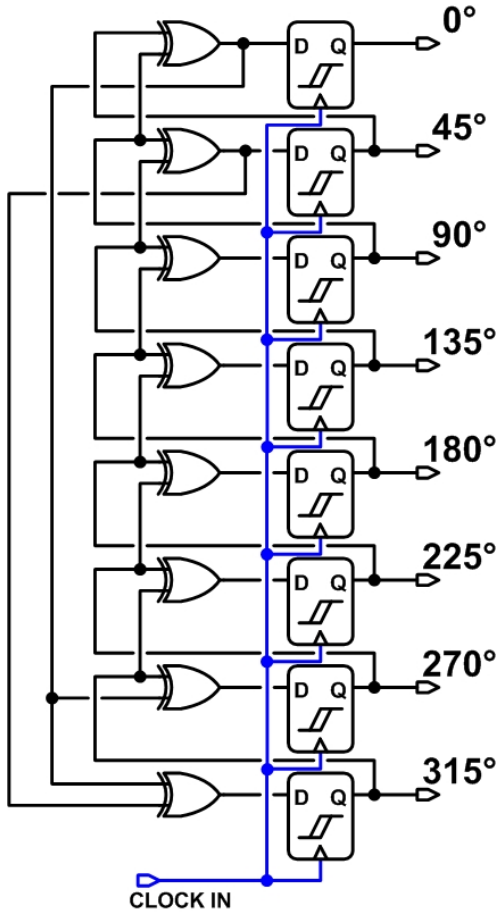


PRBS Generator Topology

Series Generator

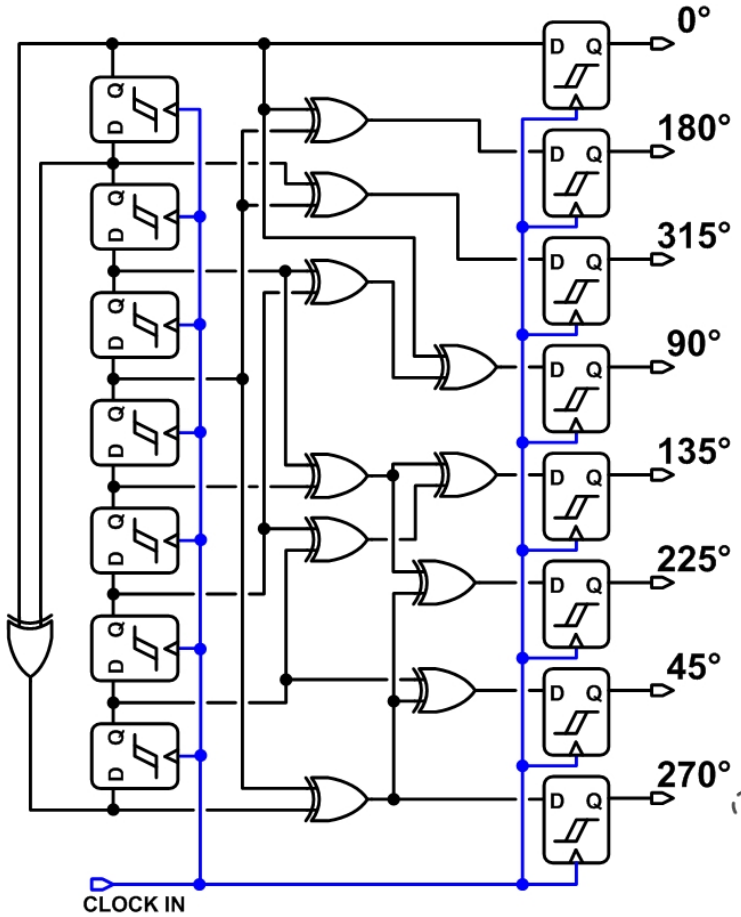


Parallel Generator [1]



PRBS Generator Topology

Series Generator

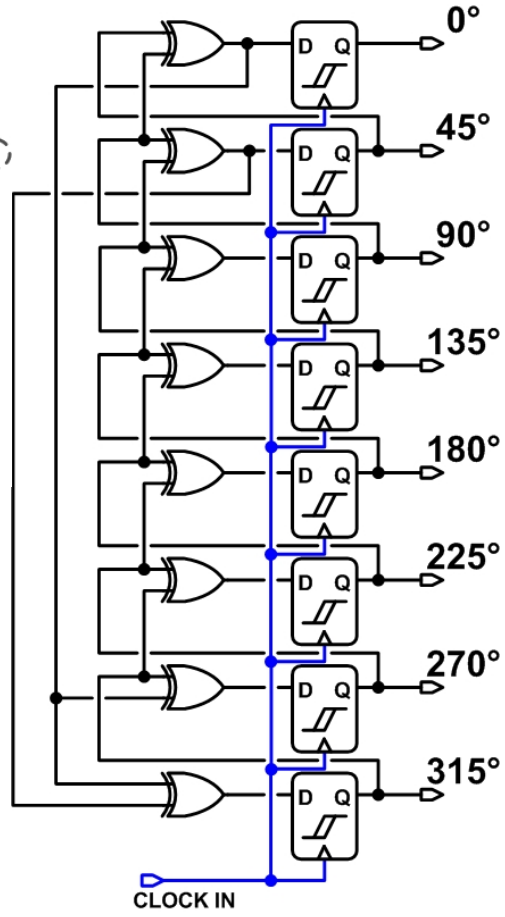


8 DFFs
8 XORs
140 mW

42%
power
savings

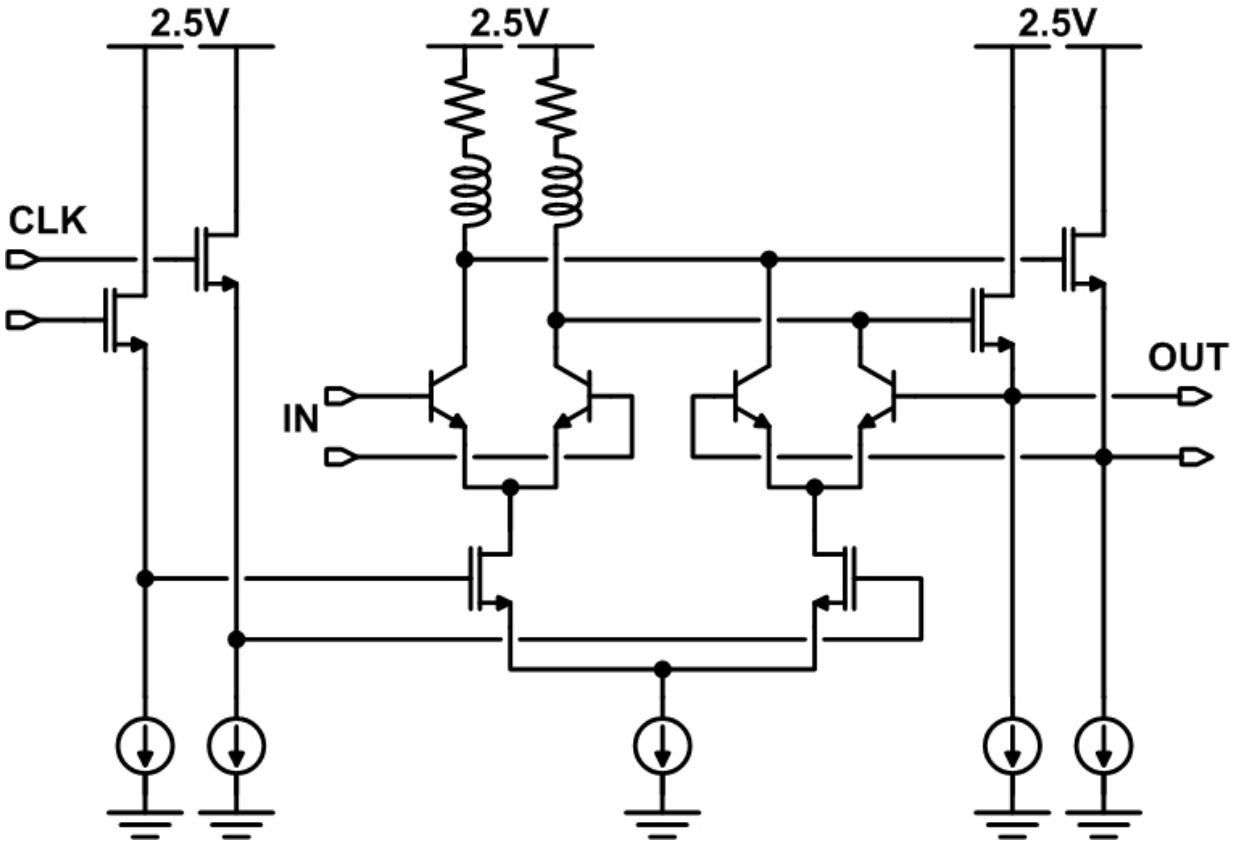
15 DFFs
11 XORs
242 mW

Parallel Generator [1]



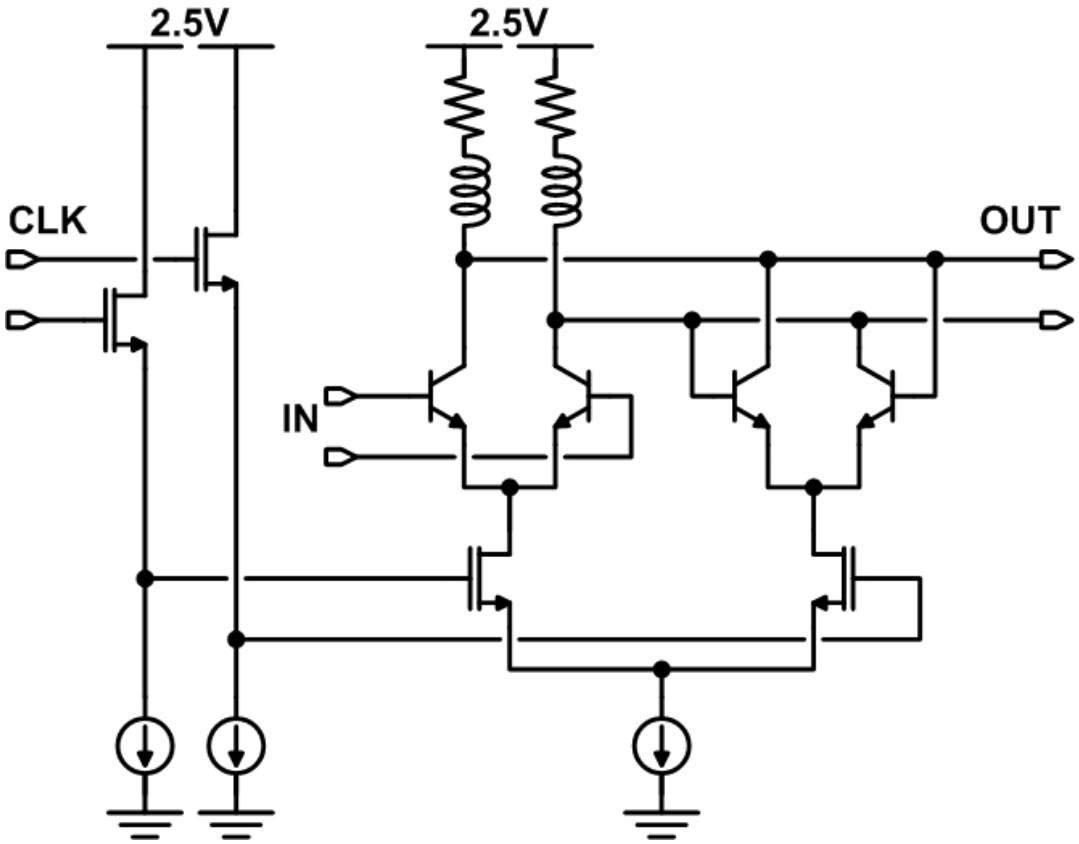
12-GHz Latch Design

- **Start from the BiCMOS cascode D-Latch [2]**



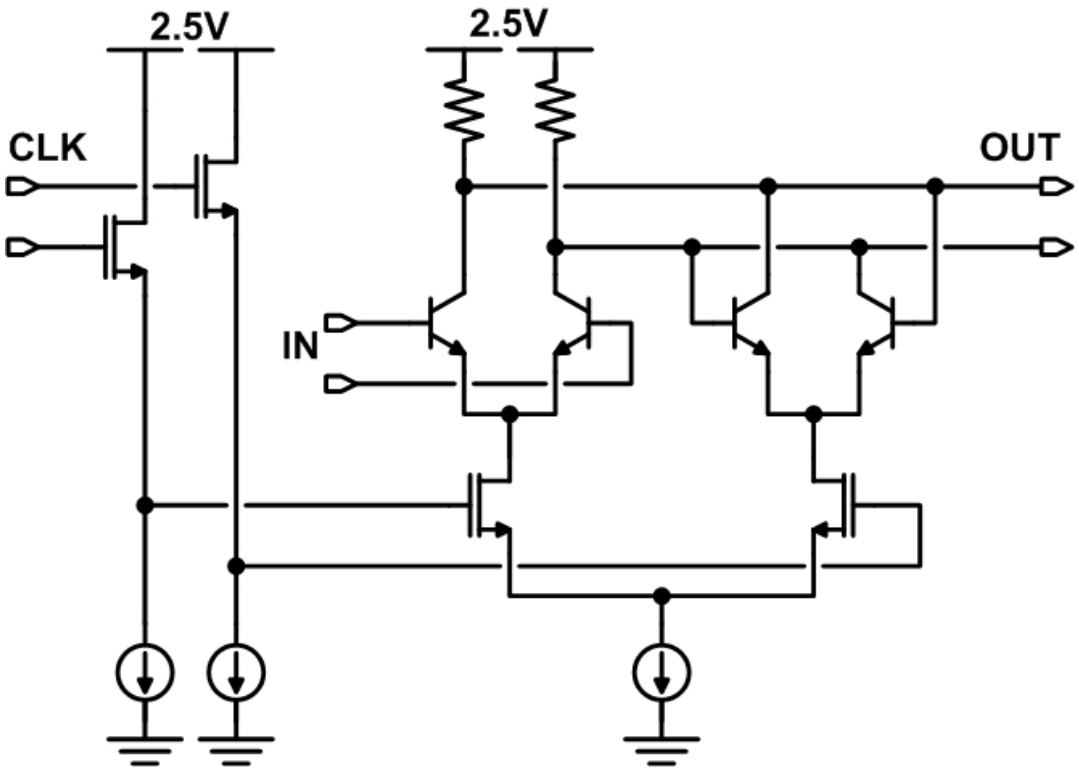
12-GHz Latch Design

- **Remove the output source-followers**



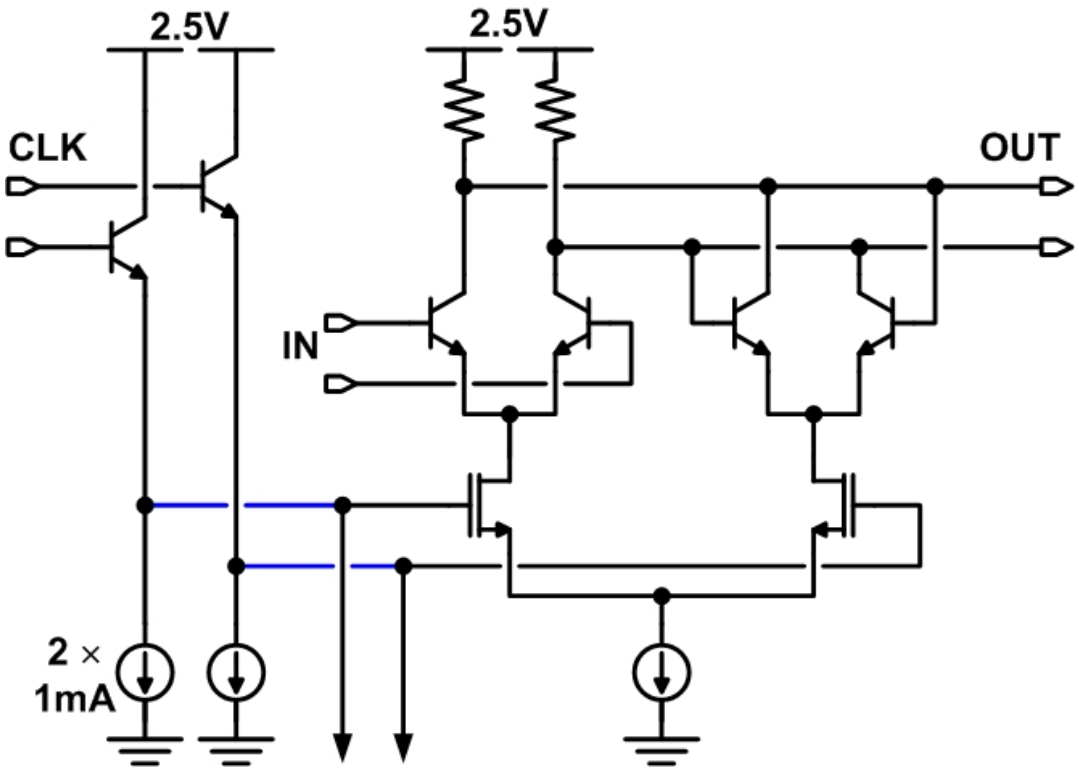
12-GHz Latch Design

- **Remove the inductors to save area**

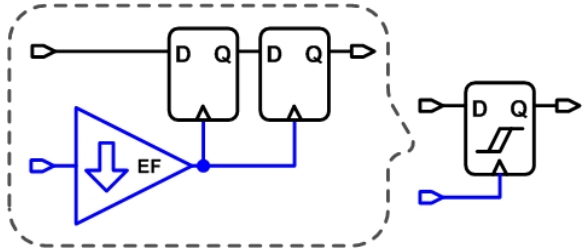


12-GHz Latch Design

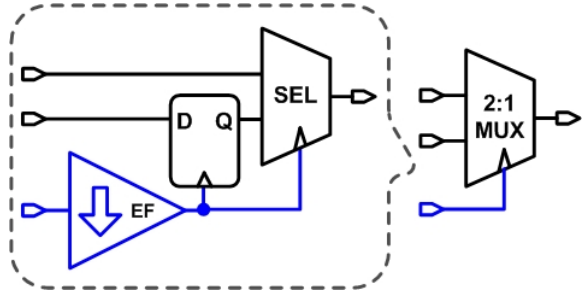
- **Share the clock emitter followers for 2 blocks**



12 - GHz DFF

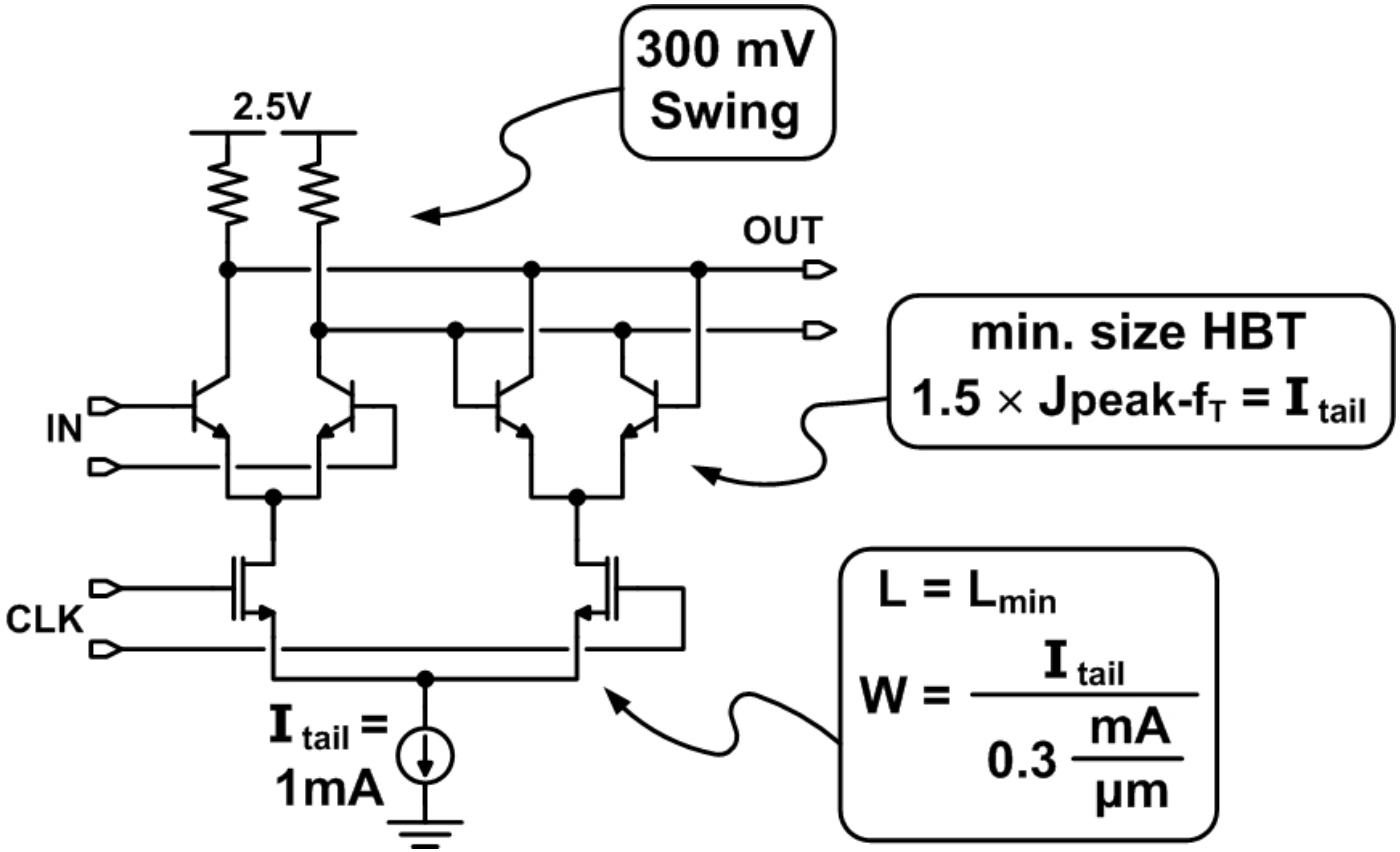


24 - Gb/s 2:1 MUX

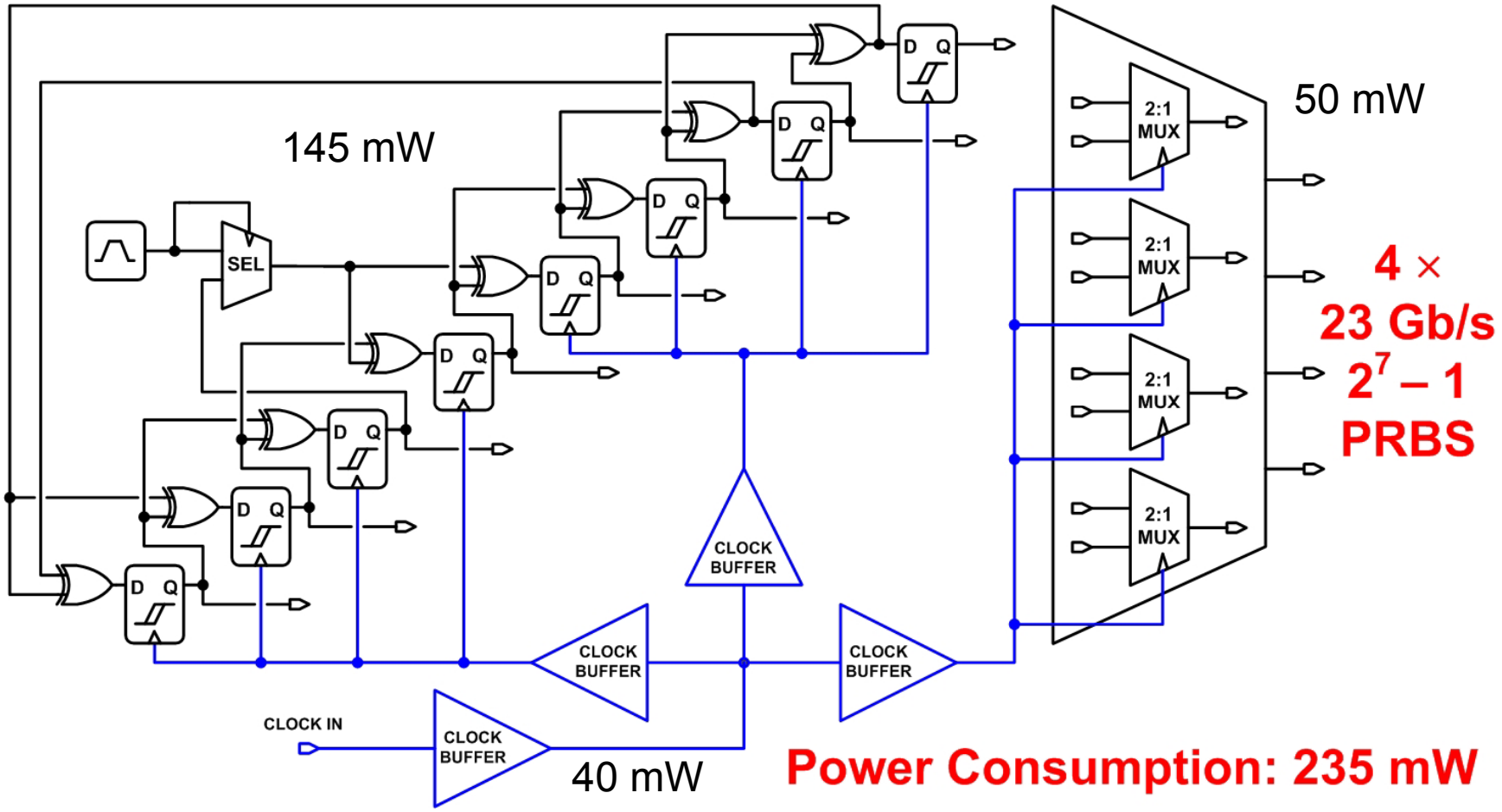


12-GHz Latch Design

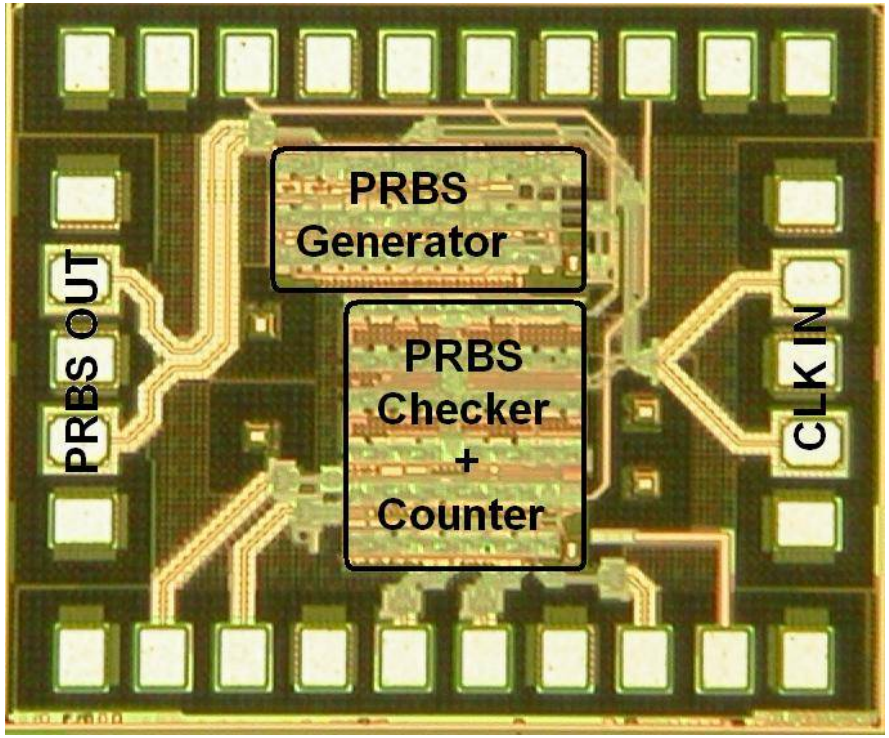
- **Reduce tail current to 1 mA**



Final Generator Schematic



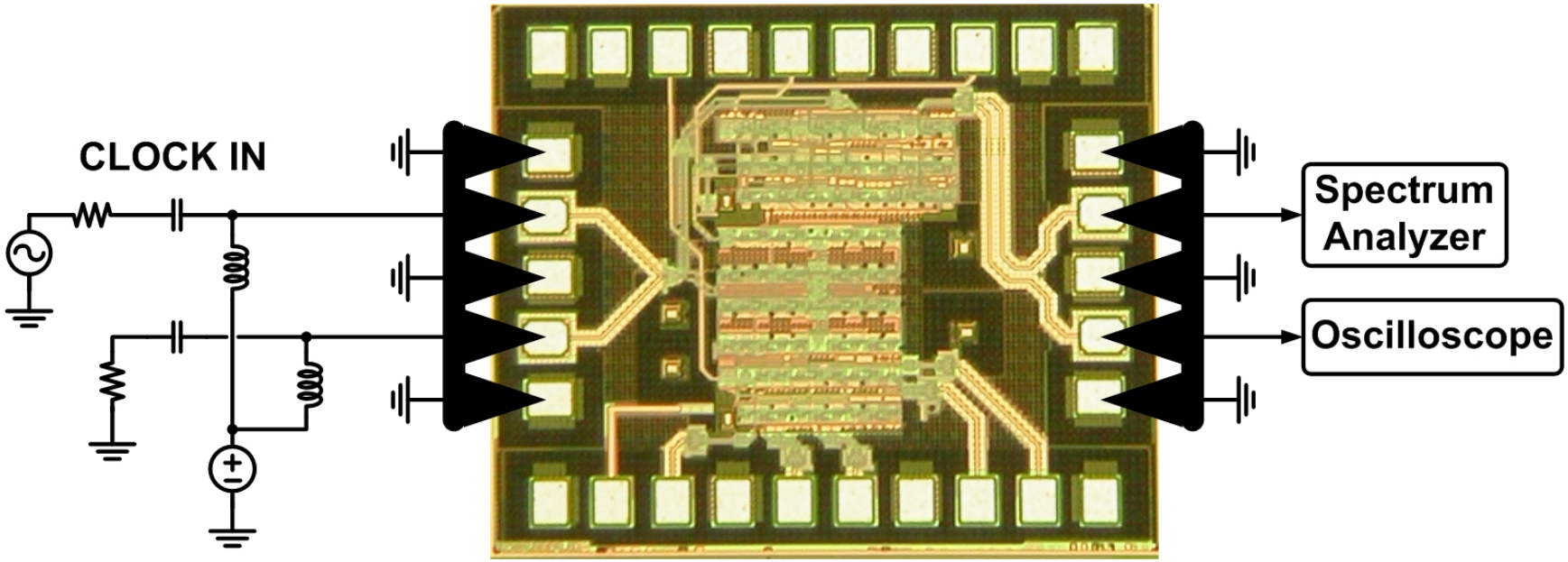
Die Photo



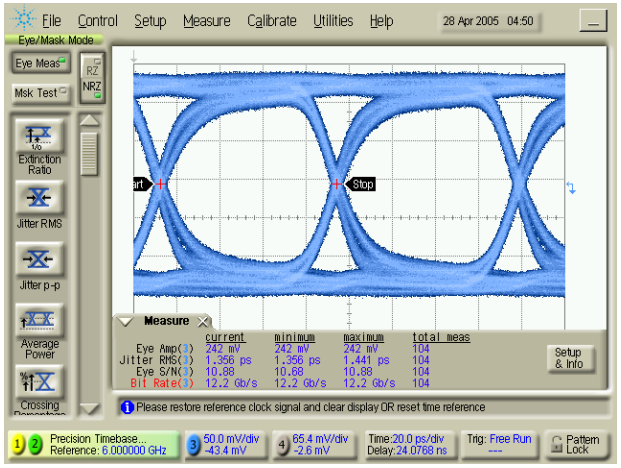
- 0.13 SiGe BiCMOS
- f_T = 160 GHz
- Chip:
  - 1 mm × 0.8 mm
  - 940 mW
- PRBS Generator:
  - 393 µm × 178 µm
  - 235 mW

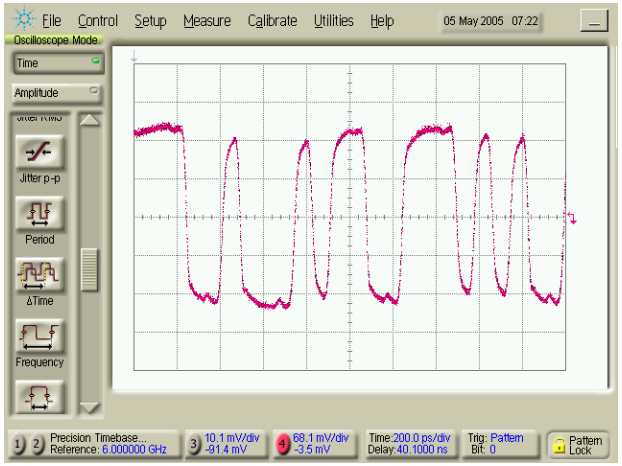
Measurement Setup

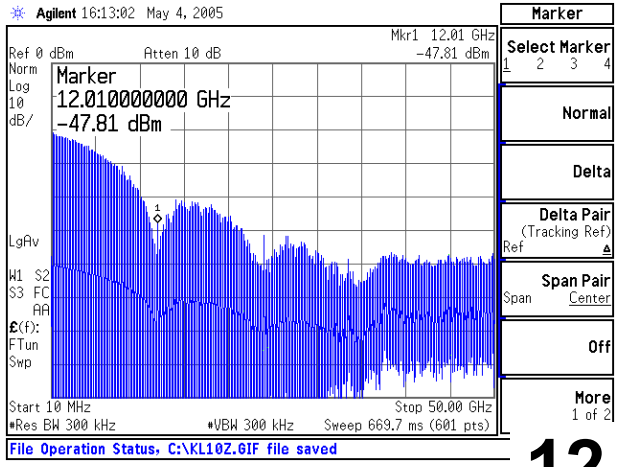
- Spectrum analyzer to verify tone spacing
- Oscilloscope capable of locking to PRBS

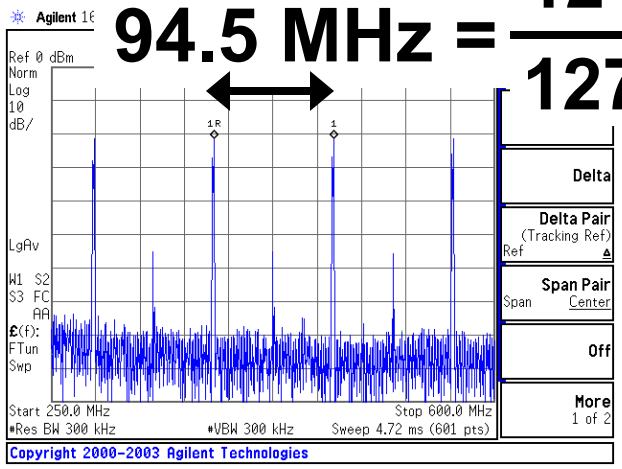


Experimental Results - 12 Gb/s



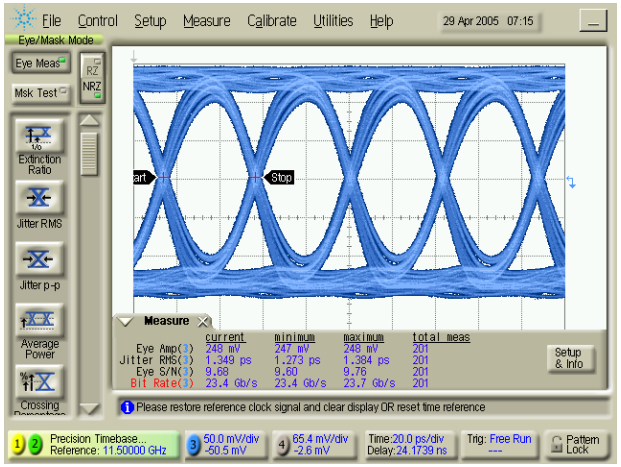


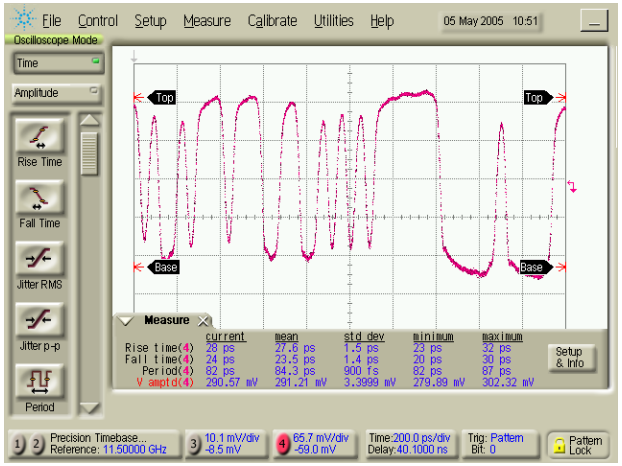


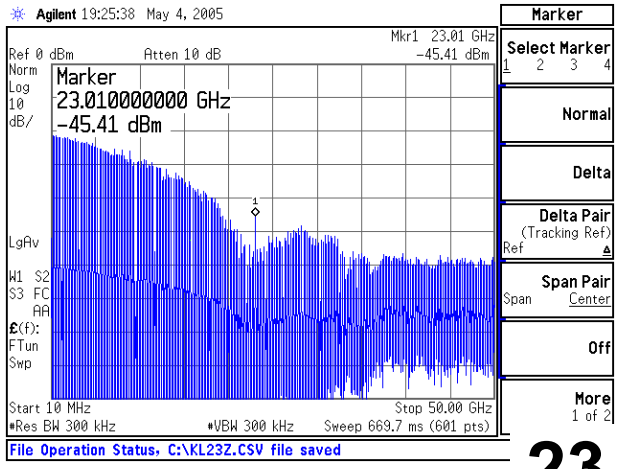


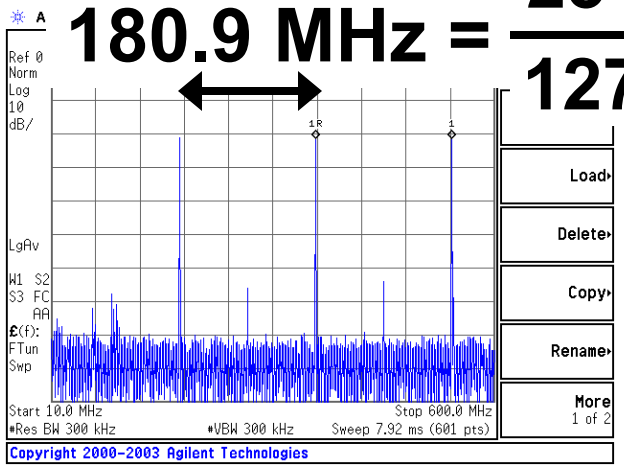
94.5 MHz = 12 Gb/s / 127 bits

Experimental Results - 23 Gb/s



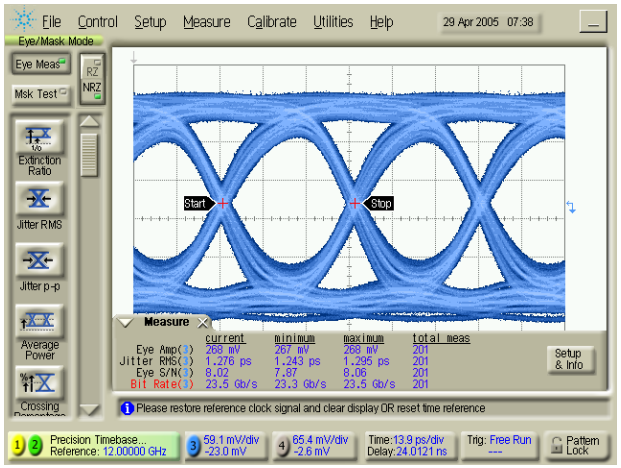


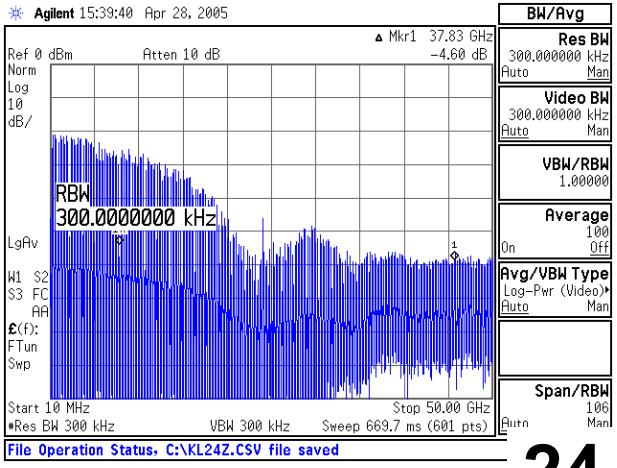


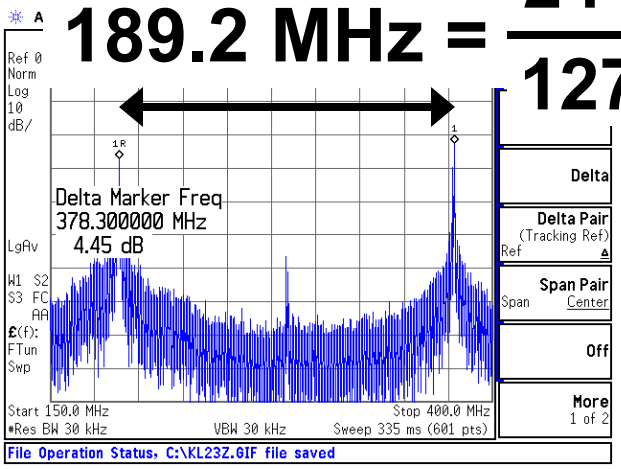


180.9 MHz = 23 Gb/s / 127 bits

Experimental Results - 24 Gb/s







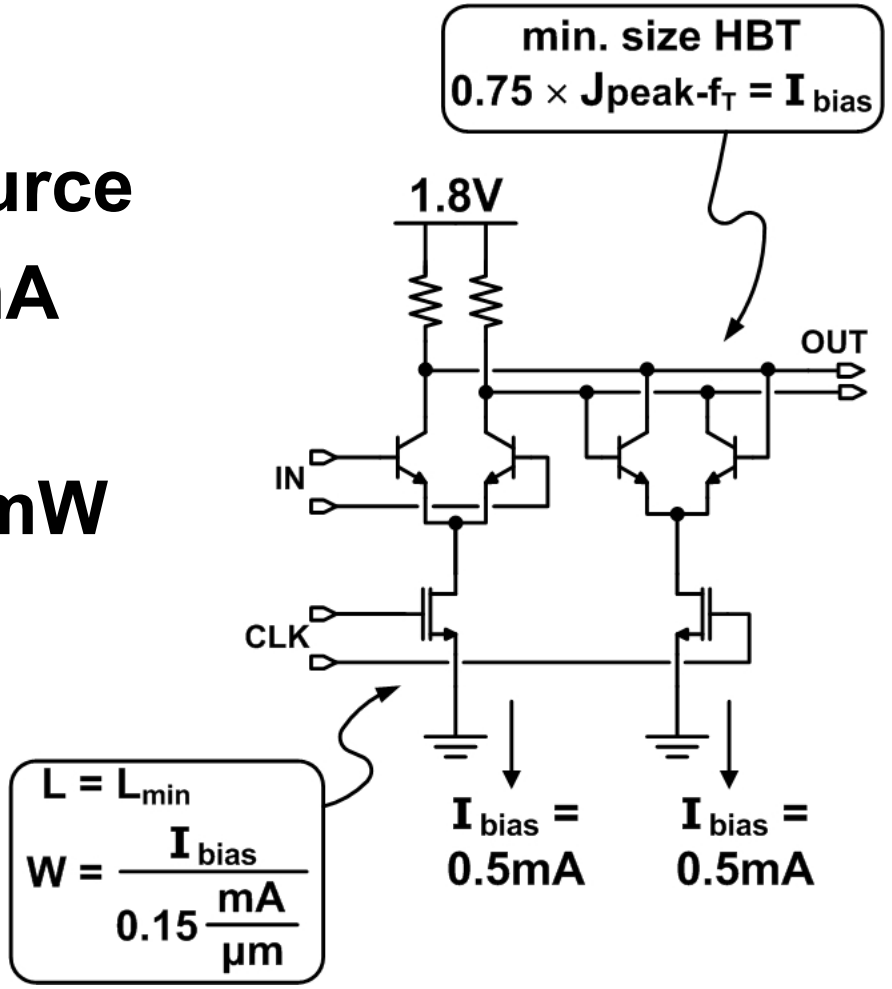
189.2 MHz = 24 Gb/s / 127 bits

- **Cannot guarantee error-free time-domain PRBS at 24 Gb/s**

Further Power Reduction

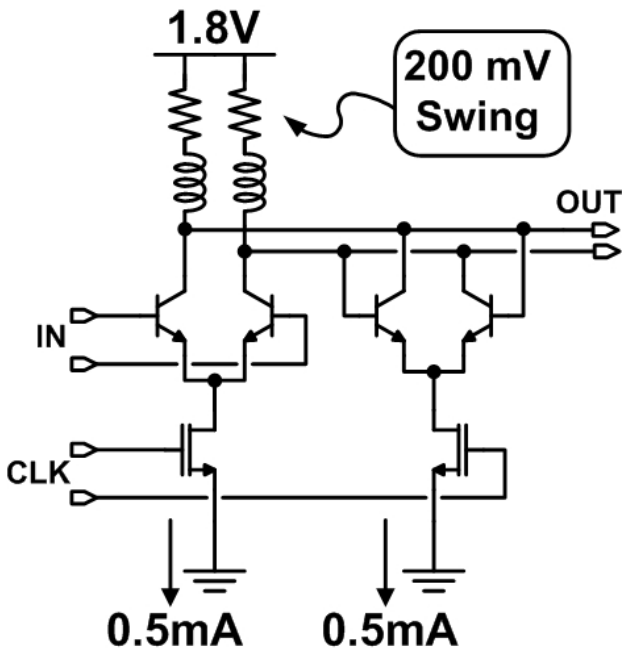
- Same technology
- Removed current source
- V_{DD} = 1.8 V, I_{total} = 1 mA
- Power reduced:

  2.5 mW → 1.8 mW
- Same speed: 12 GHz
- Simulated with extracted layout parasitics



Scaling to Next Tech. Node

- 90 nm SiGe BiCMOS [3]
- HBT f_T: 160 → 230 GHz
- MOS f_T: 80 → 120 GHz
- Same power: 1.8 mW
- f_T improvement: $\times \sqrt{2}$
- Inductive peaking: $\times$ 1.5
- ΔV reduced: $\times$ 1.3
- Speed increased : 12 GHz → 30 GHz
- Simulated with extracted layout parasitics



Summary

- **Presented a parallel architecture, 4-channel 2^7-1 PRBS generator**
- **Demonstrated a 2.5-mW 12-GHz latch in 0.13 µm SiGe BiCMOS process**
- **Investigated ways for power reduction**

Acknowledgements

- **The authors thank Bernard Sautreuil and Rudy Beerkens for their support**
- **STMicroelectronics for fabrication**
- **Micronet and CMC for CAD tools and support**
- **NSERC for financial support**

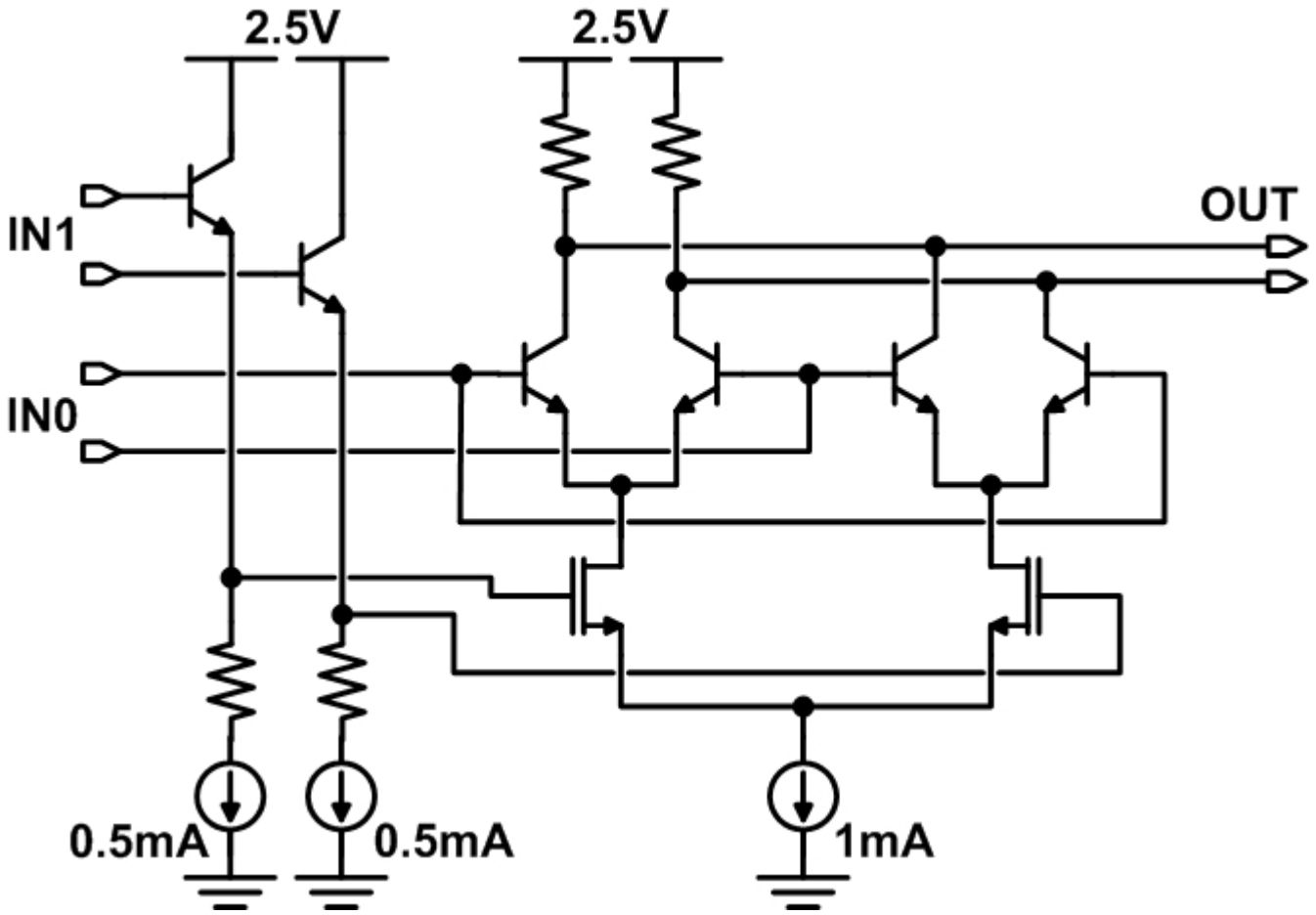
1. S. Kim, *et al.*, “45-Gb/s SiGe BiCMOS PRBS Generator and PRBS Checker,” in *CICC 2003*, pp. 313-316
2. T. Dickson, *et al.*, “A 2.5-V 45-Gb/s decision circuit using SiGe BiCMOS logic,” in *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 994-1003, Apr. 2005
3. P. Chevalier, *et al.*, “230 GHz self-aligned SiGeC HBT for 90 nm BiCMOS technology,” in *Proceedings of IEEE BCTM 2004*, pp 225-228

Thank you

Questions?

Back-up Slides

XOR Schematic



DFF Schematic