

A 1.2V, 60-GHz radio receiver with on-chip transformers and inductors in 90-nm CMOS

David Alldred, Brian Cousins, and Sorin P. Voinigescu
Edward S. Rogers Sr. Department of Electrical and Computer Engineering
University of Toronto
Toronto, ON, M5S 3G4, Canada
dave.allred@utoronto.ca, brian.cousins@utoronto.ca and sorinv@eecg.utoronto.edu

Abstract—This paper describes an integrated 60-GHz receiver in 90-nm CMOS including an LNA and downconversion mixer as well as LO and IF buffers. Transformer baluns are used for S/D conversion of the RF and LO signals to allow for conventional double-balanced mixing. The single-ended downconversion gain of a 60 GHz signal to a 5 GHz IF is 16 dB with an input compression point of -21 dBm while consuming 60 mW of power. The DSB noise figure is below 7 dB over the entire IF bandwidth which is greater than 1 GHz. The use of spiral inductors and transformers as matching elements resulted in a die area of only $600\ \mu\text{m} \times 475\ \mu\text{m}$ including pads.

Keywords—60-GHz radio; mm-wave receiver; CMOS mm-wave integrated circuits; inductors; transformers

I. INTRODUCTION

The desire for faster wireless data communication has turned attention to the 7-GHz unlicensed band around 60 GHz. This band is characterized by its limited propagation range due to oxygen absorption but offers a large amount of bandwidth and high interference isolation suitable for home and office applications.

Receiver front-ends in this frequency range have typically been realized using SiGe [1-2] or III-V technologies. Much of the recent work in CMOS mm-wave circuits focuses on the 0.13 μm node [3-4] and has yet to take advantage of the f_T and f_{MAX} improvements in 90-nm CMOS [5]. To date, only a low-noise amplifier (LNA) and a power amplifier have been reported in 90-nm RF-CMOS [6]. By presenting a receiver front-end which includes an LNA, doubly-balanced mixer, differential LO buffer and IF amplifier, this paper will further demonstrate the potential for integrating a 60-GHz radio transceiver in a standard CMOS process.

II. RECEIVER OVERVIEW

The block diagram of the mm-wave receiver front-end contains an LNA, mixer, LO buffer and 5-GHz IF buffer as shown in Fig. 1. It makes use of inductors and transformers rather than transmission lines or hybrid couplers to reduce area consumption as in [2]. The MOSFETS were biased at current densities between 0.15 mA/ μm and 0.2 mA/ μm which provide optimal NF_{MIN} and peak f_{MAX} , respectively, as described in [5]. All four circuit blocks were designed using straightforward topologies to be discussed in the following section.

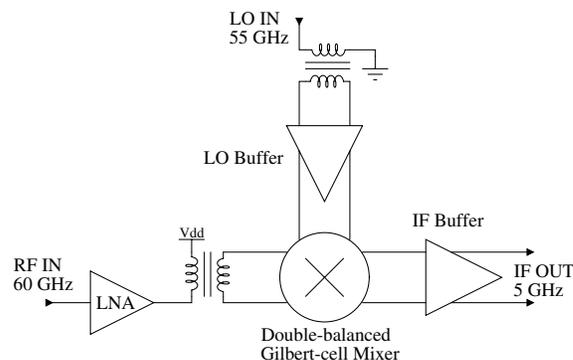


Figure 1. Receiver block diagram.

III. BUILDING BLOCKS

A. LNA

The LNA, adapted from [6], is a two-stage single-ended cascode found in Fig. 2. The inductors between the transistors in each stage absorb parasitic capacitance for increased gain over a broad bandwidth which extends beyond 60 GHz. The RF input is input impedance and noise-matched to 50 Ω by the proper sizing of the input transistor Q1 as well as its gate and source inductors. The load for the second stage is a single-ended-to-differential (S/D) transformer to interface with the downconvert mixer. The nominal current draw for the LNA is 14 mA and it can be adjusted externally via the gate bias voltages of Q1 and Q3.

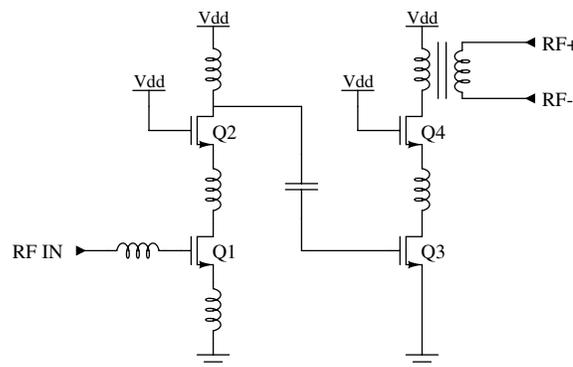


Figure 2. Two-stage cascode LNA schematic.

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B. Mixer

The mixer is realized with a double-balanced Gilbert cell as shown in Fig. 3. It consumes 6 mA with the gates of Q1 and Q2 biased by the voltage applied to the center-tap of the balun at the LNA output. The same mid-stage inductor design as in the LNA is employed to improve the conversion gain. The output is an LC tank with Q about 3-4 designed to resonate at the IF frequency of 5 GHz. It provides additional headroom compared to a resistive load while the low quality factor ensures a bandwidth of at least 1 GHz. The common-source inductor provides some common-mode rejection of the amplitude imbalance produced by inherent asymmetries in the high-frequency parasitics of the the balun. The symmetrical layout of the transistor quad, sharing a single well, and of the entire mixer was critical to ensure good isolation between ports.

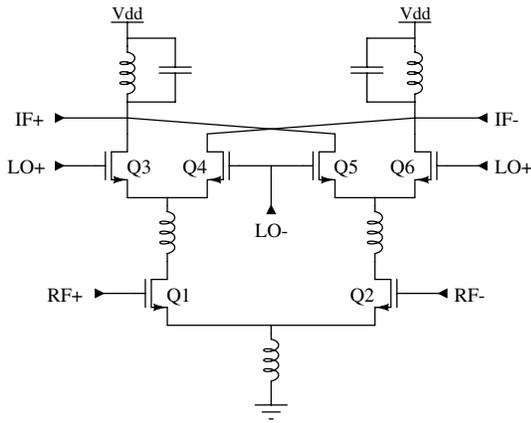


Figure 3. Schematic of double-balanced Gilbert cell mixer.

C. LO Buffer

The LO buffer consists of a differential CS stage as seen in Fig. 4. The LO buffer input conveniently features on-chip S/D conversion of the LO signal, which would otherwise be impractical to bring onto the chip differentially. Symmetry was also important in this block in order to provide the most balanced clock signal possible. The buffer is biased with a current source and draws 15 mA. The source inductor again adds some common-mode rejection since the current source does not present a high impedance at mm-wave frequencies.

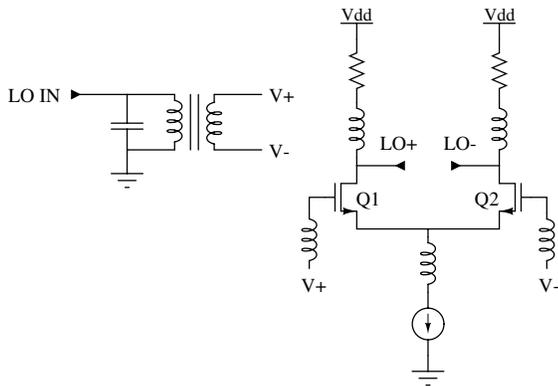


Figure 4. LO buffer schematic.

D. IF Buffer

The 5-GHz IF buffer provides additional gain and 50 Ω matching at the output for testing purposes. It uses a pair of single-ended CS stages to allow for maximum linearity as shown in Fig. 5. The inputs are capacitively coupled and the MOSFETs are sized and biased for highest linearity with a total drain current of 17 mA which corresponds to 0.3mA/ μ m.

E. Passives

The inductors were designed using the ASITIC software [7] and implemented in schematics using a $2-\pi$ model [8]. The transformer balun was modeled with the hybrid- π structure in Fig. 6 which was obtained by combining work from [9-11] to account for the distributed nature and the substrate coupling of the spirals. The balun exhibited a simulated insertion loss of 3.2 dB with an amplitude imbalance of 0.5 dB and negligible phase imbalance at 60 GHz. The amplitude imbalance is a result of the asymmetric nature of the input signal and capacitive coupling within the transformer.

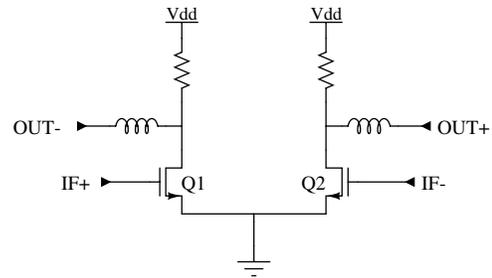


Figure 5. IF buffer schematic.

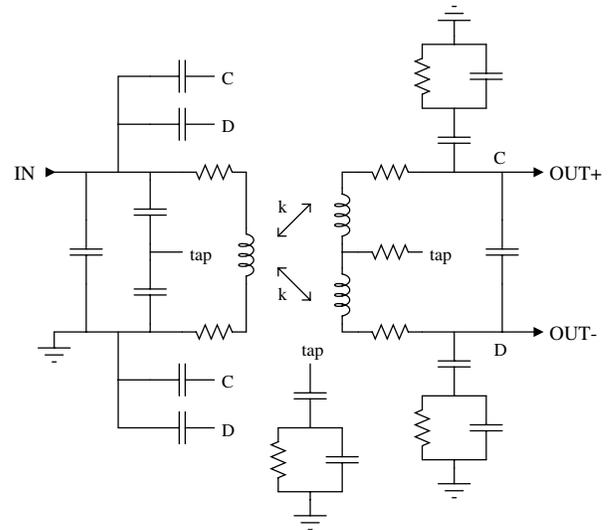


Figure 6. Balun transformer model schematic.

The final layout including pads occupies 0.6x0.48 mm² and is shown in Fig. 7. The RF and LO inputs are on the left and right sides, respectively, while the IF outputs are at the bottom.

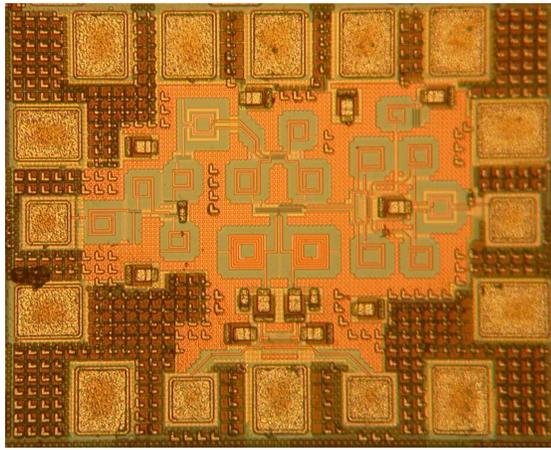


Figure 7. Die photo of receiver.

IV. EXPERIMENTAL

Most measurements were conducted using a 1.2V supply and an external VCO. The circuit draws 50 mA from 1.2V for a power consumption of 60 mW. The peak large-signal receiver gain of 21.5 dB occurs at about 53 GHz with a 3-dB bandwidth of greater than 5 GHz as shown in Fig. 8. The conversion gain from a 60 GHz RF to a 5 GHz IF is 16 dB. The input-referred 1 dB compression point is found to be -21 dBm for a 60 GHz input in Fig. 9.

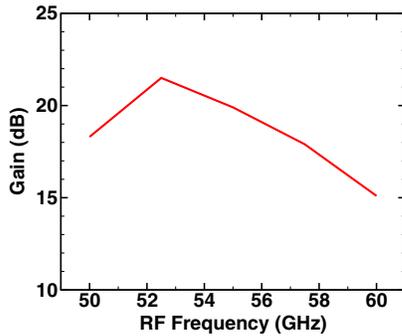


Figure 8. Measured receiver gain to 5 GHz IF.

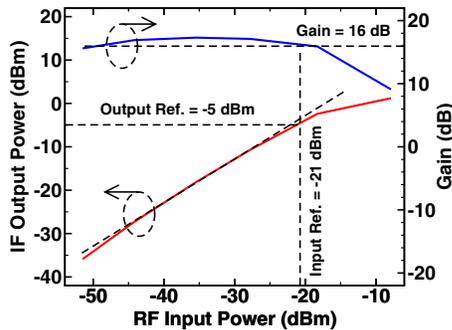


Figure 9. Measured P_{1dB} with 60 GHz RF input.

The IF output exhibits a bandwidth of over 1 GHz as illustrated in Fig. 10. The double sideband noise figure (NF_{DSB}) is < 7 dB over a 2 GHz IF band, and is found in Fig. 11 for supply voltages between 1.1 V and 1.5 V. The NF_{DSB}

was measured by applying a 50-75 GHz noise source to the RF input and observing the single-ended excess noise factor (ENF) at the IF output with an HP-8970B noise meter. The lowest DSB NF value is 5 dB at 59 GHz and V_{DD} of 1.5V.

Isolation from LO to RF was measured with a spectrum analyzer and is better than 90 dB (Fig. 12) illustrating the effectiveness of the symmetrical layout and baluns.

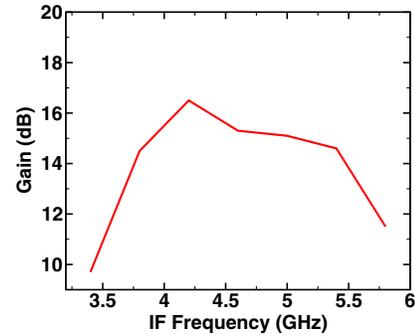


Figure 10. Receiver gain with 55 GHz LO.

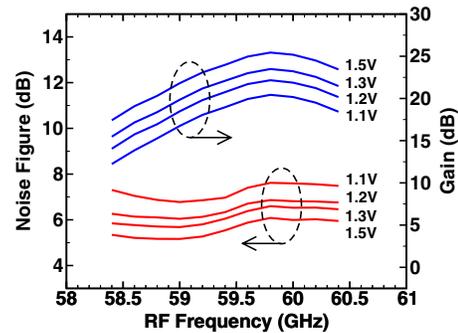


Figure 11. Measured NF and gain for various VDD.

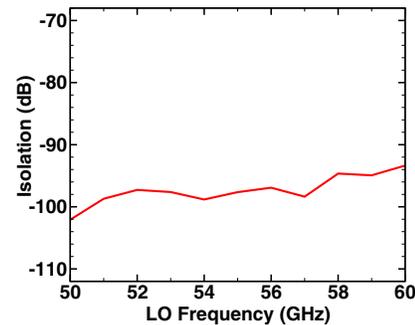


Figure 12. Measured LO-RF isolation.

Fig. 13 shows the measured NF and gain vs. LO power and reveals rapid performance degradation for LO power levels below 1.5 dBm. A plot of receiver NF_{DSB} vs. the V_{GS} of transistor Q1 in the LNA (Fig. 14) confirms for the first time at 60 GHz that the minimum noise figure bias of a MOSFET is slightly less than where the peak f_{MAX} (gain) bias occurs.

The return loss of the RF input of the receiver (Fig. 15) is better than -12 dB from 49-58 GHz and still below -10 dB at 60 GHz. It can be seen that the real part of the input impedance is 50Ω at almost exactly 60 GHz but the imaginary part crosses

zero at only 46 GHz. The estimated pad capacitance value of 30 fF used in the design is partly to blame since measurements have shown it to be closer to 20 fF. This impedance mismatch certainly contributes to the 9% lower than expected center frequency of the receiver. Otherwise, all of the results are very close to the simulated values shown in Table 1.

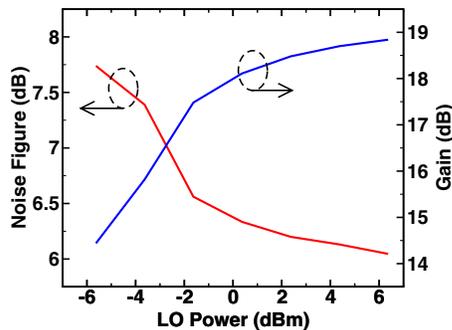


Figure 13. Measured NF and gain vs. LO power.

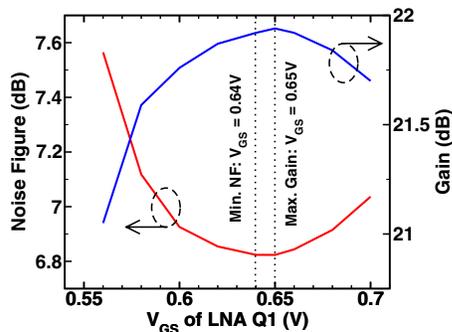


Figure 14. Measured NF and gain vs. V_{GS} of LNA Q1.

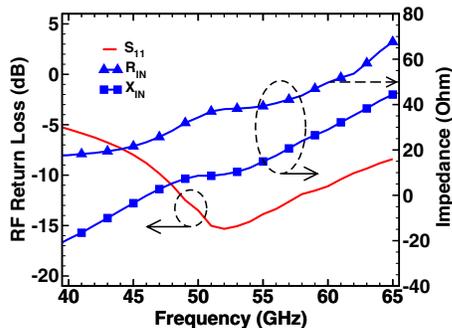


Figure 15. Measured S_{11} and impedance of the RF input of the receiver.

V. CONCLUSION

This work shows that conventional circuit topologies and design techniques can be applied at 60 GHz to realize a small form-factor receiver with < 7 dB noise figure and > 15 dB gain in the 90-nm CMOS node. The use of on-chip transformers and inductors resulted in a die area of less than 0.3 mm^2 . Table 1 indicates that the receiver has comparable noise figure and lower power than those realized in (210-GHz) SiGe HBT technology. This demonstrates the feasibility of integrating mm-wave blocks in standard CMOS to cost-effectively exploit the unlicensed band around 60 GHz.

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TABLE I. COMPARISON OF SILICON MM-WAVE RECEIVERS

Technology	0.18 μm SiGe BiCMOS	0.13 μm CMOS	0.13 μm SiGe BiCMOS	0.09 μm CMOS	0.09 μm CMOS Simulated
Frequency	65 GHz	60 GHz	60 GHz	60 GHz	60 GHz
Integration Level	LNA, mixer, VCO, IF amplifier	LNA, mixer, IF buffer	LNA, superheterodyne receiver, BB amplifier	LNA, mixer, LO and IF buffer	LNA, mixer, LO and IF buffer
Power Gain	24 dB	28 dB [V/V]	40 dB	16 dB	21 dB
NF _{MIN}	12 dB	12.5 dB	5 dB	7 dB	7.4 dB
P _{1dB}	-22 dBm	-22.5 dBm	-36 dBm	-21 dBm	-20 dBm
P _{diss}	540 mW	9 mW (excluding IF buffer)	195 mW	60 mW	62.5 mW
Isolation (LO-RF)	--	--	< -77 dB	< -90 dB	-120 dB
Area	0.79x0.74 mm ²	0.4x0.3 mm ² (no pads)	3.4x1.7 mm ²	0.6x0.48 mm ²	0.6x0.48 mm ²
Reference	[2]	[3]	[1]	This work	This work