

SiGe HBT Technology: Device and Application Issues

D.Harame, L.Larson[‡], M.Case[‡], S.Kovacic[†], S.Voinigescu[†], T.Tewksbury[×], D.Nguyen-Ngoc, K.Stein, J.Cressler[#], S.-J.Jeng, J.Malinowski, R.Groves, E. Eld, D. Sunderland, D.Rensch[‡], M.Gilbert, K.Schonenberg, D.Ahlgren, S.Rosenbaum[‡], J.Glenn[§], and B.Meyerson

IBM Microelectronics Div., B630:EM1, Hopewell Jct., NY, 12533, (914)-892-3863, FAX (914)-892-4604

[‡]Hughes Electronics, [†]Northern Telecom, [×]Analog Devices Inc., [#]Auburn University, and [§]Delco Electronics

ABSTRACT

SiGe HBT Bipolar/BiCMOS technology has a unique opportunity in the wireless marketplace because it can provide the performance of III-V HBTs and the integration/cost benefits of silicon bipolar/BiCMOS [1]. This paper will review the status of IBM's SiGe HBT technology particularly focusing on some key device and application issues for high frequency circuit applications. In this work we review graded-base SiGe HBTs optimized for analog circuits and address four key issues: 1) BV_{ceo} constraints, 2) Transmission line loss, 3) Noise performance, and 4) Process integration leverage and issues. All of the hardware results are for self-aligned, polysilicon emitter, graded-base SiGe HBTs fabricated in a 200mm semiconductor production line [2] using the UHV/CVD technique for film growth.

INTRODUCTION/TECHNOLOGY STATUS

As SiGe HBT technology has matured, the emphasis has shifted away from device performance demonstrations towards producing a practical technology with passive elements and complementary devices. Many of the applications opening up in optical networks and wireless RF technology require performance specifications in the 1-20 GHz frequency range which are difficult, at this time, to achieve with conventional CMOS and Bipolar technologies. Most of these applications are possible with SiGe HBT technology as evidenced by recent publications of optical circuits for 20 Gb/s optical networks [3] and RF wireless circuits for 1-24 GHz applications [4-7]. The availability of SiGe HBT BiCMOS technology [8] with both very high performance HBTs ($f_{max} = 60$ GHz) and $0.25\mu\text{m}$ L_{eff} CMOS for logic and memory offers the possibility of combining analog and digital components on the same chip. While SiGe HBT technology continues to look promising for a wide variety of analog mixed signal applications, there are still remaining issues which must be resolved. The characteristics of a SiGe HBT optimized for analog circuit design and the associated technology elements are summarized in Tables 1 and 2,

respectively. These tables reflect recent noise figure, radiation tolerance, and temperature dependence measurements, as well as the addition of several technology elements. The extensive device list now available for analog circuit designers, without any degradation in the performance features of the SiGe HBT, is a recent development for the technology. The combination of the speed of the SiGe HBT, the presence of the support technology elements, and the integration capabilities may well give circuit designers more flexibility and result in new "single chip" system architectures.

BREAKDOWN VOLTAGE ISSUES

The first key issue is whether SiGe HBT microwave power output is severely limited by the chosen 3.3 volt BV_{ceo} design point. While the graded-base will increase the BV_{ceo} value for a given f_T , BV_{ceo} will always be lower than the 6-8 volt values achieved in III-V HBTs. Fortunately, the 3.3 volt BV_{ceo} is NOT a significant power limitation for commercial/consumer products, especially portable ones, that operate at 3.3 volt supply voltage. Furthermore, it is not BV_{ceo} but

Table 1. Summary of SiGe HBT Characteristics.
(Data assembled from different hardware lots)

Parameter	Comment (Std. Device $A_E = 0.5 \times 2.5 \mu\text{m}^2$)
Speed	$f_T \approx 45-50$ (GHz) $f_{max} > 60$ (GHz)
Breakdown	$BV_{ceo} = 3.3$ (V) @ $\beta = 100$, $BV_{cbo} = 9.5$ (V)
Base Resistance	$R_{BI} \approx 7-10$ (k Ω /□), Maximum $r_{bb} \approx 80-120$ (Ω)
Yield	> 85% on 4K Tx chains ($A_E = 4000 \times 0.5 \times 2.5 \mu\text{m}^2$)
1/f Corner Noise Freq.	SiGe HBT = 373 (Hz), Si BJT = 480 (Hz) ($A_E = 0.5 \times 10 \times 3 \mu\text{m}^2$, $I_b = 2.25 \mu\text{A}$) [9].
Radiation Tolerance	Δ in peak $\beta = 8\%$ at 2 (Mrad(Si)) [10]
Temperature dependence	β (25°C) = 256 -> β (125°C) = 240, f_T (25°C) = 52 -> f_T (125°C) = 43, ($A_E = 0.5 \times 2.5 \mu\text{m}^2$, $R_{BI} = 18 \text{k}\Omega/\square$)

**Table 2. SiGe HBT Technology Elements
(Data taken from different hardware lots)**

Element	Comment
Resistors	Polysilicon = 320 (Ω/\square), 1/I = 2.0 (k Ω/\square)
Substrate Contact	80 (Ω) per 2x10 μm^2 contact area.
BiCMOS nFET ($L_{\text{eff}}=0.25\mu\text{m}$)	$g_{m,\text{sat}} = 260$ (mS/mm), $V_{t,\text{lin}} = 0.54$ (V) $T_{\text{ox}} = 70$ (\AA), 2.5 volt operation
BiCMOS pFET ($L_{\text{eff}}=0.25\mu\text{m}$)	$g_{m,\text{sat}} = 130$ (mS/mm), $V_{t,\text{lin}} = -0.55$ (V) $T_{\text{ox}} = 70$ (\AA), 2.5 volt operation
LPNP @10 μA	$\beta = 17.2$, $G_M = 350$ (μS) ($W_b = 0.5\mu\text{m}$, $P_e = 6\mu\text{m}$)
Precision Cap. Metal/Ins./Metal	$C = 1.0$ fF/ μm^2
6-Turn Spiral Inductors	$Q = 2-3$ on p-/p+ wafers (0.7-1 GHz) $Q = 8-10$ on p- wafers (0.9-2 GHz)
Diodes	ESD, PIN, Varactor

BV_{cer} (defined as BV_{ceo} measured with a resistor between emitter and base) which is of importance in circuits with transistor bias networks. Even when the bias resistor is as large as 2 M Ω , the breakdown voltage will shift from BV_{ceo} (3.3 V) to BV_{cbo} (10 V) as shown in Fig. 1. In addition, the microwave/RF voltage swing can exceed the BV_{ceo} limits by several volts; this is a well known phenomenon in Si power BJT circuits [11]. This is shown in the load pull measurements in Fig. 2 where the AC voltage excursion exceeds BV_{ceo} by 2 V. This single stripe device yields 60 mW output power (Power Density = 6 mW/ μm^2) at 70% efficiency at 900 MHz which is higher than that reported for III-V HBTs [12]. The weak temperature dependence of DC (β) and AC (f_T) parameters (see Fig. 6) is an additional advantage when using graded-base SiGe HBTs in power amplifiers.

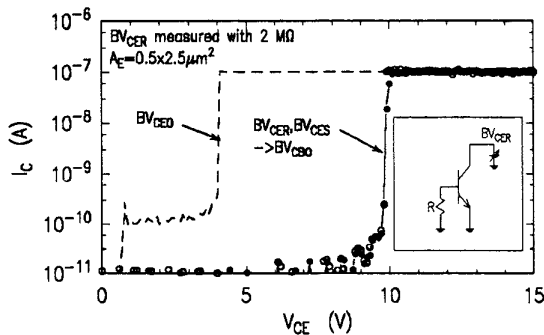


Fig. 1. Collector current versus collector-emitter voltage for three configurations: open base (BV_{ceo}), base-emitter shorted (BV_{ces}), and base-emitter shorted by a 2 M Ω resistor (BV_{cer}).

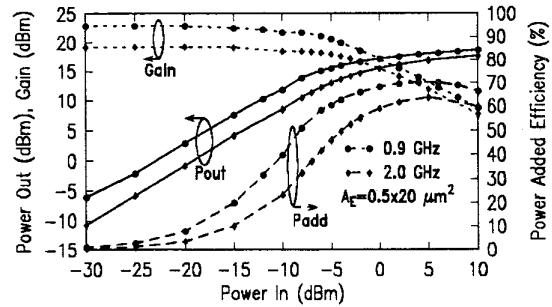


Fig. 2 Load pull measurements for transistors biased at $V_{\text{cc}} = BV_{\text{ceo}}$, $I_C = I_C$ at peak f_{max} . AC voltage excursion exceeds BV_{ceo} by 2 V.

MICROWAVE TRANSMISSION LINE LOSSES

The second key issue is whether microwave transmission line losses caused by the conductive silicon substrate will limit the high frequency response of SiGe HBT monolithic circuits. Several groups have explored the use of high-resistivity Si-substrates for the realization of SiGe MMICs, but very high resistivities ($> 20 \Omega\text{cm}$) are required [13-14] and there are significant processing problems associated with such wafers (specifically slip dislocations and warpage). Moderate resistivities (10-20 $\Omega\text{-cm}$) can be used to improve operation for 0.9-2.4 GHz applications with conventional interconnect technology. Fig. 3 shows inductance and Q for 6 turn inductors fabricated on 10-18 Ωcm p- wafers and wafers with 6 μm p- epi on p+ substrates. Although the inductor Q is improved from 2-3 to 8-10 by using p- substrates, the self-resonant frequency remains below 3 GHz, therefore limiting circuit applications to below 3 GHz.

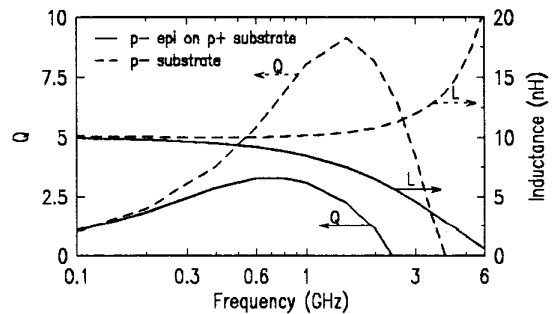


Fig. 3 Inductance and Q of a 6 turn inductor on 10-18 Ωcm wafers and 6 μm p- epi on p+ substrates.

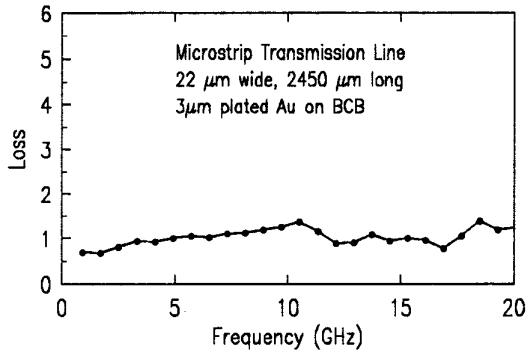


Fig. 4 Microstrip transmission line: 3 μm plated Gold, 22 μm wide, 2450 μm long on 13 μm BCB.

For higher frequency applications, we have explored the use of thick dielectric layers - physically separating the transmission lines from the substrate - as an alternative to high resistivity Si. This technique, which has been pursued by a number of groups, includes thick SiO_2 [15] and polyimide [16] approaches. Our SiGe HBT MMIC technology employs a 13 μm thick Benzocyclobutene (BCB) layer [17] with a final plated layer of gold on top of the BCB. Computer modeling of transmission line losses was employed to determine the optimum BCB thickness, and the losses were measured for a 50 Ω microstrip transmission line as a function of frequency. These are shown in Fig. 4. The loss is less than 1.5 dB/cm up to 20 GHz, which is comparable to semi-insulating GaAs substrates, and an order of magnitude lower than conventional silicon substrates. Fig. 5 shows the inductance and Q of a 2-turn inductor fabricated on BCB. The resonant frequency is beyond 15 GHz.

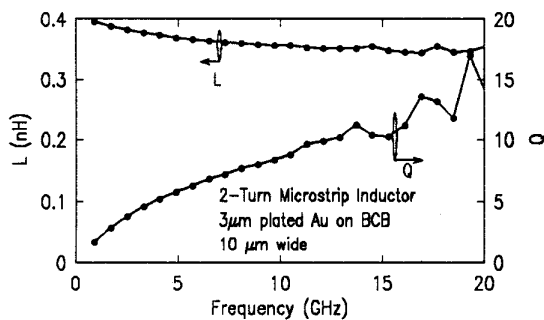


Fig. 5 Inductance and Q versus frequency for a 2-Turn 3 μm plated, 10 μm wide inductor.

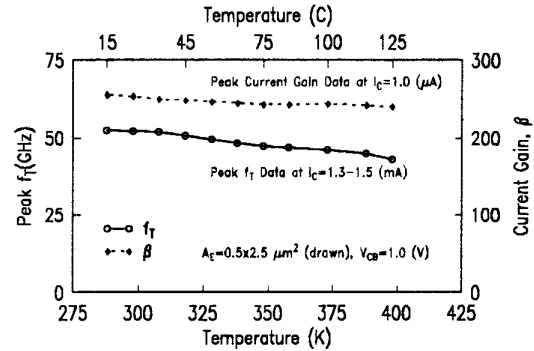


Fig. 6 Current Gain and Cutoff Frequency versus Temperature for a Polysilicon Emitter graded-base SiGe HBT.

BROADBAND AND LOW FREQUENCY NOISE

The third key issue is whether acceptable broadband and low frequency noise is achievable in graded-base SiGe HBTs, despite the intrinsic base sheet resistances being an order of magnitude higher than that found in III-V HBTs. The SiGe HBT uses minimum geometry and self-alignment to achieve low base resistance, which is the main factor in achieving a low noise figure. Peak base resistances as low as 80 Ω for transistors with standard layouts and $0.5 \times 2.5 \mu\text{m}^2$ emitter area are easily achievable and comparable to that found in III-V HBTs. Noise figure measurements on discrete devices, ($A_E = 2 \times 0.5 \times 20 \mu\text{m}^2$) have yielded less than 1 dB with 15 dB associated gain at 2.5 GHz as shown in Fig. 7. In addition, $1/f$ noise corner frequency values of 373 Hz for SiGe HBTs and 480 Hz for Si BJTs have also been achieved. These values are superior to GaAs HBTs (Fig. 8).

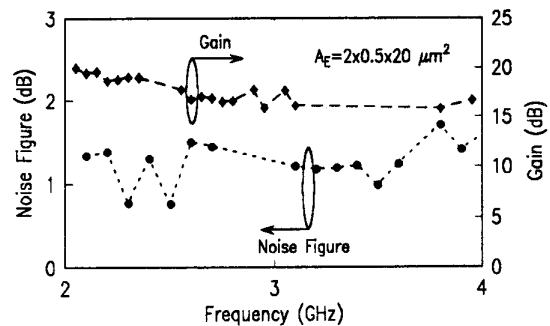


Fig. 7 Noise figure and associated gain for Si BJT with identical processing to the SiGe HBT.

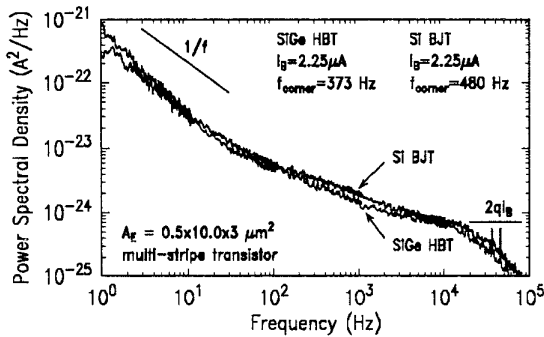


Fig. 8 Noise Power Spectral Density at a base current of 2.25 μA for multistriple Si and SiGe transistors with an emitter area of $0.5 \times 10 \times 3.0 \mu\text{m}^2$ and comparable doping profiles [9].

PROCESS INTEGRATION LEVERAGE

Finally, we address the issue of process integration leverage. High levels of integration have leverage if both performance and yield are uncompromised. Recent BiCMOS results demonstrate good yield on fully functional 64K CMOS SRAMs [8] for the CMOS and good yield on 4K transistor chains ($A_E = 4000 \times 0.5 \times 1.0 \mu\text{m}^2$) (See Fig. 9). High frequency measurements on the same wafers confirm the HBT performance with $f_T = 40 \text{ GHz}$ and $f_{\text{max}} = 60 \text{ GHz}$ and the CMOS performance with 50 ps unloaded gate delays for $0.25 \mu\text{m}$ L_{eff} and 64K CMOS SRAM access time of 4.5 ns (Fig. 10). This combination of performance and yield in both the SiGe HBT and CMOS devices opens many possibilities in system design and may well lead to novel system architectures.

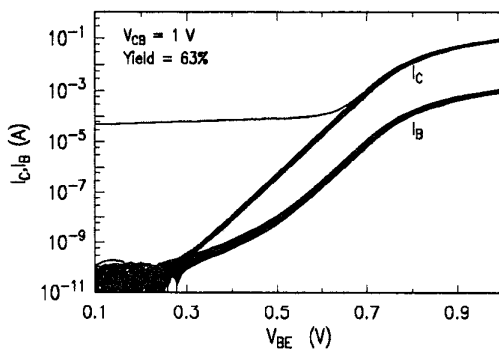


Fig. 9 Gummel plot of 44 test sites of 4,000 transistor chain of individual emitter area $0.5 \times 1.0 \mu\text{m}^2$ transistors.

SUMMARY

This review paper has focused on some key device and application issues for graded-base SiGe HBT technology and presented solutions with circuit results or

device measurements. Cross talk between analog and digital portions of integrated circuits was indicated to be largely unaddressed and an important factor that could limit the extent of integration ("single chip solutions") particularly for SiGe HBT BiCMOS technology. SiGe HBT Bipolar/BiCMOS technology provides an excellent technical solution to a large number of analog, mixed-signal, and wireless applications for today's market needs.

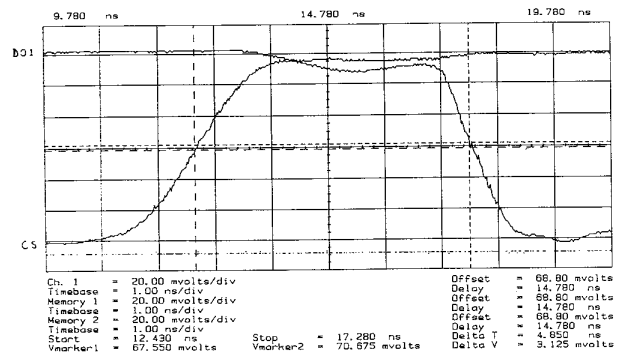


Fig. 10 64K CMOS SRAM Reading Access Time Measurement (1 ns/Div). SRAM was fabricated on a BiCMOS wafer with functional analog bipolar circuits [8].

ACKNOWLEDGEMENTS

The authors would like to thank the IBM Microelectronics Division Advanced Semiconductor Technology Center for help in fabricating these devices.

REFERENCES

- [1] D. Harame, et. al., Trans. Elect. Dev., Vol 42, March 1995, pp. 455-482.
- [2] IBM Microelectronic Division, Advanced Semiconductor Technology Center, E. Fishkill, New York
- [3] F. Sato, et. al., 1995 BCTM Proceedings, pp. 82-88.
- [4] W. Gao et. al., 1995 BCTM Proceedings, pp. 166-169.
- [5] J. Glenn, et. al., 1995 BCTM Proceedings, pp. 186-189.
- [6] H. Schumacher et. al., 1995 BCTM Proceedings, pp. 190-193.
- [7] M. Case, et. al., 1995 BCTM Proceedings, pp. 121-124.
- [8] D. Nguyen Ngoc, et. al., 1995 BCTM Proceedings, pp. 89-92.
- [9] L. Vempati, et. al. 1995 BCTM Proceedings, pp. 129-132.
- [10] J. Babcock, et. al., presented at NSREC, 1995.
- [11] F.H. Raab, IEEE Trans. on Ckts. and Systems, Vol 24, 1977, pp. 725-735.
- [12] B. Bayraktaroglu, Proc. of the IEEE, Vol. 81, 1993, p. 1762.
- [13] J. Luy, et. al., IEEE Trans. on Microwave Theory and Tech., Vol. 43, No. 4, April 1995, pp. 705-713.
- [14] J. Buchler, et. al., IEEE Trans. on Microwave Theory and Tech., Vol. 43, pp. 1516-1521, 1986.
- [15] H. Sakai, et. al., IEEE MTT Symposium, 1994, pp. 1763-1766.
- [16] P. Chinoi, et. al., IEEE Trans. on Components, Hybrids, and Manuf. Tech., Vol 16, No. 7, Nov. 1993, pp.714-719.
- [17] U. Dahlgren, et. al., 1994 ICEMM, Denver Colorado.