Process- and Geometry-Scalable Bipolar Transistor and Transmission Line Models for Si and SiGe MMICs in the 5-22GHz Range

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Abstract

Statistical transistor and transmission line models are developed and verified on Si bipolar and SiGe HBT technologies through 22GHz. Universal best/worst process files are defined using principal component analysis and verified on the high frequency performance of transistors, CML delay chains, 5.8GHz cascode LNA (NF=2dB, G=10dB, P_{diss}=9mW) and broadband amplifier (G=9dB, B_{3dB}=22GHz, S_{11}<-20dB, NF=6dB, P_{1dB}=12.5dBm, group delay ripple < 8ps).

Introduction

As illustrated in Fig.1, even above 26GHz, IBM's SiGe HBTs deliver 5-6dB gain with a minimum noise figure less than 4dB. Such performance has traditionally been the hallmark of III-V HBTs. For reference, Fig.2 compares the cutoff frequency f_T of bipolar technologies. The Si bipolar and GaAs HBT technologies are from NORTEL. Also shown is the projected requirement for InP HBTs suitable for future fiber-optic long-haul systems. In the microwave range Si substrate losses and resistive and inductive interconnect parasitics start to play a comparable role to transistor speed and can seriously degrade circuit performance. Therefore, a design environment relying on statistical process- and geometry-scalable lossy transmission line as well as transistor [1] models has been developed for, and for the first time verified on the high frequency performance of, Si bipolar and SiGe HBT MMICs.

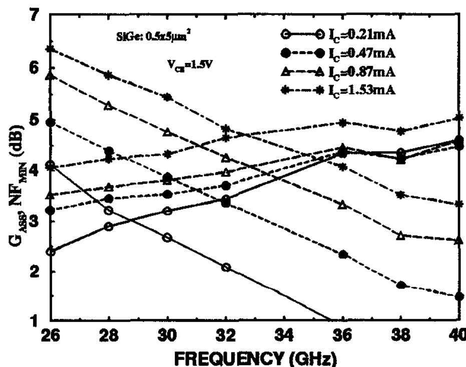

Fig.1: Measured minimum noise figure and associated gain for SiGe HBTs using an ATN NP-5 noise parameter test set.

Process-Scalable Transmission Line Models

Transmission lines models are central for the accurate simulation of Si-based circuits operating above 10GHz. While not desirable as circuit matching elements due to their losses, microstrip lines over the Si substrate occur inevitably as interconnect. We have developed an analytical process- and geometry-scalable model for metal-over-substrate microstrip lines which is employed to extract interconnect parasitics as transmission lines rather than as lumped capacitances. The HSPICE equations, based on [2-4], are given below and the corresponding lumped equivalent circuit is shown in Fig.3.

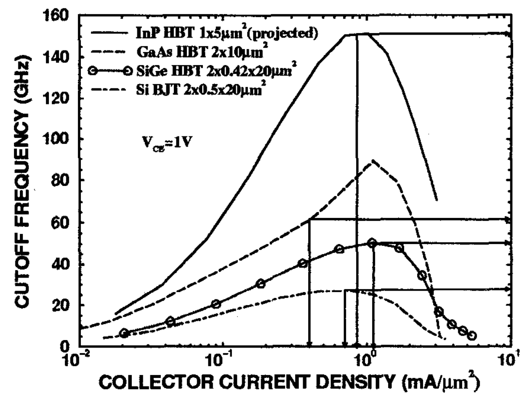

Fig.2: Measured f_T for state-of-the-art Si, Si/SiGe/Si, InGaP/GaAs and projected for InP/InGaAs/InP bipolar transistors.

```
.subckt M3S IN OUT GND w=2.4u l=200u
.param th = Nm3th  ht = Nm3ht Dself = '0.2235*(w+th)'
+ param1 = 'log((l/Dself)+sqrt(1+((l**2)/(Dself**2))))'
+ Lself = 'Lcor*l*(param1-sqrt(1+(Dself**2)/(l**2))+(Dself/l))'
+ Dmut = '(Nsubht+ht)*2'
+ param2 = 'log((l/Dmut)+sqrt(1+((l**2)/(Dmut**2))))'
+ Lmut = '2e2*l*(param2-sqrt(1+(Dmut**2)/(l**2))+(Dmut/l))'
+ L = '(Lself-Lmut)*1e-9'   R = 'Nm3r*(l/w)*(1+k*(f/1e9)**0.5)'
+ Cox = 'ε_rox*ε_o*l*(1.15*(w/ht)+Cfringe*((th/ht)**0.222))'
+ Csi = 'Csil*(l/1000u)' Rsi = 'ε_rSi*ε_o*Nsr/Csi'
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where w and l are the width and length of the line, and Nm3th, Nm3ht, Nm3r, Nsr and Nsubht are the M3 thickness, the oxide thickness between M3 and the Si substrate, the M3 sheet resistance, the resistivity of the Si substrate, and the Si substrate thickness, respectively, all defined as statistically independent process variables. Lcor, Cfringe, Csil and k are process-specific fitting parameters. Fig.4 demonstrates excellent agreement between measurements and simulations. For long controlled-impedance transmission lines, either M3-over-M1 or M3-over-polysilicon microstrip lines are recommended due to reduced loss. As illustrated in Fig.5, the latter allow for characteristic impedances as high as 100Ω with the least losses. High impedance lines are critical to achieving low-power on-chip clock and signal distribution.

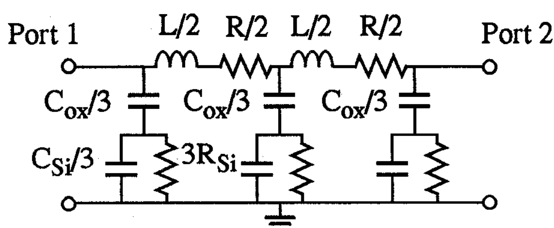

Fig.3: Lumped circuit for M3-over-substrate microstrip lines valid for line lengths of up to 1mm.

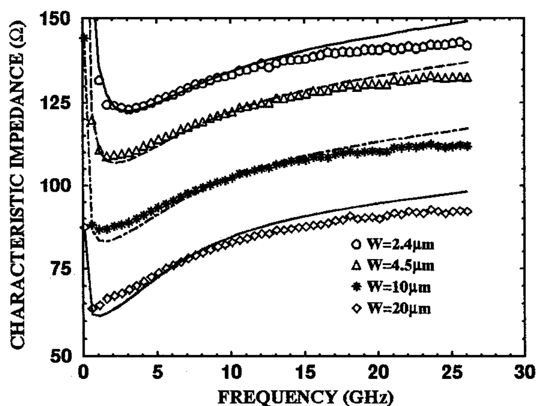

Fig.4: Measured (symbols) and simulated (lines) characteristic impedance for M3-over-substrate microstrip lines of various widths on a SiGe wafer.

Process-Scalable Transistor Models

In addition to geometry scaling, extensively verified in [1], vertical doping profile scaling is applied in this paper to the main dc and ac parameters of the SPICE Gummel-Poon bipolar transistor model, as well as on the breakdown voltage BV_{CBO}. Some of the process scaling equations listed below are based on those developed for the HICUM model [1,5].

$$C_{JE(A,P)} \sim NPbr^{-MJE(A,P)} \qquad C_{JCI} \sim Ncr^{-MJCI}$$

$$C_{JS} \sim Nsr^{-MJS} \qquad TF \sim NPbr^{-0.32} \qquad ITF \sim Ncr^{-1}$$

$$IS \sim NPbr \qquad IRB \sim NPbr^{-1} \qquad IKF \sim NPbr^{-0.69}$$

$$BVCBO \sim Ncr^{-0.5} \qquad RBX \sim NPbrx \qquad RBX \sim NWsp$$

NPbr, Ncr, NPbrx, and NWsp are the normalized pinched base resistance, normalized collector resistivity, external base sheet resistance and emitter oxide spacer width, respectively.

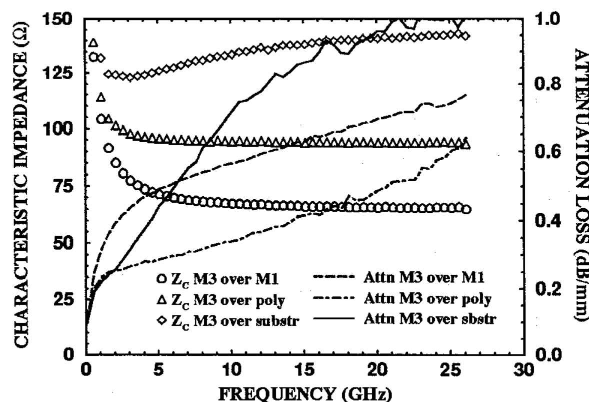

Fig.5: Measured characteristic impedance and attenuation loss of 2.4μm wide M3-over-substrate, M3-over-M1, and M3-over-polysilicon microstrip lines.

While statistical bipolar models are useful in estimating performance margin and yield [6,7], the run-time required for a meaningful number of Monte Carlo simulations becomes prohibitive for large circuits. In many instances, physically defined corner process files would provide almost as much insight into the manufacturability of a design as a full-blown Monte Carlo analysis at only a fraction of the simulation cost. To that end, principal component analysis is used here to define corner (best/fast and worst/slow case) process files that are relevant for both digital and microwave bipolar circuit performance and allow for meaningful sigma-sweep simulations. The"best" process corner definition is based on simultaneously achieving maximum f_T, f_{MAX} and minimum noise figure NF_{MIN}. For example, according to the data in Figs. 6 and 7, the sigma sign for pinched base resistance should be "+", while that for the emitter spacer width ought to be "-", as shown in the HSPICE implementation below.

```
xPbr = agauss(9K, 3K, 3)     NPbr = 'xPbr + 3K*sigma/3'
xWsp = agauss(0.2u,0.03u,3) NWsp = 'xWsp - 0.03u*sigma/3'
```

A "+" sign indicates that, as a particular process variable drifts towards larger values, the process becomes "better" or "faster". All independent process variables are treated in this manner. Measurements carried out across Si bipolar batches over the last two years, and more recently over SiGe wafers, were used to confirm that the above best/worst case

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definition simultaneously applies for f_T (Fig.8), f_{MAX}, CML delay (Fig. 9), and power gain of broadband amplifiers (Fig. 10). In the case of tuned circuits, such as the cascode LNA, "best" and "worst" translated into higher, and respectively, lower tuned frequency, as shown for the input return loss in Fig.11

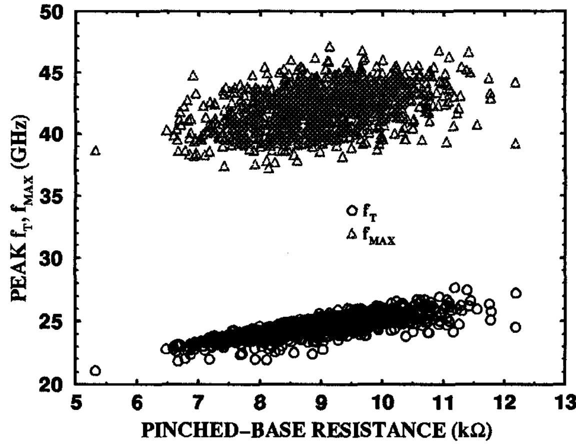

Fig.6: 1000 Monte Carlo simulations of the statistical variation of peak f_T and f_{MAX} with pinched-base resistance for a 2x0.5x20μm^2 Si BJT.

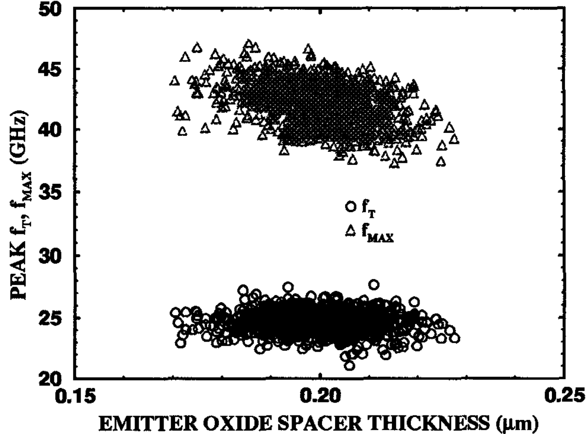

Fig.7: 1000 Monte Carlo simulations of the statistical variation of peak f_T and f_{MAX} with emitter spacer width for a 2x0.5x20μm^2 Si BJT.

Benchmark MMIC verification

Record-breaking cascode LNAs at 5.8GHz (NF=2dB, G=10dB, P_{diss}=9mW) and broadband amplifiers (G=9dB, B_{3dB}=22GHz, S_{11}<-20dB, NF=6dB, P_{1dB}=12.5dBm, group delay ripple < 8ps) have been designed, fabricated in IBM's SiGe HBT process, and tested across wafers with excellent agreement between measurements and statistical and corner simulations. Both circuits were first designed in Si bipolar technology [8] and have all the matching inductors on chip. The performance quoted above includes the effect of the 60x60μm^2 bonding pads which feature grounded n^+ or polysilicon regions under the pad in order to achieve substrate isolation and Q enhancement without increasing pad capacitance beyond 30fF.

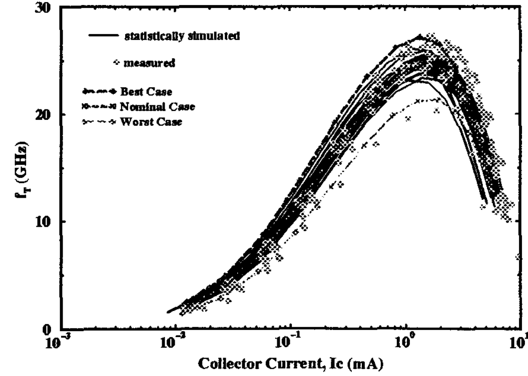

Fig.8: Measured across wafers, statistically simulated, and best, worst and nominal case simulations of f_T vs. I_C characteristics for a 0.5x5μm^2 Si bipolar device.

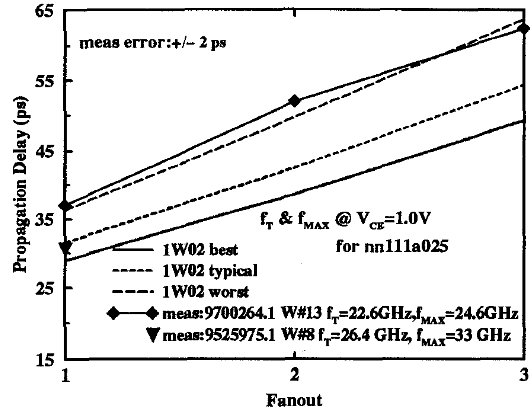

Fig.9: Measured Si bipolar CML delay vs. fanout for two wafers and the simulated best, worst and nominal case performance. 0.5x2.5μm^2 transistors are used.

The accuracy of the transistor and passive component models allowed for post-layout fine-tuning of input transistor length to compensate for a 15% circuit bandwidth degradation due to interconnect parasitics, as illustrated in Fig.12. The successful use of on-chip inductors to significantly improve input return loss through 20GHz is a premiere for Si-based processes. At 10GHz the input return loss was dropped from -10dB to -20dB. These results also demonstrate a doubling of the gain-bandwidth product for SiGe HBT Darlington amplifiers over their Si BJT variants, commensurate with the f_T, f_{MAX} leverage between the two technologies. When compared to identical Si LNAs, 2dB and 1dB improvement is noticed, respectively, for the gain and noise figure of tuned 5.8GHz SiGe LNAs. The measured noise figure is shown in Fig.13. Noise parameter measurements of SiGe LNA implementations with and without the input inductor on chip revealed a 0.4dB contribution to the overall noise figure from the input inductor.

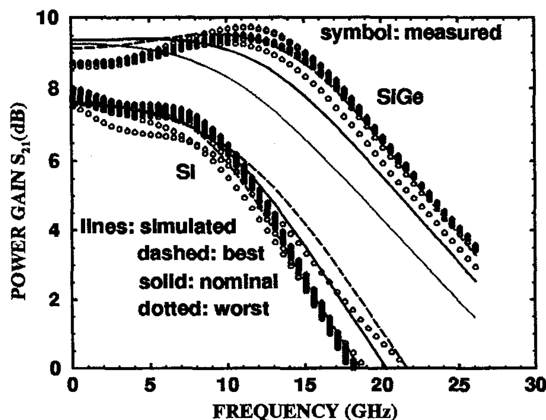

Fig.10: Si and SiGe Darlington amplifier gain vs. frequency characteristics measured across wafers and best, worst and nominal case simulation results.

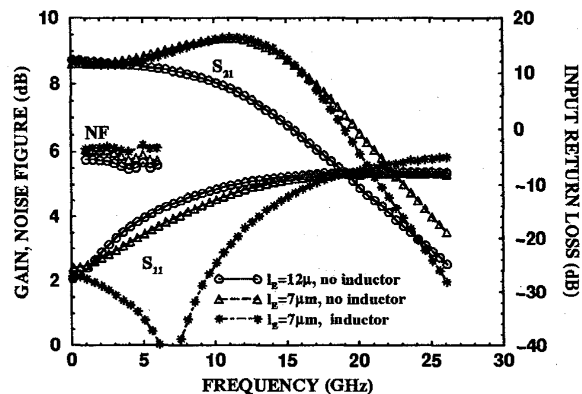

Fig.12: Measured impact of input inductor and transistor length l_E on SiGe Darlington amplifier characteristics. A 3GHz improvement in the 3dB-bandwidth is achieved.

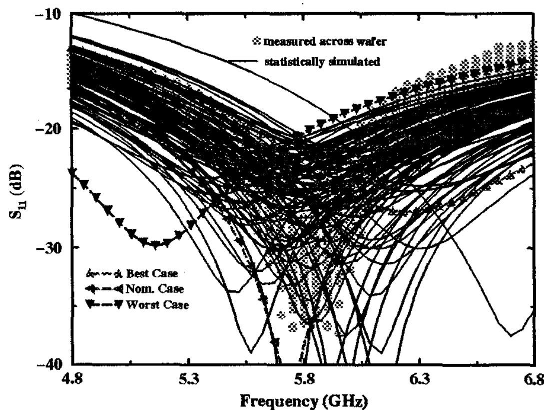

Fig.11: Si LNA input return loss vs. frequency characteristics measured across a wafer, as well as statistical and best, worst and nominal case simulation results.

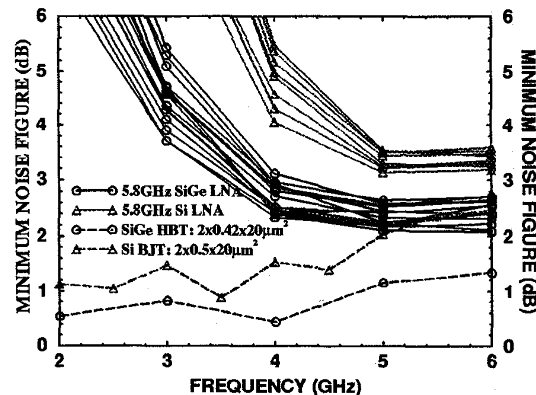

Fig.13: Measured NF_{MIN} for Si and SiGe LNAs across wafers. Transistor performance is also shown for reference.

Conclusion

A design environment for Si and SiGe MMICs relying on statistical process- and geometry-scalable transistor and transmission line models was developed and verified on the high frequency performance of tuned LNAs and Darlington amplifier circuits through 20GHz. Principal component analysis was used to define best- and worst-case process files simultaneously valid for device, analog circuit and digital circuit performance. This approach allowed for circuit design fine-tuning after layout extraction to offset significant performance degradation due to interconnect parasitics. Record-breaking noise figures of 2dB (on-chip input inductor) and 1.6dB (no input inductor) were achieved for tuned cascode SiGe LNAs at 5.8GHz

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References

[1] S.P.Voinigescu et al., "A scalable high frequency noise model for bipolar transistors with application to optimal transistor sizing for low-noise amplifier design," *IEEE J.Solid-State Circuits*, vol.32, pp.1430-1438, 1997.

[2]D.M.Krafcsik and D.E.Dawson,"A closed-form expression for representing the distributed nature of the spiral inductor," *IEEE-MTT Monolithic Circuits Symposium Digest*, pp.87-91, 1986.

[3]T.Sakurai and K.Tamaru,"Simple formulas for two- and three-dimensional capacitances," *IEEE Trans. ED*, vol.ED-30, pp.183-185, 1983.

[4]E.Pettenpaul, H.Kapusta, A.Weisgerber, H.Mampe, J.Luginsland, and I.Wolff, "CAD models of lumped elements on GaAs up to 18GHz,"*IEEE Trans. MTT*, vol.36, pp.294-304, 1988.

[5] D.J. Walkey and M.Schroter, "Modelling the effect of doping variation in bipolar transistors", *NORTEL internal report*, May24, 1996.

[6]C.McAndrew, J.Bates, R.Ida, and P.Drennan, "Efficient statistical BJT modeling, why β is more than Ic/Ib," *BCTM Proceedings*, pp.28-31, 1997.

[7] K.Walter et al., "A scaleable, statistical SPICE Gummel-Poon model for SiGe HBTs," *BCTM Proceedings*, pp.28-31, 1997.

[8]S. P. Voinigescu, and M. C. Maliepaard, "5.8GHz and 12.6GHz Si bipolar MMICs," *ISSCC-Digest*, pp.372-373, Feb.1997.