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A COMPARISON OF SILICON AND III−V TECHNOLOGY PERFORMANCE AND BUILDING BLOCK IMPLEMENTATIONS FOR 10 AND 40 Gb/s OPTICAL NETWORKING ICs

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Scalable models for both active and passive components are essential for the design of highly integrated fiber−optic physical layer ICs. This paper focuses on the various technology options available for 10 Gb/s and 40 Gb/s applications, on how their constituent components are modeled and what the characteristics and requirements are for the basic building blocks. As part of the technology comparison, an overview of the performance of leading edge Si CMOS, SiGe BiCMOS and III−V technologies is presented. Scalable models for SiGe HBTs and GaAs p−HEMTs are then compared with measured data for various device sizes. Inductors, varactors, transmission lines and isolation techniques on Si and III−V substrates are discussed next followed by technology−specific implementations of VCO and digital building blocks. Finally, Transimpedance Limiting Amplifier (TIALA) as well as laser and modulator driver designs in SiGe BiCMOS, InP HBT and GaAs p−HEMT processes using scalable device models are illustrated for 10 and 40 Gb/s fiber−optics applications.

Keywords: Heterostructure technolologies, transimpedance amplifier, output driver

1. Introduction

Bandwidth demand in local area networks (LANs) and over the Internet is growing rapidly due to applications such as video, multimedia, E−commerce, and advanced digital services. This ever−increasing need for bandwidth is creating huge demand on the short to medium reach applications. At the forefront of addressing this, the IEEE 802.3ae standards committee has approved Ethernet specifications for 10 Gb/s premises networking applications. Current generation Ethernet LANs are being deployed with 100 Mb/s connections at the desk, and 1 Gb/s on the LAN backbones. At present, 10 Gb/s physical layer (PHY) integrated circuits (ICs) can be found primarily in long haul applications such as transport or wide area networks (WAN). Unfortunately their power consumption, high cost, lower level of integration [1] and footprint make them unsuitable for Very−Short−Reach (VSR) links, Storage Area Networks (SAN), LAN, and MAN (Metropolitan Area Networks) networks.

Regardless of the reach and data rate of a typical application, fiber−optics modules have very similar architectures, containing both high speed digital, as well as analog building blocks such as TransImpedance Amplifier (TIA), post amplifier, driver, clock and data recovery (CDR), and transmit phase−lock−loop (PLL), as illustrated in Fig.1. In addition, depending on the application, a significant amount of logic gates might be required for traffic and protocol processing.

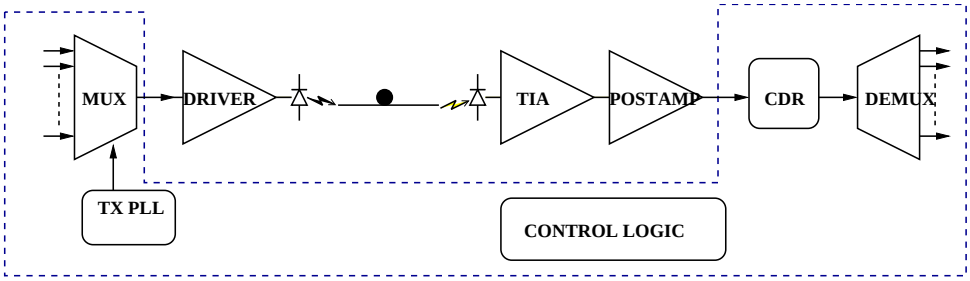


Fig.1. Typical PHY layer block diagram for 10 Gb/s and 40 Gb/s fiber systems.

High levels of IC integration in the 10 Gb/s and eventually 40 Gb/s markets are logical steps in optimizing such systems in terms of speed, power and cost performance. Indeed, several highly integrated SiGe BiCMOS (Bipolar Complementary Metal Oxide Semiconductor) and CMOS (Complementary Metal Oxide Semiconductor) transceivers in the 10 Gb/s range have been reported during the last three years [2−7].

This paper will start with an overview of the competing semiconductor technologies vying for 10 and 40 Gb/s applications. Next, basic building blocks such as Voltage−Controlled−Oscillators (VCOs), multiplexers (MUX), demultiplexers (DEMUX), output drivers and their technology requirements will be addressed. Finally, examples of 10 and 40 Gb/s transimpedance limiting amplifiers (TIALA) and laser and modulator drivers implemented in SiGe BiCMOS, InP Heterostructure Bipolar Transistor (HBT) and GaAs p−HEMT (pseudomorphic−High Electron Mobility Transistor) processes will be presented.

2. Semiconductor Technologies

2.1 *Technology requirements*

The first generation OC192 (10 Gb/s) systems of the mid 1990's [1] have relied exclusively on GaAs HBT, GaAs MESFET (Metal Semiconductor Field Effect Transistor) and GaAs p−HEMT technologies to deliver the performance required in fiber−optics modules. To date, they have low levels of integration and are dominated by a "mix−and−match" of discrete components and ICs. It is noteworthy that the raw transistor speed of these technologies, with typical f_T and f_{MAX} values of 60−70 GHz, far exceeded the capabilities of Si−based state−of−the−art devices at the time. This situation is now tending to favor SiGe npn and CMOS transistors as their cutoff and oscillation frequencies now exceeds 80 GHz.

The list of critical active and passive device requirements for successful implementation of highly integrated PHY ICs starts with the transistor speed. Historical data indicate that, at a minimum, the cutoff frequency, $f_{T,}$ and the maximum oscillation frequency, $f_{MAX,}$ should both exceed the system bit rate by a factor of at least 4. i.e. 43 GHz for 10.7 Gb/s systems, and 172 GHz for 43 Gb/s. These conditions must be met *over all process corners and the entire range of operating temperatures*. In some instances, as long as f_{MAX} is larger than four times the bit rate, the requirement for f_T can be relaxed, as in one circuit example discussed in Section 5. In order to successfully integrate VCOs and clock and data recovery circuits, the technology must also be able

to support high quality passive components such as inductors, transmission lines, varactor diodes and MIM capacitors. All these passive components should have good quality factors and high resonant frequencies (f_{res}) beyond 20 GHz for 10 Gb/s systems, and beyond 80 GHz for 40 Gb/s applications. While in the past most of the research on model development focused on transistors, it has since been acknowledged that accurate models for passive components and interconnect are equally, if not more, important in the successful design of fiber−optic ICs. Finally, in order to maximize the integration level, minimize parasitic capacitance and to ensure good isolation between circuit blocks, a large number of metal layers with low−k inter−metal dielectric is desirable.

2.2. *Transistor performance*

The most relevant transistor performance for fiber−optic ICs is effectively captured by the following figures of merit, most of which are also summarized in Table 1:

- *peak f_T and f_{MAX}* values − determine the ultimate circuit speed;
- *peak f_T current density* J_{cpfT} − determines the power dissipation of a high speed circuit at a given data rate;
- $I_{cpfT}/C_{BC}(C_{GD})$, also known as the *intrinsic slew−rate* of the transistor, is defined as the ratio of the peak f_T current and the output capacitance (for completeness, C_{CS}/C_{DB} should be added to the output capacitance);
- BV_{CEO}/BV_{DG} − the *breakdown voltage* of the transistor which limits the maximum output swing achievable in the technology;
- *turn−on/threshold voltage*: V_{BE}/V_T − limits the minimum value of the power supply voltage and, usually, power dissipation of a circuit and favors CMOS over bipolar devices, and InP HBTs over SiGe HBTs;
- *minimum feature size* −affects power dissipation and integration levels and favors Si CMOS and SiGe BiCMOS over III−V technologies due to the more mature processing techniques;
- *thermal resistance* is closely related to the semiconductor material and to the minimum feature size and affects indirectly the integration levels and the transistor speed that can be achieved under reliable operating conditions.

Table 1. Performance of State−of−the−Art Production Semiconductor Technologies (best lab results shown in brackets)

Device/ Parameter	InP HBT @ Vce=1.5 V	SiGe HBT @ Vce=1.5V	CMOS @ Vds=1.2 V	GaAs p−HEMT @ Vds=1.5 V	InP HEMT @ Vds=1 V
feature size (μm)	1	0.18	0.13 (0.09)	0.15	0.1
f_T (GHz)	180 (300)	160 (200)	80 (120)	110	175
f_{MAX} (GHz)	200 (300)	150 (200)	80..100 (120)	180	300
J_{cpfT} (mA/μm^2)	2	6	1.66 (2.5)	1.87	2.9
I_{CpfT}/C_{BC} (V/ps)	0.34	0.5	0.54	2.86	1.16
BV_{CEO}/BV_{DS} (V)	>2	>2	>1.5 (>1V)	>6	>2
V_{BE}/V_T (V)	0.75	0.95	0.35 (0.3)	−0.9	−0.6

Fig. 2 illustrates how the f_T of Si CMOS and Si/SiGe bipolar devices scales with process feature size. For the same generation of lithography, n−channel MOSFETs exhibit at best half the speed of SiGe HBTs with p−channel device performance half that again. SiGe HBTs have been aggressively scaled in the last two generations in order to retain their x2 and x4 speed advantage over n−channel and p−channel MOSFETs, respectively. In general, for the same f_T, the n−MOS feature size is two generations ahead of the bipolar one, thus offsetting the lower cost associated with the smaller number of masks in a CMOS process compared to a SiGe BiCMOS process.

SiGe HBT f_T and f_{MAX} values in the 160 to 200 GHz range, or even higher, have recently been announced by several foundries [8−11]. For 40 Gb/s applications, devices with over 160 GHz f_T and f_{MAX} values are required and such performance had, until the last year, been reached only by InP HBTs [12] and HEMTs [13]. Fig. 3(a) compares the f_T and f_{MAX} dependence on collector current density for state−of−the−art SiGe and InP HBTs. The InP devices enjoy some advantage in f_T (180 GHz versus 160 GHz), f_{MAX} (200 GHz versus 150 GHz), *peak f_T current density* (2 mA/μm^2 vs. 6 mA/μm^2) and *turn on voltage* (0.75 V as opposed to 0.95 V). The latter feature allows for InP ECL and even E^{2}CL circuits to operate with large margin from a 3.3V supply which is not achievable with SiGe HBT E^{2}CL circuits.

The lower *peak f_T current density* of InP HBTs is not typically exploited fully due to the coarser lithography employed in state of the art III−V HBTs compared to SiGe HBTs. For example, the minimum size 0.18 μm x 0.5 μm SiGe HBT has a peak f_T current of 0.6 mA, almost half that of a very "aggressive" minimum size 0.5 μm x 1 μm InP HBT featuring a peak f_T current of 1 mA. Reducing the emitter size in InP HBTs beyond 0.5 μm has proven very difficult because of increasing surface recombination, which reduces current gain below acceptable levels.

To facilitate the comparison between bipolar and FET performance, Fig. 3(b) shows the measured f_T and f_{MAX} dependence on drain current linear density (current per unit gate width) for 0.13 μm Si n−MOSFETs, 0.15 μm GaAs p−HEMTs and 0.1 μm InP HEMTs. While the f_T values of the GaAs p−HEMT and InP HEMT devices (110 GHz and 170 GHz, respectively) are lower or comparable to those of the SiGe and InP HBTs, the f_{MAX} values are higher (180 GHz and over 300 GHz, respectively.)

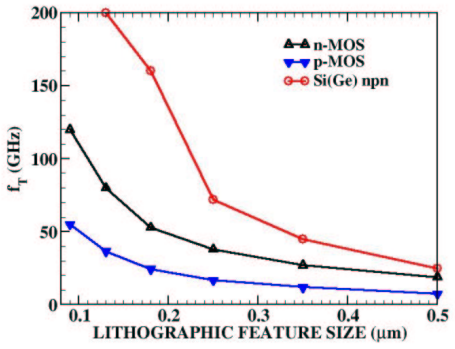


Fig.2. Scaling of Si CMOS and Si(Ge) npn devices as a function of feature size.

The f_{MAX} is higher in III−V HEMTs due to the very low resistance of the metal gate, when compared to HBT base resistance, and due to much lower drain−gate capacitance compared to HBT collector−base capacitance. The peak f_T current for all FETs shown in Fig. 3(b) occurs between 0.28 and 0.32 mA/μm. According to field effect transistor scaling rules [14], the current per unit gate width should remain constant, as the device gate length is reduced to 0.09 μm and beyond. As illustrated in Table 1, one can define a current density for FETs by dividing the drain current linear density by the gate length. In that case, the peak f_T current density for field effect transistors is comparable to that of the InP HBT and it scales as l_G^{-1} , where l_G is the gate length.

The *intrinsic slew rate* is an important figure of merit for digital circuits and output drivers. It reflects the capability of a device technology to operate with large voltage swing at very high speed. Typical values are 0.34 V/ps for InP HBT processes and 0.5 V/ps for the fastest SiGe HBTs and 0.13 μm n−MOSFETs. The best values are obtained for InP HEMTs and GaAs p−HEMTs. Even though the intrinsic slew rate is very high, the loaded slew rate (including interconnect capacitance) is severely degraded by the interconnect capacitance. This is particularly the case for Si MOSFETs and SiGe HBTs because the interconnect capacitance is higher in silicon technologies than on semi−insulating III−V substrates. As an example, a 3x0.13μmx2μm n−MOSFET or a 0.18μmx1μm SiGe HBT, both with a peak f_T current of about 1.1 mA driving a 2 fF interconnect capacitance will have a loaded slew rate of 0.27 V/ps, and 0.26 V/ps, respectively, half the value of the intrinsic slew rate. In most practical situations, the parasitic capacitance is larger than 2 fF and the slew rate degradation is more severe, unless larger devices with higher bias currents are deployed.

Unlike bipolar devices, which, for a given process, exhibit a fairly constant f_{MAX} for different emitter lengths, the f_{MAX} of field effect transistors is strongly dependent on unit gate finger width, as well as on gate access geometry (single side versus double side, T versus Π shape, etc.) The measured variation of f_{MAX} and f_T with unit gate finger width is illustrated in Fig.4 for various FET technologies.

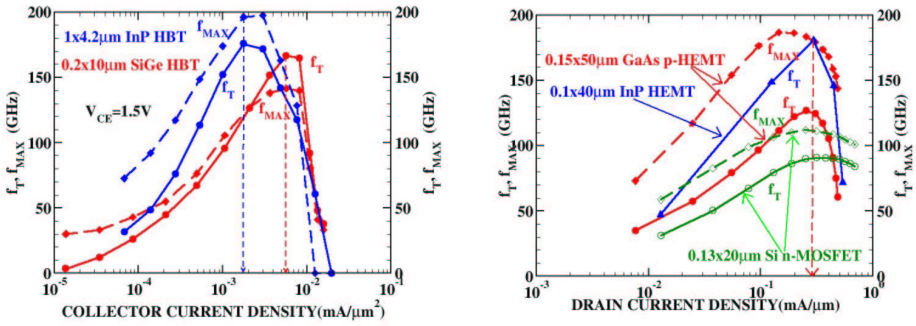


Fig.3. a) Measured 0.18x10μm² SiGe HBT vs. 1x4.2μm² InP HBT f_T and f_{MAX} characteristics as a function of the collector current density; b) measured 0.1μm InP HEMT vs. 0.15 μm GaAs p−HEMT vs. 0.13 μm Si n−MOSFET f_T and f_{MAX} characteristics as a function of drain current per unit gate width.

As the unit finger width is scaled down, fringing capacitance becomes dominant for all technologies degrading both f_{MAX} (in the case of III−V FETs) as well as f_T in the extreme case of very narrow gates. For Si MOSFETs, the polysilicon gate resistance, several orders of magnitude larger than the metal gate resistance of III−V HEMTs, is the dominant factor in f_{MAX} degradation [14−15]. f_{MAX} only scales as $l_G^{-1/2}$ [14] while f_T is proportional to $1/l_{G,}$ Unless methods to significantly reduce the gate sheet resistance in MOSFETs are introduced, maintaining a higher f_{MAX} than f_T is going to be very problematic as gate lengths are shrunk to 0.09 μm and beyond.

With shrinking device dimensions, accurately predicting in simulation the $f_T(I_C)$ characteristics for a wide range of V_{CE}/V_{DS}, values, as well as for different device geometries (gate width and emitter length, respectively) becomes even more critical. Fig. 5 compares the modeled and measured characteristics for a family of 0.25 μm SiGe HBTs for emitter lengths varying between 3.2 and 25.6 μm. By carefully selecting a range of emitter sizes and using suitable de−embedding structures in transistor measurements and model extraction, excellent agreement is reached between measurements and simulations using one single scalable model for all SiGe HBTs. A foundry−proprietary, modified Spice Gummel Poon model with improved saturation region and breakdown behavior was employed. In Fig. 6, measured characteristics from an entire wafer are compared with best, worst and typical Spice−Gummel Poon model simulations. It is important to note that the measured peak f_T values, centered at 160 GHz, vary by +/−10% across the entire wafer, a range commensurate with the spread predicted by the best and worst case corner models. It becomes imperative that all process corners be used in circuit design to ensure good circuit yield in production.

Fig. 7 illustrates measured versus simulated $f_T(I_{DS})$ characteristics for single− and multi−finger 0.15 μm GaAs p−HEMTs with different unit gate finger widths. Again, given good process control and careful test and de−embedding structure design, it is possible to fit all device sizes with a single large signal scalable model. In this case a modified Agilent EE−HEMT model was used.

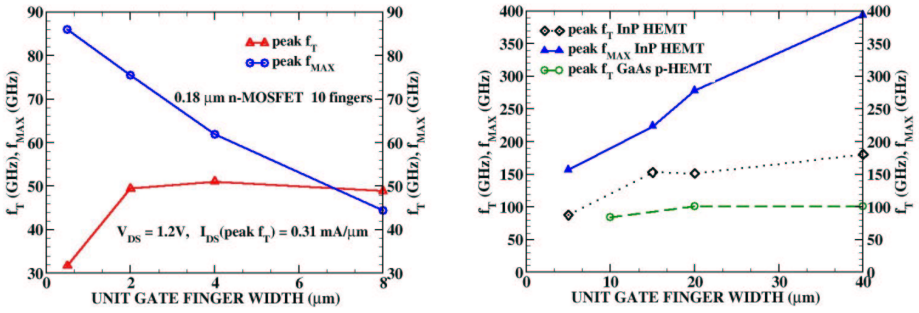


Fig.4. a) Measured f_T and f_{MAX} dependance on unit gate finger width for 0.18 μm n−channel MOSFETs. b) Measured f_T and f_{MAX} dependance on unit gate finger width for single−gate finger 0.1 μm InP HEMTs and 0.15 μm GaAs p−HEMTs.

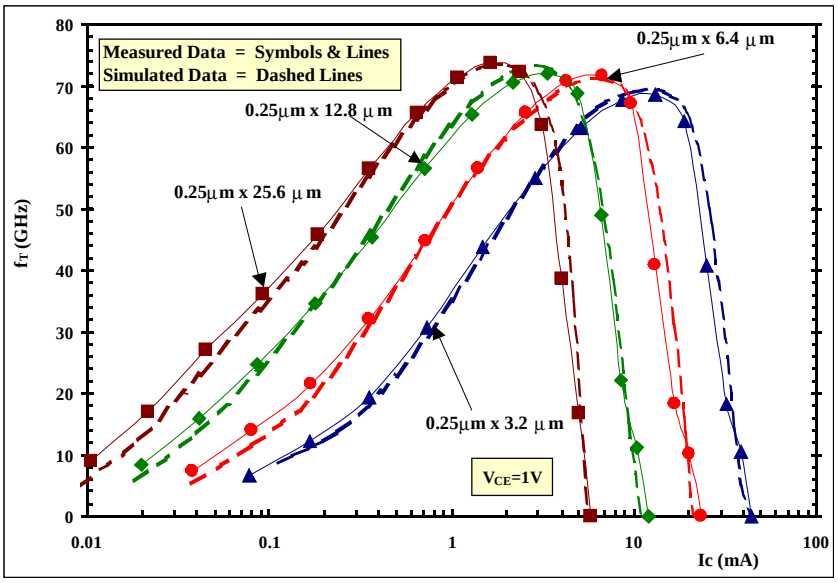


Fig.5. Measured vs. modeled f_T (I_C) characteristics as a function of emitter length for SiGe HBTs in a 0.25 μm SiGe BiCMOS process. A modified Spice Gummel Poon model was used.

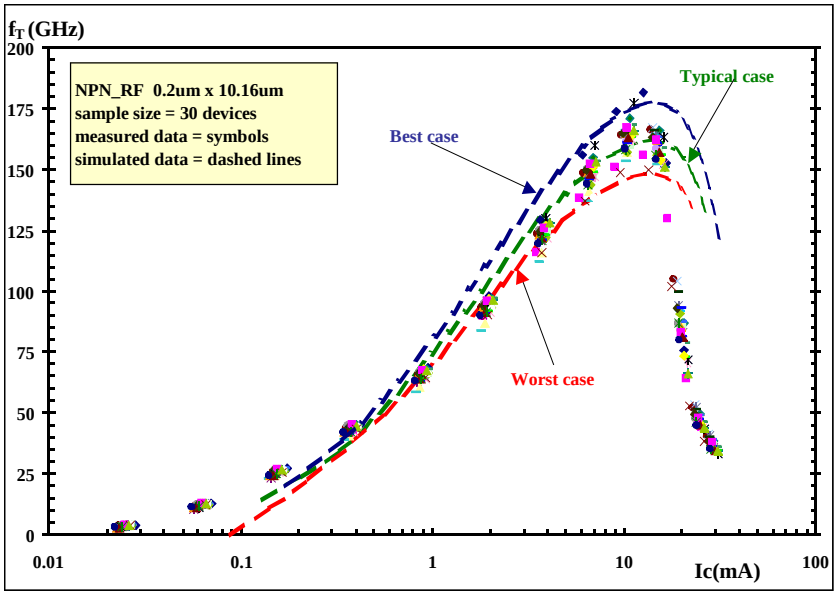


Fig.6. Measured across a wafer vs. best, typical and worst case model f_T (I_C) characteristics for SiGe HBTs in a 0.18 μm SiGe BiCMOS process. The Spice Gummel Poon model provided by the foundry was used in simulation.

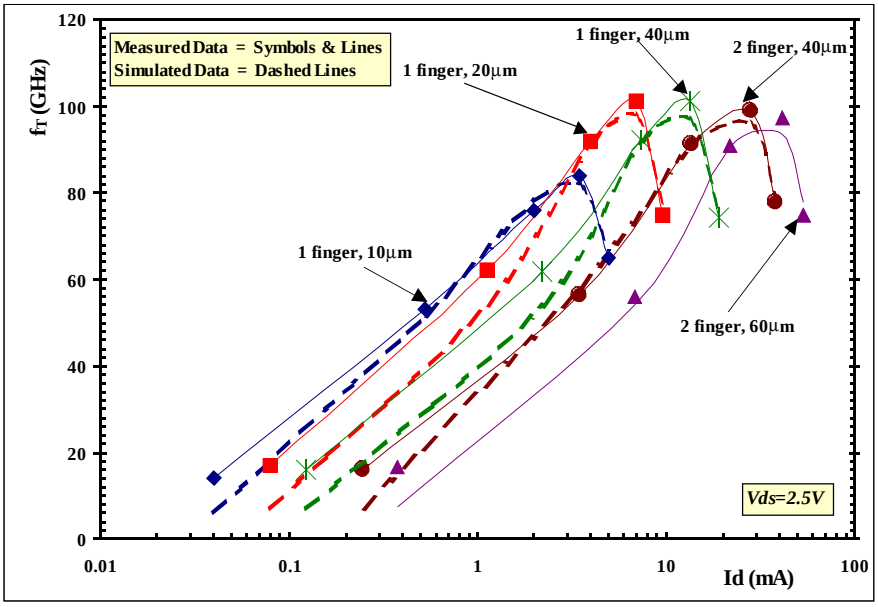


Fig.7. Measured vs. simulated f_T (I_{DS}) characteristics as a function of gate width (beyond 50 μm two or more gate fingers are used). The simulated characteristics are obtained using the large signal, scalable HEMT model.

2.3. *Passive devices: inductors, varactors, transmission lines and isolation techniques*

Recent results, shown in Fig. 8, indicate that inductors and varactors with Qs larger than 10 and resonant frequencies beyond 50 GHz can be realized on silicon substrates in conventional processes where only the top metal layer was thickened to 3 μm [18]. Measured characteristics of a 425 pH octagonal inductor are shown in Fig. 8(a) as a function of frequency. The peak Q is above 12 in the 20 to 50 GHz range. The frequency of operation was maximized by reducing the metal width to 5 μm and by minimizing the total inductor area, thus minimizing parasitic capacitance and substrate losses, the dominant loss mechanism beyond 5 GHz. Si varactor diode *Q(f)* characteristics, obtained from S parameter measurements, are shown in Fig. 8(b) for voltages between 0 and 5 V. Q is larger than 4 up to 50 GHz, even when the device is biased at 0 V. With a capacitance ratio of over 2.5, this device is superior to any varactor that can be realized in a conventional III−V technology that also integrates HBTs or HEMTs on the same die.

Computer programs are available today to accurately design and model two terminal and three−terminal (or differential) inductors. Fig. 9 compares measured vs. modeled apparent inductance and quality factor for a rectangular 150 pH inductor on an InP substrate and for a 650 pH three terminal (differential) inductor fabricated in a 0.35μm SiGe BiCMOS process. In both cases, good agreement between measurements and simulations is obtained.

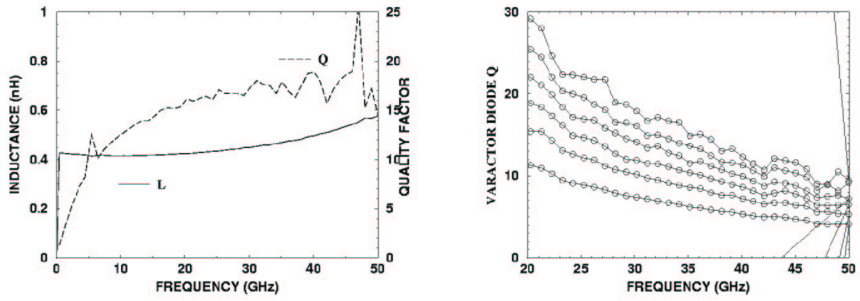


Fig.8. a) Measured inductance and quality factor of a 0.425 nH octagonal inductor in a 0.5 µm SiGe HBT process; b) Measured quality factor of a 2x1.6µmx20µm multi−stripe varactor diode as a function of frequency and varactor voltage between 0 V and 5 V [18].

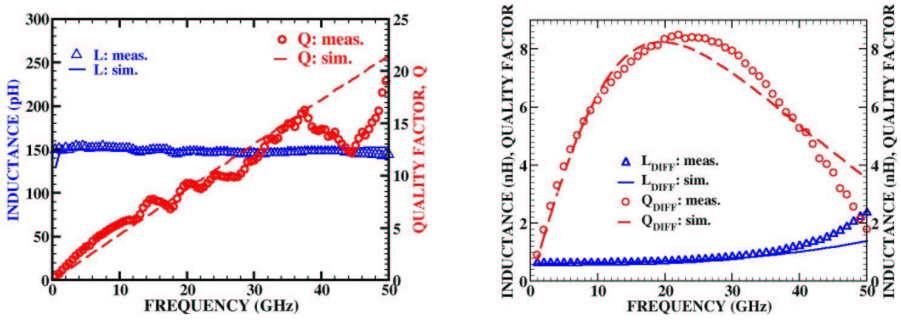


Fig.9. Measured vs. modeled inductance and quality factor for a) a rectangular 150 nH inductor in an InP process, and b) a 0.650 nH three terminal inductor in a SiGe HBT process

Traditionally, it has been assumed that silicon−based technologies lack the low−loss and good isolation properties of III−V technologies. Even with circuit techniques such as top metal over first metal ground planes and top metal over salicided polysilicon ground planes developed to overcome the disadvantages of the lossy silicon substrate [16−17], the loss and parasitic capacitance of interconnect over Si substrates continue to be slightly higher than those over semi−insulating III−V substrates.

The use of transmission lines is unavoidable in any highly integrated PHY IC at 10 or 40 Gb/s. At a minimum, clock signal distribution is typically implemented using controlled impedance, on−chip terminated transmission lines. In addition, it is common for the fiber side inputs and outputs of the PHY die to have on−chip matched 50 Ω transmission lines that conduct the signal between the pads and the circuit core. Transmission lines with a characteristic impedance larger than 50 Ω (typically up to 100 Ohm) are preferred for intra−chip signal distribution in order to minimize power dissipation. However, as data rates and frequencies increase, the bandwidth of the

transmission line itself can become a high speed bottle−neck for the entire circuit and the value of the characteristic impedance must be lowered. By taking advantage of the large number of metal layers and of the high quality of low permitivity dielectrics typical of Si CMOS and SiGe BiCMOS technologies, transmission lines can be realized in Si processes with good control of the characteristic impedance and low loss even at 50 GHz. Fig. 10(a) compares the measured characteristic impedance and loss per mm of GaAs and SiGe microstrip lines as well as of InP coplanar waveguides (CPW). The 55Ω GaAs microstrip lines were fabricated on a 28 μm thick semi−insulating substrate with 5 μm thick Au interconnect. The 50 Ω SiGe transmission lines were realized using 3 μm thick Al top metal with 0.45 μm thick Al as the ground plane and 9.5 μm SiO_2 dielectric. The 50 Ω InP CPW line was implemented with 2 μm thick Au interconnect on a 600 μm thick semi−insulating substrate. The frequency dependence of the characteristic impedance, as well as of the attenuation of these microstrip and coplanar transmission lines, are well captured by the built−in models available in most common microwave and SPICE−like circuit simulators, as illustrated in Fig. 10(b). The agreement between the measured and simulated characteristic impedance for both SiGe microstrip and InP coplanar lines is better than 5%. However, to accurately model microstrip or coplanar lines over a lossy Si substrate, lumped RLC models based on measurements are still necessary [16].

It is not widely known that coupling between interconnect lines is significantly higher in III−V than in advanced Si technologies. Fig. 11 illustrates, using 3D EM simulation results, the cross−coupling between two adjacent metal interconnect lines on Si and InP substrates. As described above, the Si transmission line is realized using the top metal layer and the first metal layer as ground plane. In the InP case, the line is placed on top of the semi−insulating substrate while the ground is on the back side of the 100 μm thick wafer. In each case, the interconnect lines were designed to have a characteristic impedance of 66 Ohm when widely spaced apart. For a given line spacing, the cross−coupling is significantly weaker on the Si substrate. The thicker InP substrate seriously impedes high interconnect densities and integration levels. Ironically, this problem can only be solved in III−V technologies by resorting to either silicon−like interconnect with many metal layers and low−k dielectrics where the transmission lines have ground planes above the III−V substrate [14−15], or by thinning the semi−insulating GaAs or InP substrate. The latter situation is illustrated in a circuit example in Section 5.

On Si substrates, pn−junctions can be used in conjunction with deep n−wells and large first metal ground planes to reduce cross coupling through the substrate. Each circuit block is surrounded by a sufficiently wide guard−ring made of the above combination. 50−60 dB isolation is possible even above 10 GHz [2−5, 16]. In order to reduce the noise and loss associated with the substrate resistance under the signal pads, and in order to isolate the signal pads from the substrate, a salicided n−well is placed under the signal pad. The n−well is grounded outside the pad, thus forming a reverse−biased junction with the substrate. The pad behaves like an ideal high Q (>20 at 26 GHz) capacitor. This solution also provides very low pad capacitance. A typical 40x80 μm^2 pad has 12 fF capacitance, which is comparable to that of a similar size pad on 75 μm thick GaAs or InP substrates, and is usable beyond 50 GHz [3, 16−17].

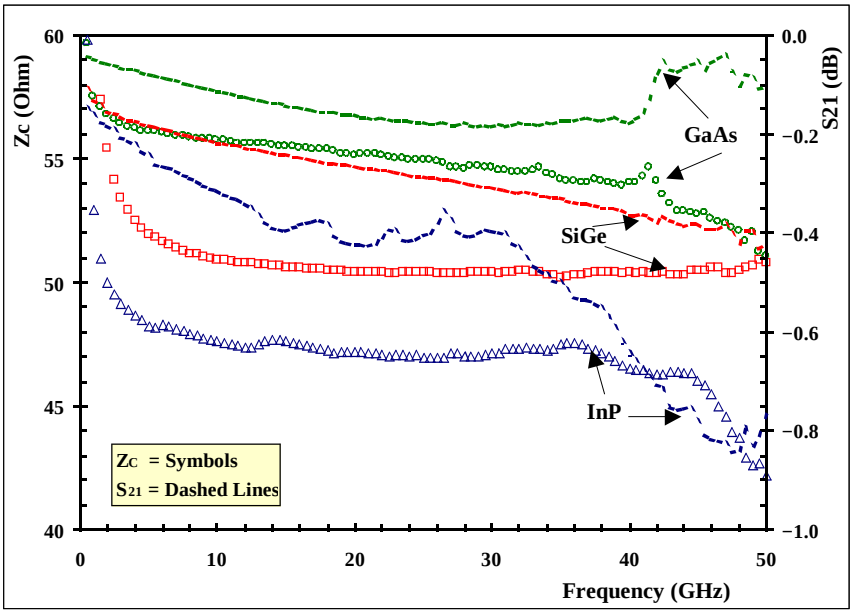


Fig.10. a) Characteristic impedance Z_C and attenuation S_{21} as a function of frequency for microstrip lines on Si and GaAs substrates and CPW lines on InP substrates.

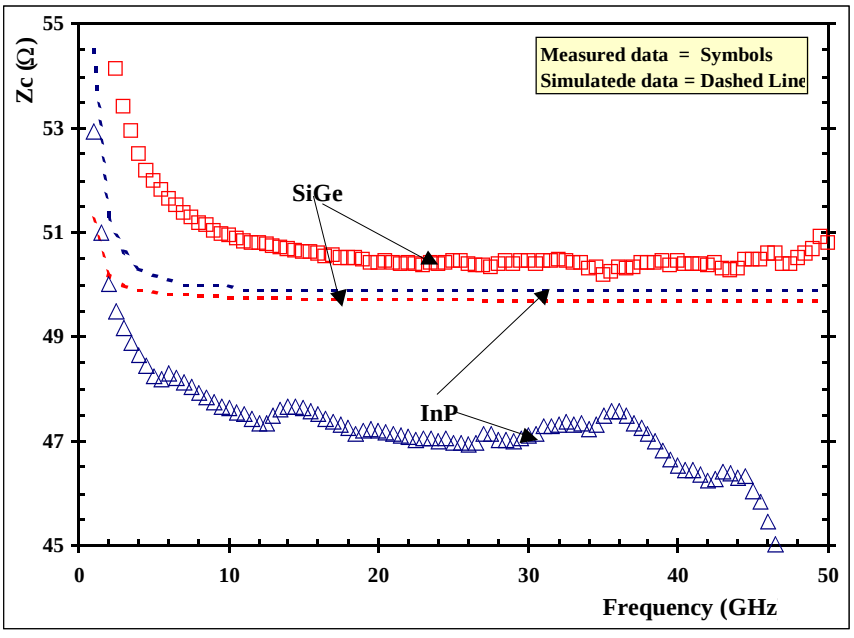


Fig.10. b) Measured vs. simulated characteristic impedance for SiGe and InP transmission lines.

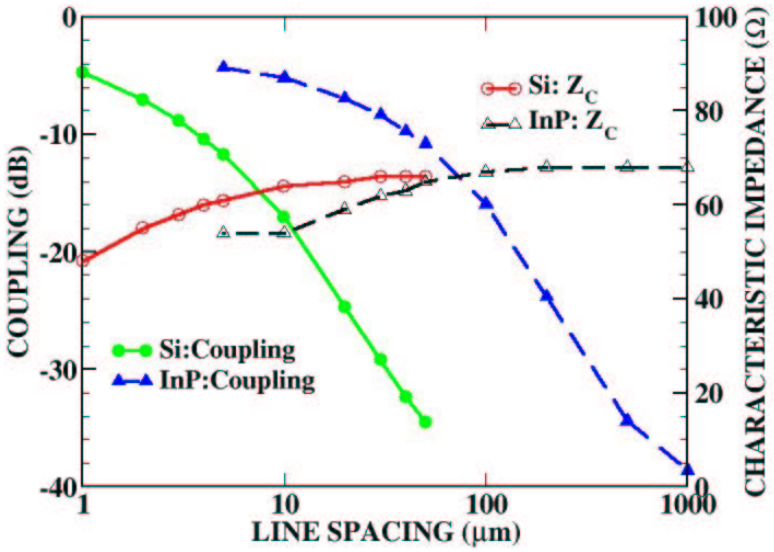


Fig.11. Coupling and characteristic impedance of two adjacent, infinitely long, microstrip lines on Si and InP substrates as a function of the spacing between lines.

3. Building Blocks

In terms of active and passive device performance, RF and fiber−optic ICs have similar requirements. However, unlike wireless applications which typically operate over a narrow frequency band and in which inductor−based tuned, narrow band circuit design is common place, PHY ICs for fiber−optics are broad band. Their frequency of operation typically extends from DC to a frequency equal to the bit rate. Also, while in most RF transceivers amplifiers and drivers tend to operate in linear mode and linearity is a critical system goal, in fiber−optics, with the exception of the transimpedance amplifier, drivers and post amplifiers are typically operated in limiting switching mode, similar to a digital circuit. For a given semiconductor device technology, the limiting switching mode of operation helps maximize the circuit bit rate and the voltage swing.

The requirements for various digital and analog blocks making up a fiber−optic system can be summarized as follows.

- Digital blocks need (i) high f_T/f_{MAX} for speed, (ii) low peak f_T current density to reduce power dissipation, (iii) low V_{BE} to reduce power supply and power consumption, (iv) small device size, and (v) fine metal pitch, the latter two being critical to reaching high levels of integration with low power dissipation.
- 50 Ω laser/modulator drivers require (i) large intrinsic slew−rate for bandwidth and S_{22} matching, (ii) large breakdown voltage for voltage swing, and (iii) high f_{MAX} to achieve the bandwidth.

- Transimpedance and post amplifiers are best realized with transistors that have (i) high f_{MAX} for bandwidth and (ii) low noise figure for good sensitivity.
- The VCO is the common block in fiber−optic and wireless ICs and it needs (i) high Q inductor for low noise, (ii) high Q varactor with large capacitance ratio to cover process spread, (iii) high Q, low parasitic capacitance MIM capacitor for low noise and large oscillation frequency and tuning range, (iv) high f_{MAX} transistor for large power and low−noise, and (v) low *1/f* noise transistor.

Arguably, the analog functions place more demanding requirements on the speed of transistor technologies than do digital functions [19]. One exception is the master−slave D−type flip−flop in the decision circuit which is typically clocked at a frequency equal to the data rate [14]. Because of its simplicity and wide band operation, the differential inverter with resistive loads is the basic circuit topology − known as current−mode−logic (CML) in its bipolar implementation − employed in both digital blocks as well as in output drivers. Other functions such as multiplexing and de−multiplexing, pulse−width (duty−cycle) [26] and peaking control can be implemented using Gilbert−cell topologies based on such inverters, or by connecting inverters in parallel at the output node of the transistor, as in Fig. 12. Its bandwidth is limited by the value of the resistive load, the output capacitance of the differential transistor pair, as well as by the input capacitance of the next stage

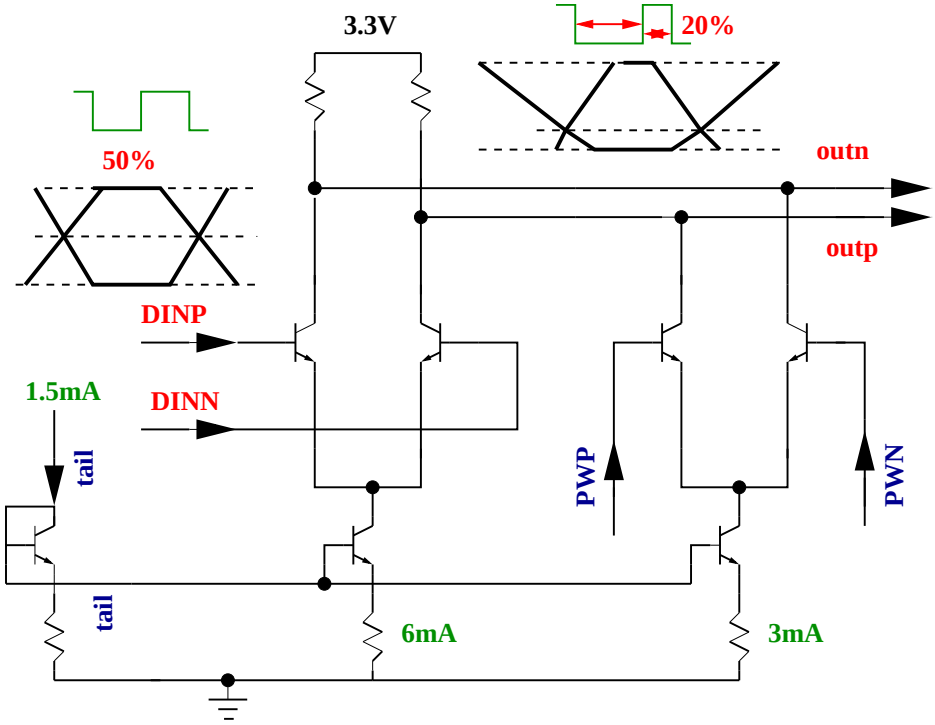


Fig.12. Circuit topology for a pulse−width control function implemented with bipolar circuits.

While active loads have the benefit of providing more gain with low DC voltage drop for a given current and power dissipation, they are seldom usable at the highest speed due to a smaller bandwidth when compared to a resistive load. If the cutoff frequency of the transistor is high enough, such that the current gain is adequate at the bit rate frequency, an inverter can drive directly another inverter, as shown in Fig. 13 for a 0.18 μm CMOS digital chain operating at 10 Gb/s [7]. The cutoff frequency of the n−channel MOSFET is 55 to 60 GHz. Also illustrated in Fig. 13 is how the bandwidth of a resistive load inverter can be extended by using inductive peaking [27]. This compensates to some extent for the low transconductance and gain of the MOSFET when operated with a resistive load and small supply voltage.

The distributed amplifier [1, 26, 27] and the distributed inverter [15] are extreme cases of inductor peaking, where, in each section of the distributed circuit, the resistive load is replaced by appropriately designed inductors to create an artificial transmission line together with the output capacitance of the transistor. This technique, which helps to push the circuit bandwidth closer to the maximum frequency of oscillation of the transistor, results in the highest bandwidth with the largest possible swing. It is primarily used in modulator drivers with voltage swings larger than 3 V at 10 Gb/s [1] and especially at 40 Gb/s [26]. Its main limitation, not an issue at 80 Gb/s [15], is the larger die area, as well as the requirement for a low−loss substrate as a transmission line medium. When the cutoff frequency of the transistor is not large enough to provide sufficient current gain at the desired bit rate, 43 Gb/s in the case of the GaAs p−HEMT implementation of Fig. 14(a) and of the SiGe HBT circuit of Fig. 14(b), the CML topology is modified by inserting one or two source/emitter follower stages between inverters [19,27]. Such f_T−doubling topologies, known as SCFL (source−coupled−FET−logic) for FET technologies and ECL (Emitter−follower−CML) or E^2CL for bipolar technologies, do not favor low supply voltage and low power dissipation.

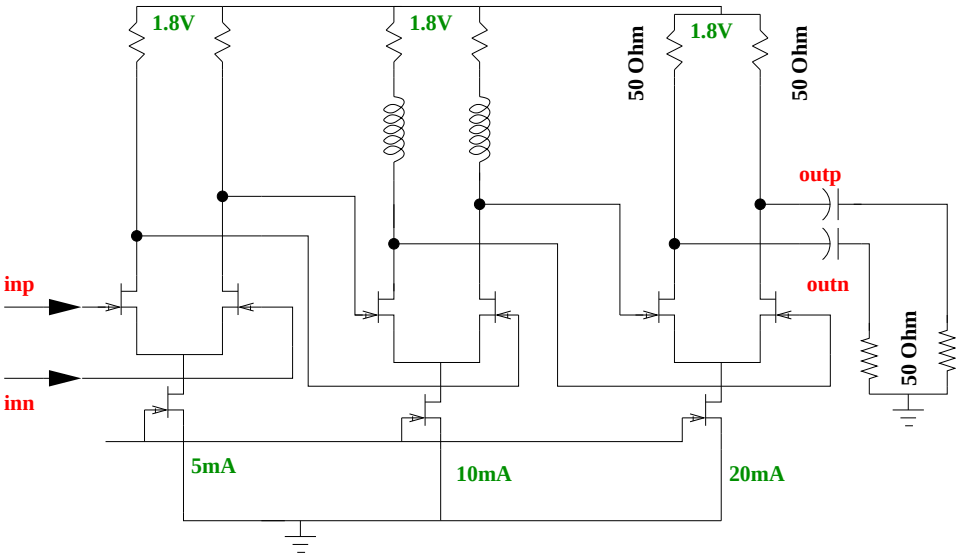


Fig.13. Schematics for CMOS−CML building block [7].

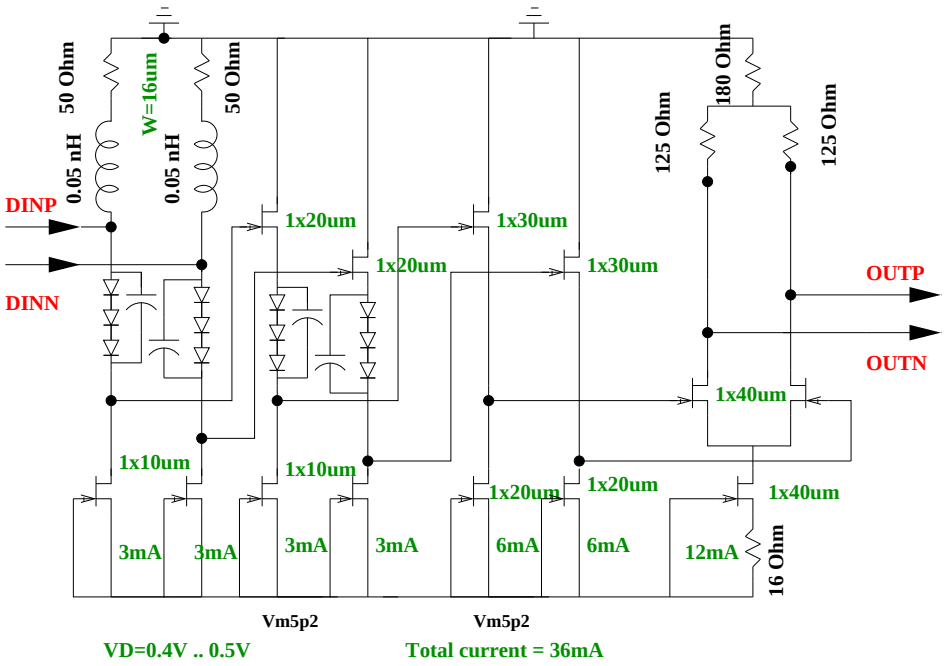


Fig. 14. a. Schematics for GaAs p−HEMT SCFL building block [26].

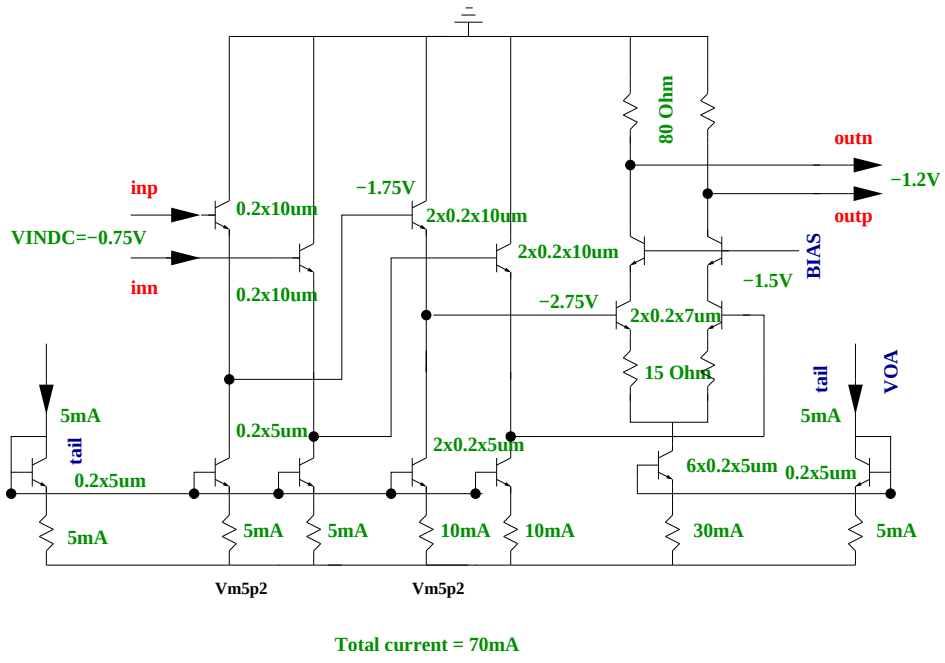


Fig.14. b. Schematics for SiGe HBT E^2CL building block.

Of all the building blocks in a fiber system, low phase noise VCOs with 15−20% tuning range have proven to be the most challenging to integrate at 10 Gb/s. Owing to the difficulty of integrating high quality inductors, varactors and fast transistors on the same substrate, it has not always been possible to achieve adequate performance. This is equally true for 20 GHz and 40 GHz VCOs. As an example, Fig. 15 shows the schematics of a 20 GHz VCO [18]. It has a differential varactor−tuned LC Colpitts topology in common−base configuration, with two inductors or a single, center−tapped 3−terminal inductor. This topology is scalable over a wide range of frequencies from 1.5 GHz to 120 GHz [3, 17−18, 24−25] and employs resistive emitter degeneration R_E to suppress harmonics and to reduce up(down) converted noise. The VCO can also operate on the second harmonic of the VCO tank, i.e. 40 GHz, when the signal is collected at node X. Fig. 16 illustrates the measured impedance as a function of control voltage and frequency for the half−circuit of the resonator, consisting of inductor L_B, MIM capacitor C_E and multi−stripe varactor diode D1. In order to characterize the resonator performance, the S parameters were measured between 10 GHz and 40 GHz with 50 MHz steps for each varactor bias. The resonant frequency was obtained from the peak, and the Q (larger than 4) was calculated from the 3 dB half−window, respectively, of the magnitude of the measured tank impedance. The resonant frequency of on−chip LC tanks is tunable over a 15% bandwidth and has low sensitivity to temperature variations [17−18]. The measured phase noise of the 20 GHz VCO is 100 dBc/Hz at 1 MHz from the carrier, as shown in Fig. 17. When operated on the second harmonic of the tank, the VCO frequency was tunable over the 40 to 45 GHz range but the phase noise was degraded due to the transistor operating beyond f_T (42 GHz) and close to f_{MAX}. (55 GHz).

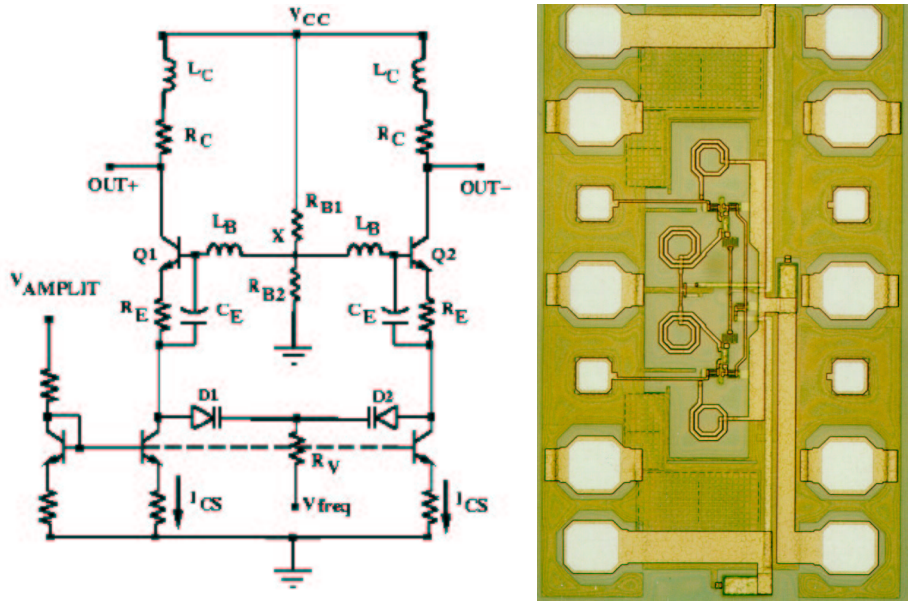


Fig.15. Schematic and layout of a family of L−C−varactor VCOs operating in the 20−40 GHz range [18].

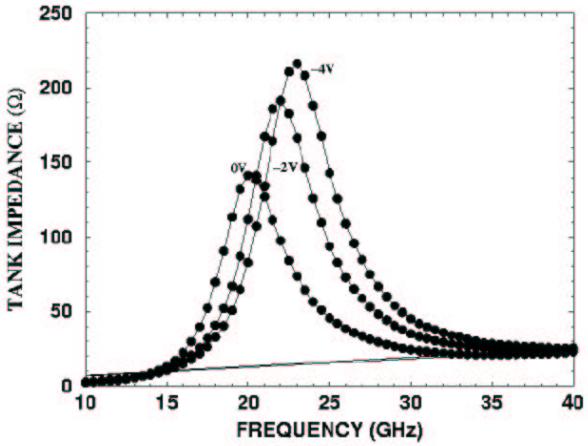


Fig.16. Measured impedance of a 20 GHz VCO L−C−varactor tank fabricated in a SiGe HBT process as a function of frequency and varactor voltage [18].

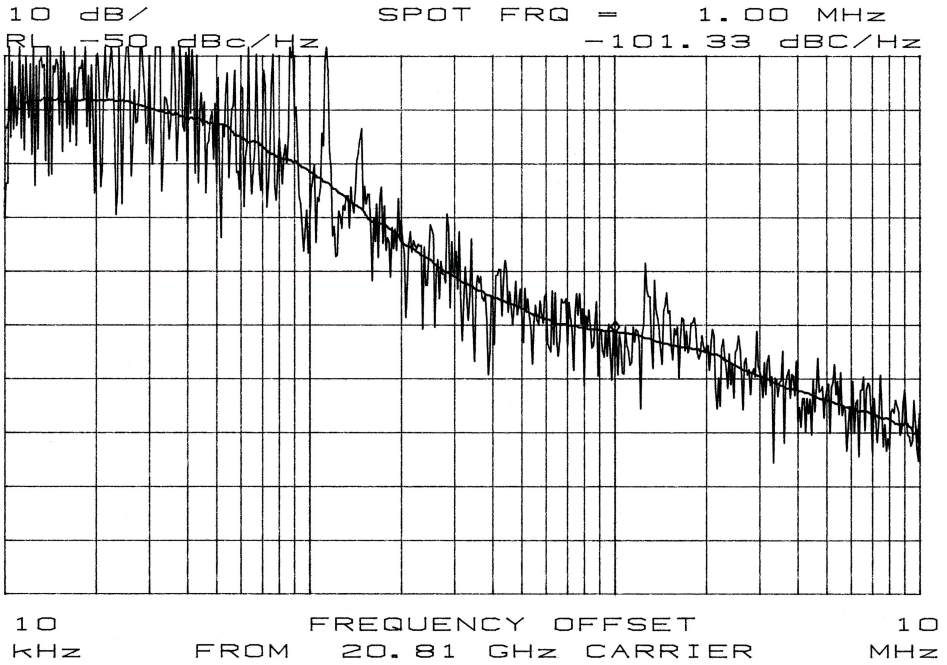


Fig.17. Measured phase noise of the 20 GHz VCO at 1 MHz from the carrier [18].

4. Technology Choices

At 10 Gb/s, it has been possible to implement most of these analog and digital functions, including 5V drivers, in a production GaAs HBT process [1]. In general, PLL and CDR circuits were initially implemented using discrete components. More recently they have been integrated in either Si CMOS or SiGe bipolar/BiCMOS processes, even for 40 Gb/s systems [2−4,20−21].

III−V HEMTs and MESFETs have been the technology of choice for modulator drivers at 10 Gb/s [1] and 40 Gb/s [26]. 10 Gb/s receivers and transceivers have been demonstrated in SiGe HBT processes and some are now commercially available [2,4−5]. Separate TIAs and 3 V laser/modulator drivers have been fabricated in Si bipolar or SiGe HBT technologies [19]. Receivers, transmitters and transceivers, clocked at 5 GHz [6] or at 10 GHz [7], have also been realized in 0.18 μm SOI−CMOS, or 0.18 μm CMOS, respectively, but it is highly probable that 10 Gb/s 3V or 5V drivers will not be realizable in present or future generation Si CMOS. GaAs HBTs and p−HEMTs will retain the 5V modulator driver markets in long−haul SONET/SDH applications.

For 10 Gb/s serializer−deserializer (SERDES) functions operating at or below 3.3V supply, 0.13/0.18 μm CMOS and second generation SiGe BiCMOS (f_T = 70 GHz, f_{MAX} = 80 GHz) have become the technologies of choice. 10 Gb/s short to medium reach applications require the most cost effective high performance technology available. As illustrated in Figs 18−19, for f_T values beyond 80 GHz, the impact of the transistor speed on the rise/fall time of the 10 Gb/s eye diagram at the output of a packaged SERDES diminishes. However, the improvement in the overall deterministic and random jitter is still noticeable with every new technology generation.

SiGe BiCMOS is a technology that has been in high volume production for the last 3 years, driven by consumer wireless applications and given the more relaxed lithography, is very cost effective. It is perfectly suited for analog functions at 10 Gb/s because of the high speed (SiGe) bipolar transistors and CMOS for some control function implementation. From the point of view of implementing large amounts of digital logic, CMOS is crucial. For more complex applications where the SERDES function is integrated with large digital processing functions such as Forward Error Correction (FEC), 0.13 μm CMOS is needed to keep die size and power consumption as low as possible. However, such a CMOS process is higher cost than conventional "digital" CMOS processes because it also has to integrate high quality varactor, MIM capacitor and thick top metal inductors.

OC−768 circuits require rise/fall times below 10 ps and random jitter values below 0.25 ps rms. The integration of low−phase noise VCOs with very wide tuning range and adequate output power at 40 GHz continues to be a problem, irrespective of the technology. The first commercial 40 Gb/s systems will have lower levels of integration and reduced functionality using 20 GHz rather than 40 GHz clocking schemes [20−21,23]. A combination of technologies, such as InP HBTs for the highest speed sections and CMOS or SiGe BiCMOS for the lower speed sections of the system, is the most likely implementation. Third generation SiGe BiCMOS (> 170 GHz f_T, f_{MAX}) will take over the SERDES function as the technology matures and volumes pick up. Modulator driver functions will continue to be implemented in GaAs p/m−HEMT technologies, the only ones that have proven capable of accommodating large voltage swings reliably at 40 Gb/s and beyond.

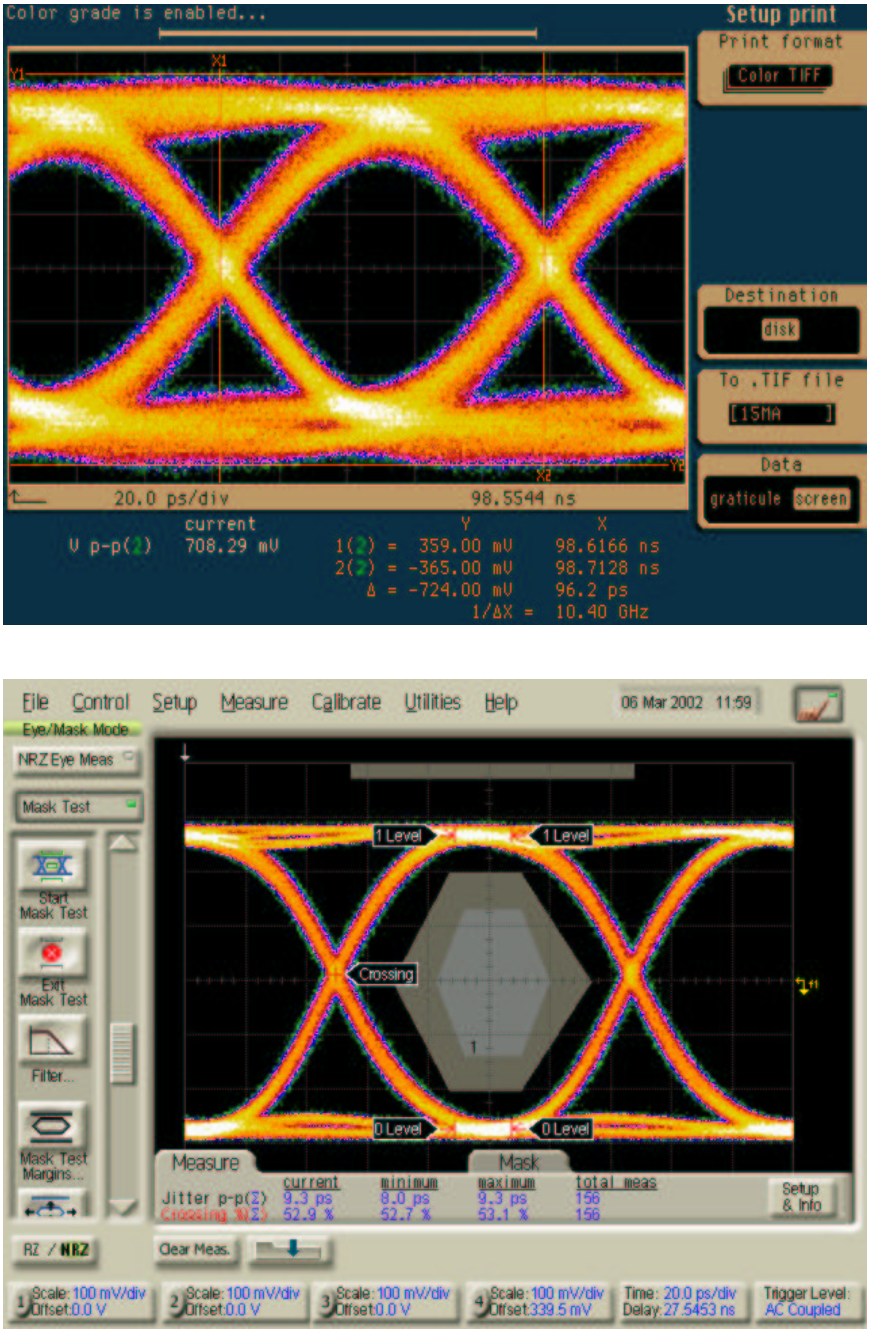
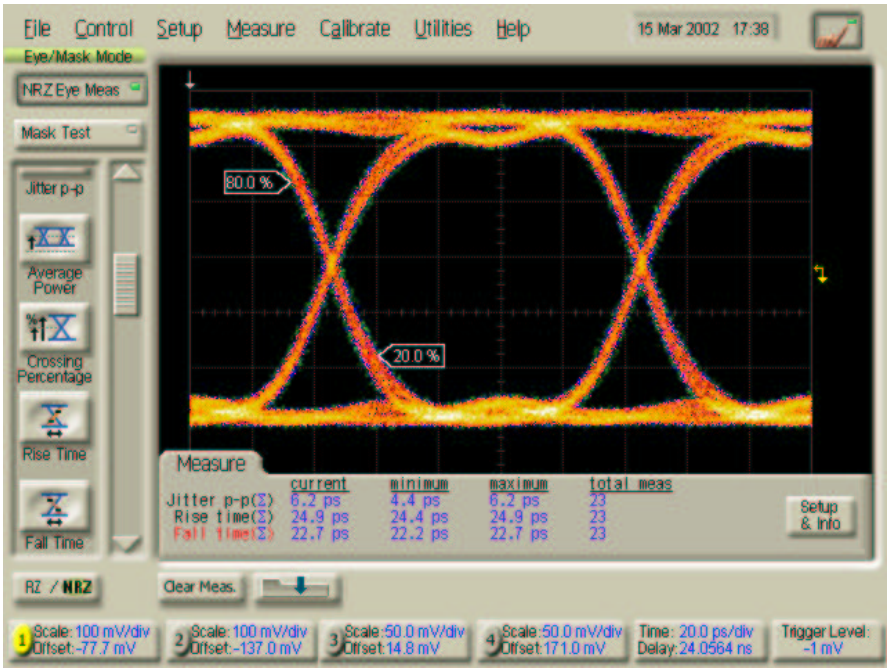


Fig.18. Measured 10.3 Gb/s eye−diagrams at the transmitter output for a packaged SERDES fabricated in a SiGe BiCMOS process with: a) npn f_T = 45 GHz and f_{MAX} = 45 GHz; b) npn f_T = 70 GHz and f_{MAX} = 80 GHz.



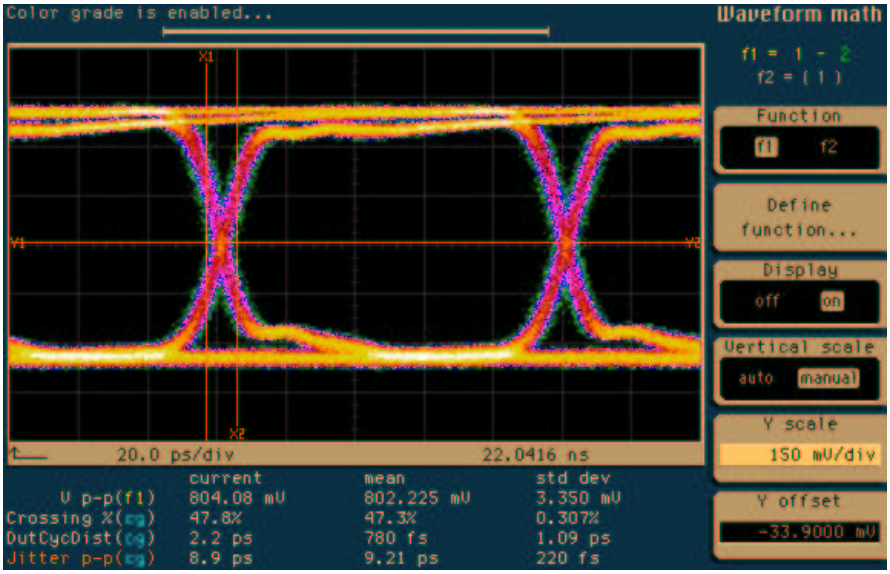


Fig.19. Measured 10.7 Gb/s eye−diagrams for an output driver fabricated in:
a) a SiGe BiCMOS process with npn f_T = 160 GHz and f_{MAX} = 150 GHz and mounted in a PBGA package
b) an InP HBT process with f_T = 170 GHz and f_{MAX} = 150 GHz and measured on wafer (no package).

5. Examples of 10 and 40 Gb/s Circuits

5.1. *10 Gb/s Transimpedance−limiting amplifier*

Fig. 20 shows the block diagram of a single−chip transimpedance limiting amplifier (TIALA) for OC−192 SONET/SDH STM−64 and 10 Gb/s Ethernet (IEEE802.3ae, 10GE) applications with data rates up to 12.5 Gb/s. The block diagram combines a single−ended TIA stage, a multi−stage limiting amplifier, an output buffer with a gain of 1.5, a feedback amplifier for dc offset cancellation, a peak detector for monitoring the input signal, a loss−of−signal (LOS) circuit with adjustable threshold, and a bandgap reference. The TIA stage has 500 Ω transimpedance gain and was designed to minimize the equivalent input noise, while maintaining good linearity for the entire range of input currents: 25 μAp−p to 2 mAp−p. It operates in linear mode and has a bandwidth greater than 8 GHz over all process, supply and temperature corners. The limiting amplifier stages consist of differential inverters with optional three−terminal inductor peaking and emitter followers. The CAZ1 pad can also be used to externally adjust the slicing level [27] at the input of the limiting amplifier between 20% and 80% of the eye height. The LOS block features a hysteresis comparator with low−voltage TTL outputs. The threshold of the LOS circuit is adjustable via an external potentiometer placed between the VREF, VSET and GND pads. The entire circuit draws 60 mA from a single 3.3 V supply.

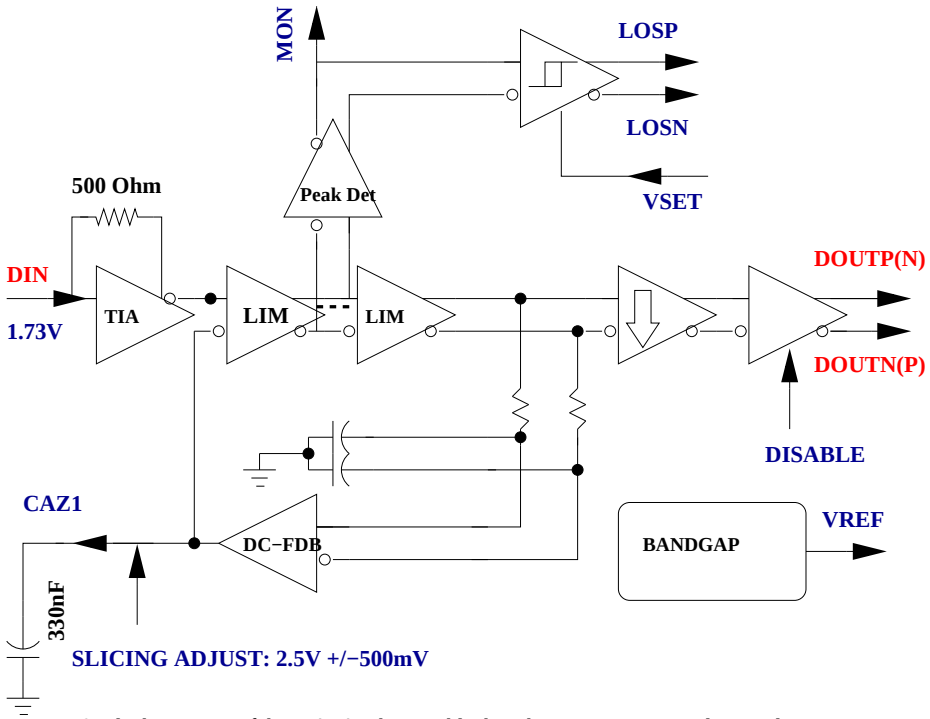


Fig.20. Block Diagram of the TIALA. The gain block with an arrow pointing down indicates an emitter−follower stage.

The circuit was fabricated in two successive generations of SiGe BiCMOS technologies with 0.35 μm and 0.25 μm feature sizes, respectively. The main features of the two processes are described in Table 2, together with the TIALA performance. The 1.1x1.3mm^2 TIALA die is shown in Fig. 21 and has over 400 npn/MOS transistors, inductors for peaking, and MIM capacitors for bias de−coupling filters. On−chip resistively matched high impedance transmission lines and pn junctions [5,17] are employed to ensure high input−output isolation (S_{12} < −60 dB) as required by the small die size and high gain (S_{21} > 40 dB) of the circuit. Because of the very large gain, the TIALA operates in limiting mode even at input currents as low as 30 μAp−p.

Table 2. 10Gb/s TIALA Technology and Circuit Performance

Parameter	***0.35 μm BiCMOS***	***0.25 μm BiCMOS***
SiGe npn peak f_T @ V_{CE} = 1 V	45 GHz	75 GHz
SiGe npn peak f_{MAX} @ V_{CE} = 1 V	50 GHz	80 GHz
peak f_T current density	1 mA/μm^2	3 mA/μm^2
BV_{CEO}	3.5 V	2.8 V
TIALA rise/fall time	30 ps	25 ps
Imin @BER 1E−12, 10.7 Gb/s R = 0.9	37 uAp−p −16.5dBm	25 uAp−p −18.5 dBm
Imax @BER 1E−12, 10.7 Gb/s	3 mAp−p	2 mAp−p
Duty Cycle Distortion	<8 ps	<8 ps
TIA bandwidth	>8 GHz	>8 GHz
TIALA small signal bandwidth	5.5 GHz	9 GHz

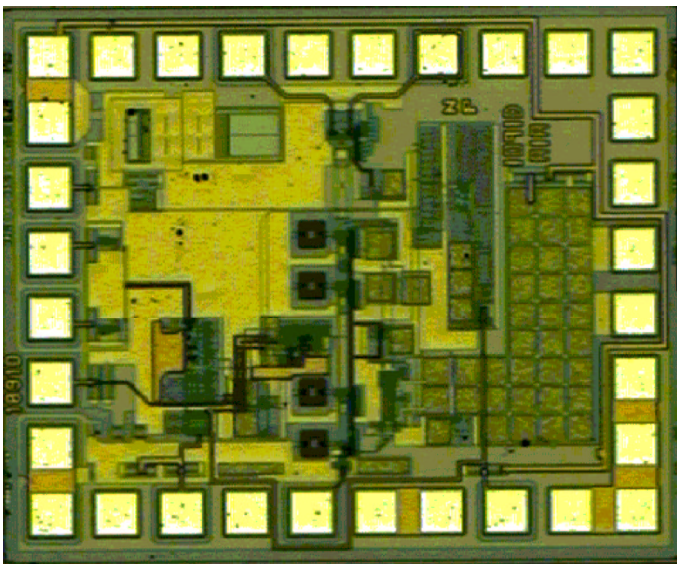


Fig.21. Layout the of the 0.35 μm SiGe BiCMOS TIALA.

Fig. 22 shows the measured single−ended small signal power gain. Also plotted is the output return loss for different loads on the input pad. It is better than −10 dB up to 20 GHz. Because the input impedance of the TIALA is almost 50 Ω, S_{11} is better than −10 dB. This allows for the circuit to be fully testable, including sensitivity, through electrical measurements only, by directly applying the signal from the Bit−Error−Rate−Tester (BERT).

Fig. 23 reproduces the on−wafer measured eye diagrams at 10.7 Gb/s for an input current level of 30 μAp−p and a pseudo−random−bit−signal PRBS pattern of 2^{31}−1. The output swing is limited to 300 mVp−p per side for input currents between 25 μAp−p and 3 mAp−p. The performance parameters summarized in Table 2 indicate that, as long as the TIA bandwidth remains unchanged, the process speed and small signal bandwidth of the entire TIALA only impact the sensitivity and, due to the limiting mode of operation, to a less extent the rise/fall times and data rate of the circuits. The peaking inductors were eliminated from the limiting amplifier stages in the case of the faster process implementation.

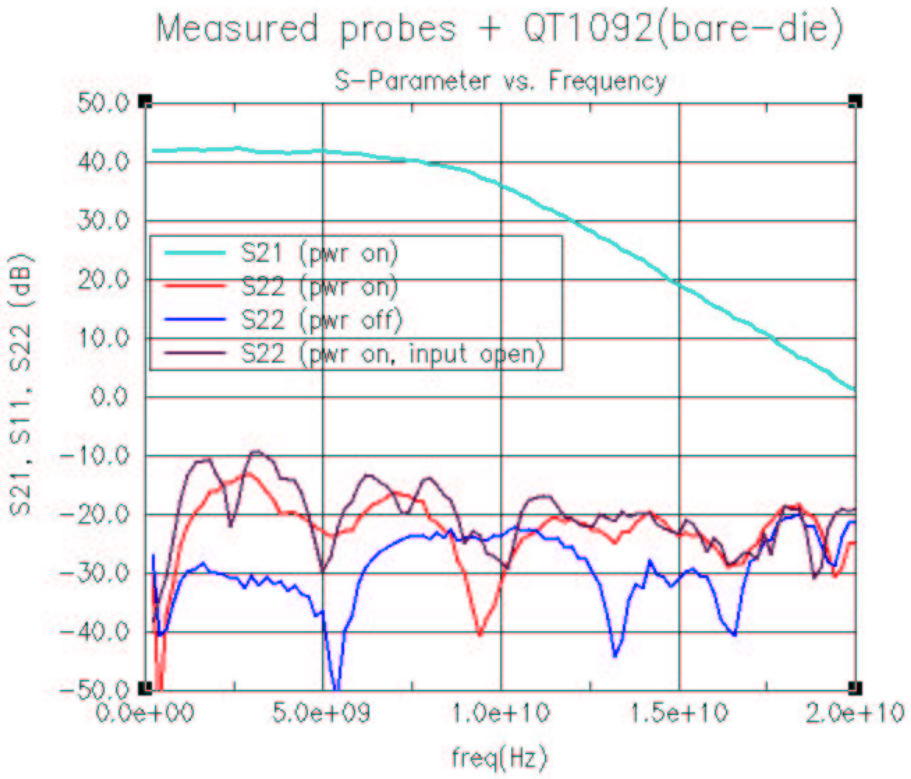


Fig.22. Measured small signal (Pin=−65 dBm) bandwidth and S parameters for the 0.25 μm SiGe BiCMOS implementation.

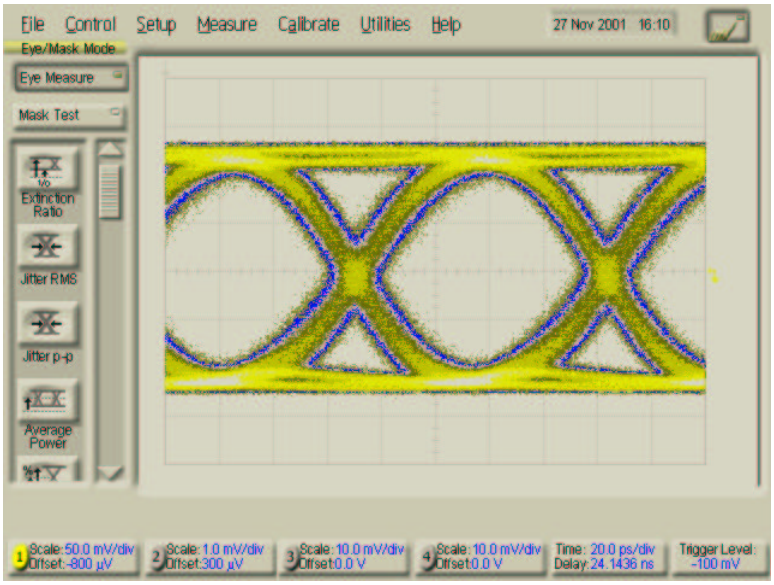


Fig.23. Measured 10.7 Gb/s eye−diagram with 30 µAp−p input for the 0.25 µm SiGe implementation. The scales are 20 ps/div. and 50 mV/div, respectively.

5.2. *40 Gb/s Transimpedance−limiting amplifier*

Figs. 24 and 25 show the block diagram and layout, respectively, of a 40 Gb/s TIALA implemented in an InP HBT process. The circuit integrates more than 300 HBTs on a single 1x1.8mm^2 die, while consuming only 550 mW from a 3.3 V supply. The measured on−wafer differential eye diagram at 42 Gb/s is illustrated in Fig. 26 for an input current level of 500 µAp−p and a $2^{31}-1$ PRBS pattern. The output swing is limited to 400 mVp−p per side for input currents between 100 µAp−p and 3 mAp−p.

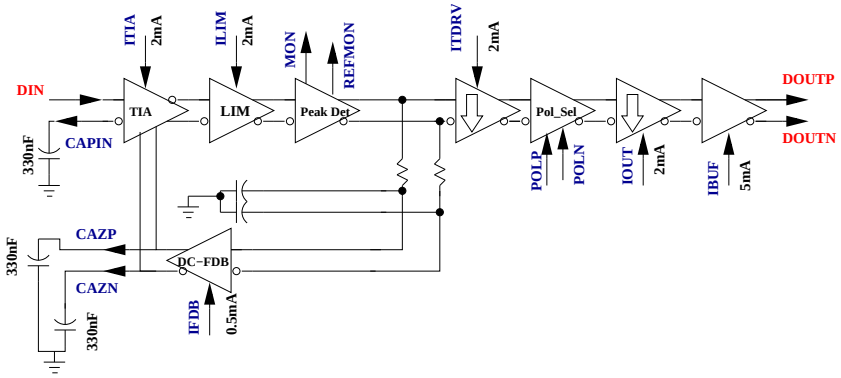


Fig.24. Block diagram of the 40 Gb/s InP HBT TIALA

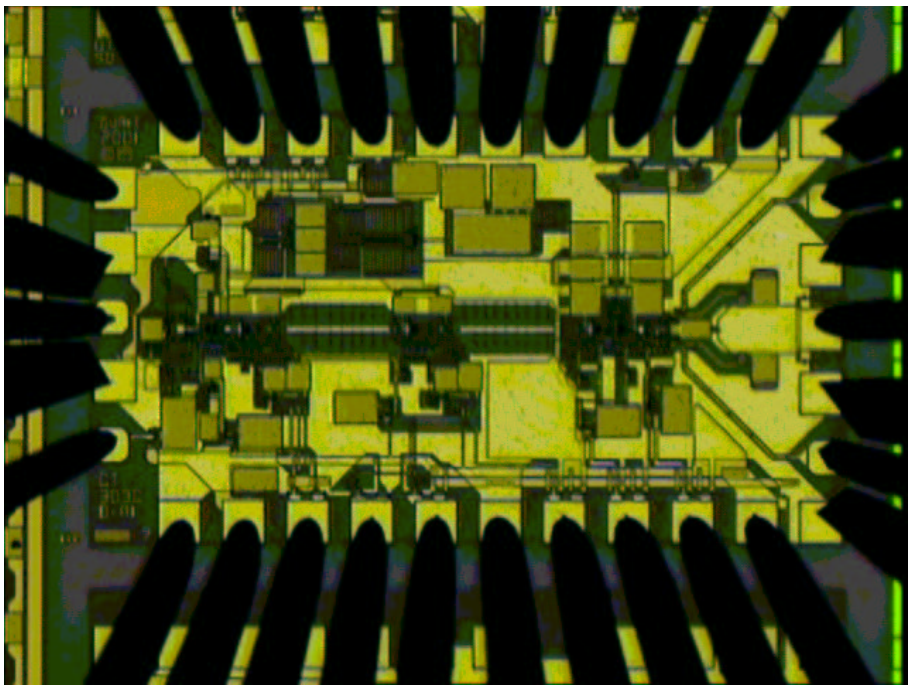


Fig.25. Layout of the 40 Gb/s InP HBT TIALA

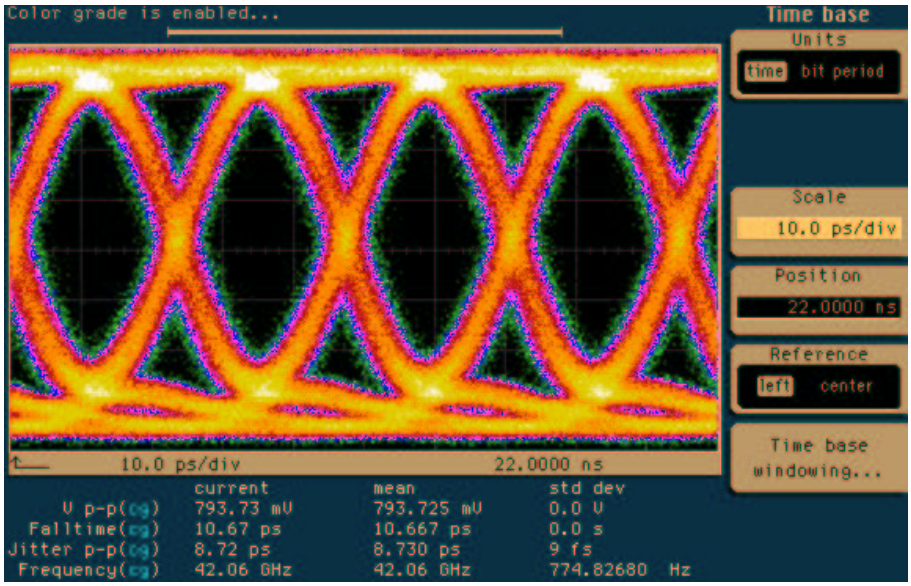


Fig.26. Measured TIALA 42 Gb/s differential eye−diagram with 0.5 mAp−p input. The scales are 10 ps/div. and 100 mV/div, respectively.

5.3. *10 Gb/s Driver.*

The block diagram of a differential output driver with programmable wave shape is illustrated in Fig. 27. It features output swing control between 250 mVp−p per side and 800 mVp−p per side into 50 Ω loads, up to 30% separate positive and negative peaking control, as well as pulse−width (or duty−cycle) control. As in the case of the 10 Gb/s SiGe BiCMOS TIALA, simple building blocks using differential inverters and emitter followers are employed.

The pulse−width (DCD) control block is implemented as shown in Fig. 12. In order to separately control the output signal amplitude, the amount of positive, and the amount of negative pre−emphasis (or peaking), the signal is split in three parallel paths. The two bottom digitally differentiate the rising and falling edge, respectively, of the data signal, as illustrated with dotted triangles in the block diagram. Each path terminates with an open−collector differential inverter featuring an adjustable bias current source which controls the amplitude of the signal for that path. The collectors of all three inverters (one for each path) are tied together in a summing 50 Ohm resistive load. To ensure the proper alignment of the signals, the delays along each path must be matched across process corners and temperature.

The chip operates from a single positive 3.3 V supply with a power consumption of 0.5 W for a midrange output swing of 500 mVp−p per side. It has over 3000 HBTs and MOSFETs and is fabricated in a 0.35 µm SiGe BiCMOS process. Fig. 28 presents the on−wafer measured 10.3 Gb/s eye−diagrams with a 2^{31}−1 PRBS pattern at a single−ended output demonstrating 800 mVp−p per side and peaking control.

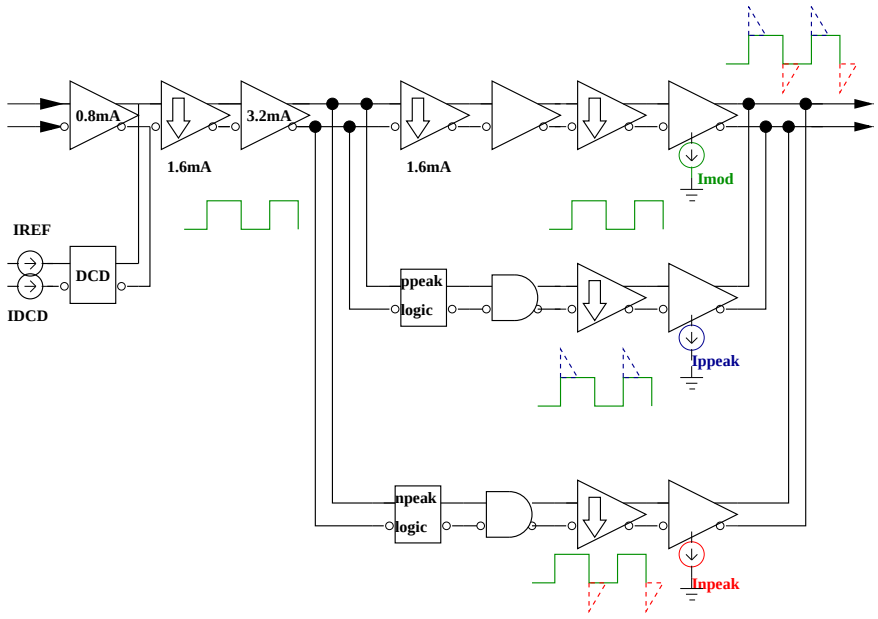


Fig.27. 10 Gb/s output driver schematic. The gain block with an arrow pointing down indicates an emitter−follower stage. The signal shape at various stages is also illustrated.

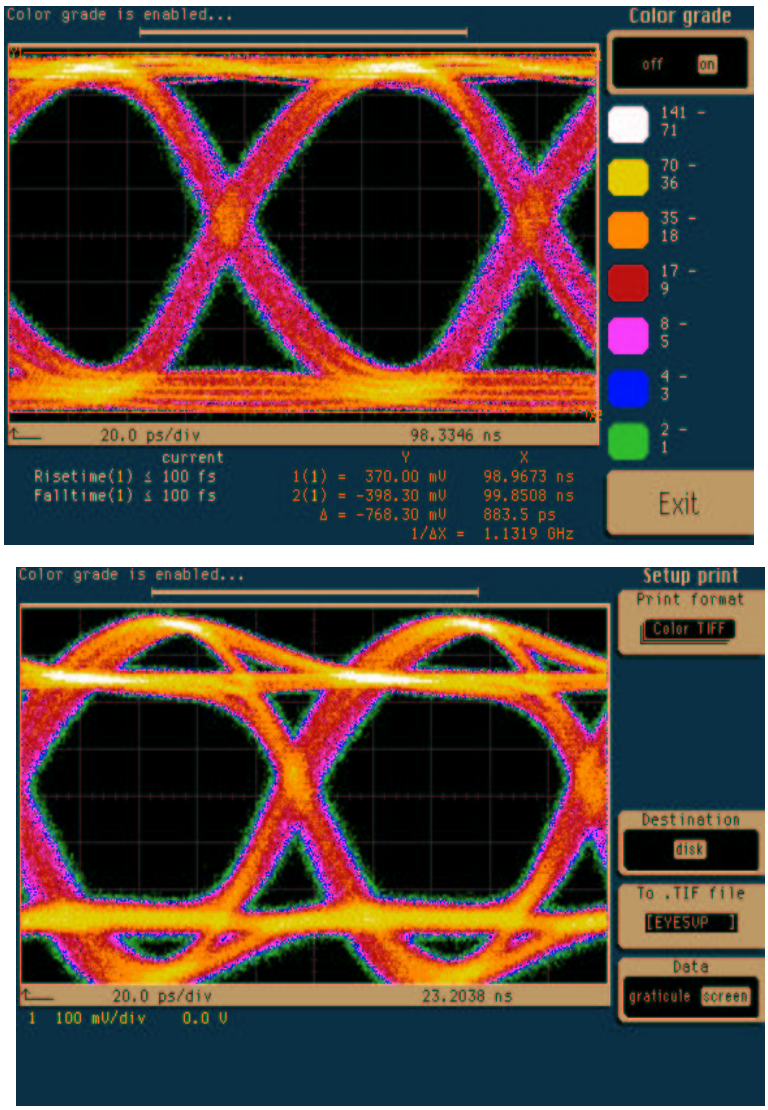


Fig.28. On wafer measured 10.3 Gb/s eye−diagrams for a driver fabricated in a 0.35 µm SiGe BiCMOS process with npn f_T = 45 GHz and f_{MAX} = 45 GHz. a) without pre−emphasis, b) with both positive and negative pre−emphasis. The scales are 20 ps/div. and 100 mV/div, respectively.

5.4. *40 Gb/s Driver.*

The block diagram of a 40 Gb/s Electro−Absorbtion (EA) modulator driver, shown in Fig. 29, features three limiting amplifier blocks: a lumped input block, a middle lumped limiting amplifier with adjustable duty cycle (pulse width) and a 5−stage distributed

limiting amplifier block. The lumped limiting amplifier blocks, as well as the sections of the distributed amplifier have a similar topology, consisting of double source follower stages and a differential inverter, as in Fig. 14(a) More details can be found in [26]. The entire driver operates from a single −5.2 V supply with a gain of at least 16dB and limits the output swing to 3 Vp−p per side for input signals larger than 0.7 V p−p per side. The differential outputs are DC−coupled to the EA modulator and to an external 50 Ω load, respectively. The DC level at the two differential outputs, also called the DC output offset, is adjustable between −0.75 V and −2.25 V. This provides flexibility in biasing the EA modulator. A differential drive Mach−Zender modulator can also be DC−coupled to the differential outputs of the driver.

The die, shown in Fig. 30, is 60 μm x 1.95 mm x 3.99 mm and is fabricated in a 0.15 μm GaAs p−HEMT process with f_T of 110 GHz and f_{MAX} of 180 GHz.. The process features one metal layer, airbridge and back−side via, interdigitated p−HEMTs with more than 6 V breakdown, interdigitated Schottky diodes, epitaxial resistor (110 Ω/sq) and MIM capacitor. The maximum permissible junction temperature is 120 °C. The measured 42 Gb/s differential eye−diagram with 3 Vp−p per side is shown in Fig. 31.

6. Conclusions

The main semiconductor technologies which vie for the implementation of highly integrated 10 Gb/s and 40 Gb/s PHY ICs have been compared based on system and circuit block requirements. Important aspects related to active and passive device scaling and modeling were addressed demonstrating excellent accuracy when compared to experiments. Specific trade−offs in the implementation of digital and analog building blocks in silicon and III−V technologies were discussed. In the case of basic digital building blocks, circuit topologies which best take advantage of the features of a particular technology were illustrated using FETs as well as bipolar transistors. Finally, fully featured 10 Gb/s and 40 Gb/s transimpedance limiting amplifier and laser/modulator driver circuits fabricated in SiGe BiCMOS, InP HBT and GaAs p−HEMT processes were described.

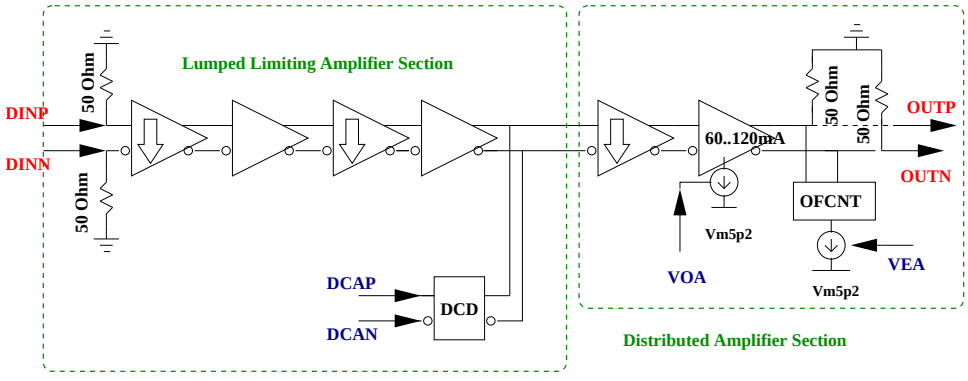


Fig.29. Block diagram of a 40 Gb/s SERDES EA modulator driver with pulse−width, output amplitude and dc offset control. The gain block with an arrow pointing down indicates a source−follower stage.

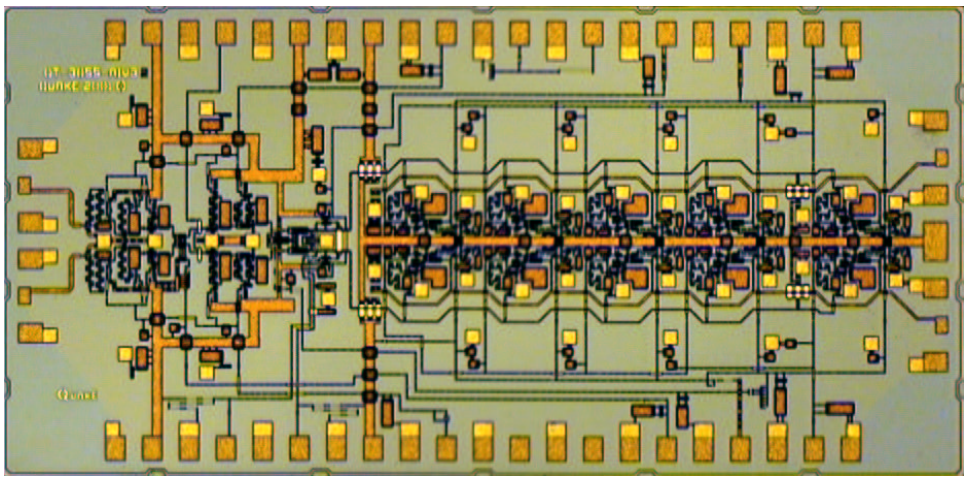


Fig.30. Layout of the 40 Gb/s EA modulator driver.

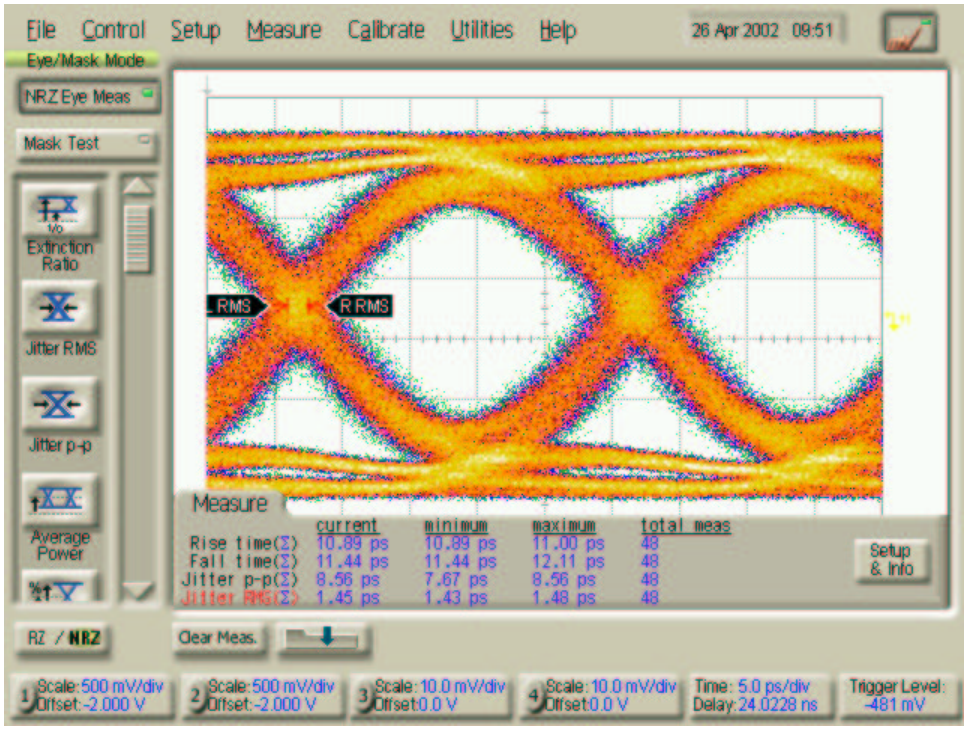


Fig.31. Measured 42 Gb/s differential eye−diagram with 3 Vp−p output swing per side. The scales are 5 ps/div and 500 mV/div, respectively.

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