RF and Thermal Considerations of a Flip-Chip Integrated 40+ Gb/s Silicon Photonic Electro-Optic Transmitter

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***Abstract*—We demonstrate a flip-chip integrated electro-optic transmitter incorporating a high-swing CMOS driver and silicon photonic Mach–Zehnder modulator, and discuss the RF and thermal characteristics of the assembly. The transmitter showed a dynamic extinction ratio of 8 dB, which is the highest to date for 40+ Gb/s-class transmitters using CMOS drivers with silicon modulators. The input reflection coefficient of the module was mostly determined by the input electrical lines, solder bumps, and driver, while the electro-optic transfer function was mostly set by the Mach–Zehnder modulator. Despite the high power consumption of the driver and modulator (553 mW) and the close proximity between the electronic and photonic dies, the thermal simulations show that heat can be efficiently sunk from the bottom side of the silicon photonic die.**

***Index Terms*—Driver circuits, flip-chip integration, integrated optics, optical modulators, silicon photonics.**

I. Introduction

HIGH bandwidth silicon (Si) optical modulator technology has evolved rapidly over the past decade [1]–[7]. Most typically, carrier depletion in a PN junction built into a Si rib waveguide is used to modulate the refractive index via the free carrier plasma dispersion effect. Lateral [5]–[7], vertical [8], interdigitated [9], [10], and U-shaped [11]–[14] PN junctions have been demonstrated for Si carrier depletion Mach-Zehnder modulators (MZMs) at non-return-to-zero (NRZ) bit rates up to 60 Gb/s [7]. Among the variety of PN junction geometries, the lateral PN junction phase-shifter is the most mature and commonly used. Due to the low capacitance and moderate overlap between the depletion region and the optical mode, the lateral PN junction phase-shifter exhibits a modest $V_\pi \cdot L$ of around 2.5 V·cm in the C band, but has the lowest propagation loss, typically around 10 dB/cm [5]. Electro-optic (EO) bandwidths up to 41 GHz have been demonstrated for Si MZMs with lateral PN junctions [15].

The maturing of Si optical modulator device performance is spurring the development of drivers and electronic-photonic integration approaches. A central aim of Si photonics is the dense and low-cost co-packaging of integrated electronic circuits with photonic circuits. For Si traveling-wave MZMs, the typical phase-shifter efficiencies necessitate high drive signal swings of several volts, which are not generally compatible with conventional complementary metal oxide semiconductor (CMOS) drivers. While silicon-germanium (SiGe) BiCMOS drivers have been investigated [16]–[18], the demonstrated extinction ratios (ERs) have been $<$3 dB at 56 Gb/s [17], [18], which are prohibitive for longer distance communication and advanced modulation formats [19]. Recent progress in SiGe BiCMOS drivers has shown high voltage swings up to 4.8 V_{pp} [20], [21], but the integration of these SiGe BiCMOS drivers with optical modulators at 50+Gb/s data rates is yet to be shown. With segmented electrodes, ERs of 7.1 dB at 25 Gb/s can be achieved without equalization [22], but the precise timing control required between the multiple driving signals become more challenging with increasing symbol rate. To integrate an electronic driver with a Si photonic die, three-dimensional (3D) integration using solder bump or copper pillar flip-chip bonding offers the highest integration density and the least parasitics (e.g., loss, capacitance, delay) compared to approaches using wire-bonding or interposers [23]. However, the close proximity between the electronic and photonic dies in 3D integrated packages leads to concern over thermal management.

In [24] and [25], we reported a flip-chip integrated EO transmitter with a record-high ER for 40+ Gb/s operation that comprised a lateral junction Si MZM and a 28 nm CMOS

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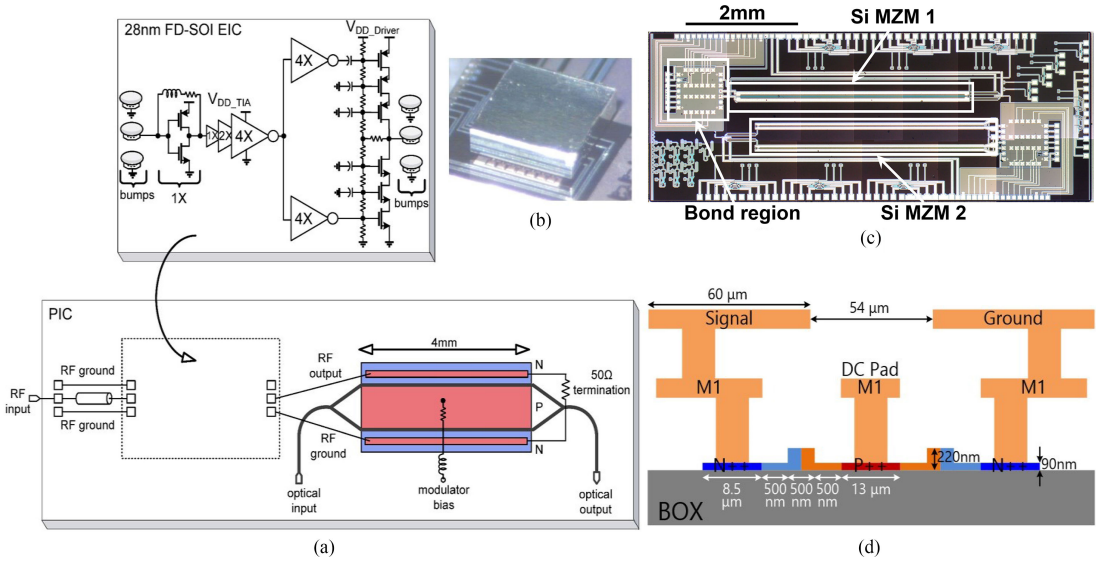

Fig. 1. (a) Circuit schematic of the EIC bonded onto the PIC. (b) Optical micrograph of the bond region after flip-chip bonding. (c) Optical micrograph of half of the photonic die before flip-chip bonding. Each PIC has 4 Si MZM designs and 2 of them are labeled in the figure. (d) Cross-section schematic of the MZM electrode configuration reproduced from [24], [25].

driver. The electronic integrated circuit (EIC) was fabricated in the STMicroelectronics 28 nm ultra-thin body and buried oxide (UTBB) fully depleted silicon-on-insulator (FD-SOI) CMOS technology [26], and the photonic integrated circuit (PIC) containing the Si MZM was fabricated in a multi-project wafer shuttle at A*STAR IME [27]. Both the EIC and PIC tapeouts were coordinated by CMC Microsystems. Fig. 1(a) shows a cartoon of the circuit schematic of the EIC flip-chip bonded with the PIC using solder bumps. Fig. 1(b) shows the bond region after flip-chip bonding using a custom die-to-die solder bump process at CVInc, and Fig. 1(c) depicts the optical micrograph of half of the photonic die before the bonding. The cross-section of the modulator electrode configuration is reproduced from [24], [25] and shown in Fig. 1(d). A full photonic die (with dimensions of 3.2 mm $\times$ 16 mm) contained 4 Si MZMs and served as the interposer for the assembly. The EIC had a footprint of 1 mm $\times$ 1 mm, and it was capable of supplying high voltage swings of up to 5.2 V_{pp} at 40 Gb/s and 4.2 V_{pp} at 60 Gb/s to a 50 Ω load [26].

In this article, expanding upon the results reported in [24]–[26], we show the RF design and simulations of the Si MZM and the integrated assembly, explain the heat transfer and dissipation between the EIC and PIC, and report a record-high ER of 8 dB at 50 Gb/s. The article is organized as follows. In Section II, we describe the design of the Si MZM. Section III illustrates the simulation of the flip-chip bonded assembly and the characterized performance. Section IV presents the thermal dissipation analysis of the bonded assembly.

II. Silicon Mach–Zehnder Modulator

For the 3D integrated EO transmitter in [24] and [25], the EIC has been presented in [26], but the design of the MZM has not been previously described in detail. Fig. 1(a) shows a schematic of the Si MZM. It used the standard lateral PN junction in the A∗STAR IME Si photonic process [5], [28]. It consisted of two 3 dB multimode interference (MMI) couplers, 4 mm long phase-shifters and a 500 μm long thermal tuner implemented in the N-doped Si waveguide. The top metal layer of the electrodes was 60 μm wide and separated by 54 μm, and the lower metal layer of the electrodes was 23.5 μm wide and separated by 23 μm. Lensed fibers with a 2.5 μm spot diameter were used to couple light into and out of the MZM. The modulator insertion loss was measured to be 7.1 dB, and the average $V_\pi \cdot L$ of the two arms was measured to be 2.5 V·cm, similar to the values in [5].

The traveling-wave electrodes for the Si MZM (Si MZM 1 in Fig. 1 (c)) are in the single-drive push-pull configuration [29], [30]. From the electrical point of view, the MZM was formed as coplanar striplines (CPS) terminated with a 50 Ω resistor. In the bonded assembly (to be discussed in Section III), only one of the three available transceiver channels in the EIC was connected to the modulator. The modulator in the bonded assembly did not operate in push-pull mode because the output signal from the EIC was DC-coupled, such that the RF output in Fig. 1(a) had a DC offset. This would lead to an additional current path from the RF output to the RF ground through the 50 Ω termination resistor. A differential drive arrangement would have enabled true push-pull operation and avoided the DC current flow through the termination. Such an arrangement can be seen in Fig. 1(c) for Si MZM 2 but has yet to be bonded to an EIC.

A. PN Junction Capacitance

The performance of the traveling-wave electrodes depends on the lateral junction resistance and capacitance. In the single-drive push-pull configuration, the DC bias is isolated from the RF signal using an on-chip resistor and inductor [29], [30], so the junction resistance and capacitance cannot be measured directly. Using separate test structures on the PIC, we measured the resistance and capacitance of the PN junction using a source meter and LCR meter (Agilent E4980A). Fig. 2(a) shows the measured capacitance as a function of the reverse bias voltage,

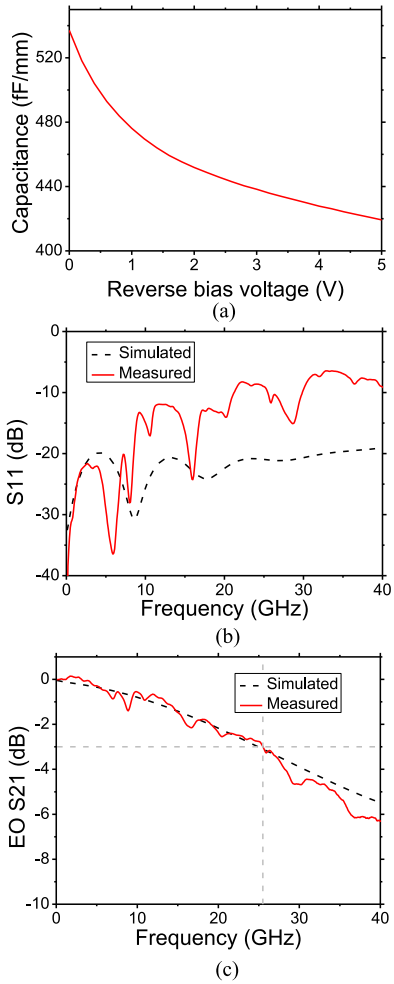

Fig. 2. (a) Measured lateral junction capacitance as a function of the reverse bias voltages. Measured and simulated S11 (b) and EO S21 (c) of the MZM at −2 V bias.

which is similar to the values in [5]. The measured junction series resistance was 7.2 Ω·mm.

B. Traveling-Wave Electrode Design and Characterization

The design of the traveling-wave electrodes was divided into two parts. The first part was to calculate the RLGC model of electrodes. Using ANSYS HFSS, we simulated the *S* parameters of the electrodes and converted them into a RLGC model. The high resistivity handle wafer (>750 Ω cm) of the PIC was also included in the simulation. The second part was to modify the RLGC model to include the Si PN junction resistance and capacitance [31]. In the single-drive push-pull configuration, both arms of MZM should be loaded to the designed traveling-wave electrodes; hence, the PN junction resistance would be doubled and capacitance halved in the calculation [29], [30]. With the modified model, we calculated the propagation constant and characteristic impedance of the electrodes. The key to the design is to achieve velocity matching between optical and RF signals, impedance matching between device characteristic impedance and termination resistance, and low RF signal

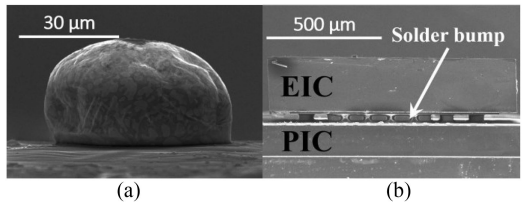

Fig. 3. Cross-section SEM images of (a) solder bump and (b) the bonded assembly. The solder bump diameter is approximately 52.5 μm, and the pitch of the solder bumps is 100 μm.

loss. The RF loss, α (in dB/mm), should meet the 6.4 dB rule: $\alpha(f\,3\text{dB})\cdot L \leq 6.4$ dB, where L is the device length, f_{3dB} is the device EO 3dB bandwidth [32]. We designed the Si MZM to terminate with a 50 Ω impedance formed in the highly N-doped Si slab. The metal layer thicknesses were fixed by the process. Hence, we varied the electrode width and separation to obtain the velocity match, impedance match and low RF loss. The final electrode design was presented in [25].

Fig. 2(b) and (c) show the simulated *S* parameters of the Si MZM assuming an ideal 50 Ω source and load impedance, and the measured *S* parameters. Fig. 2(b) shows the S11 with a −2 V reverse bias. The simulation used the measured PN junction resistance and capacitance at −2 V reverse bias in the electrode RLGC model. The measurement was done using a vector network analyzer (Agilent N5227A) and 50 GHz photodetector (Finisar XPDV2320R). At the low frequency range, the simulated and measured results show good agreement. Beyond 10 GHz, the simulated results are better than the measurement.

Fig. 2(c) shows the simulated and measured EO S21 at −2 V bias. The measured EO 3 dB bandwidth was around 26 GHz when the wavelength was set to be the −3 dB transmission point (i.e., quadrature point) of the optical spectrum. The measurement and simulation show excellent agreement. Since the EIC had a 3 dB bandwidth of 35 GHz with a large signal input [26], the bandwidth of the bonded assembly was not limited by the bandwidth of the CMOS driver. The *S* parameters shown here are for −2 V bias, which is similar to the DC bias applied by the EIC to the MZM.

III. Flip-Chip Bonded Assembly

The PIC served as the bonding interposer and contained the input pads and interconnect for the EIC. Fig. 3(a) shows the cross-section scanning electron micrograph (SEM) of the SnPb (63/37%) solder bumps used in the bonding. The bumps had a nominal diameter of 50 μm, and the diameter of the solder bump in Fig. 3(a) is 52.5 μm. The pitch of the bonds was 100 μm. Fig. 3(b) shows the cross-section SEM of the bond region. No underfill material was used between the electronic and photonic dies. In the assembly, although the MZM was originally designed to be driven differentially, one electrode was connected to ground to accommodate the single-ended topology of the driver.

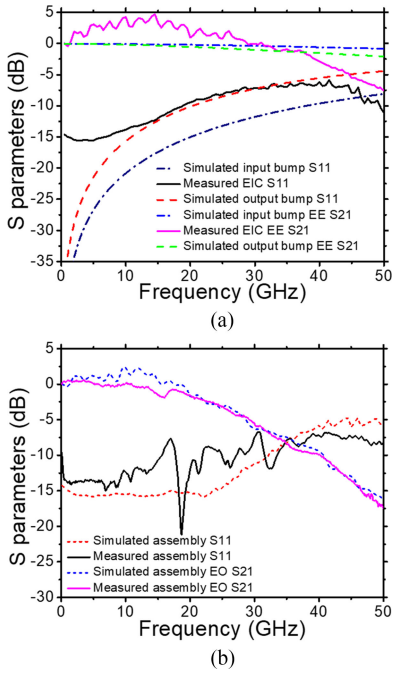

Fig. 4. (a) The simulated S11 and EE S21 of the input/output pads, lines, and bumps, and the measured S11 and EE S21 of the EIC. (b) The simulated and measured S11 and EO S21 of the bonded assembly. The S11 and EO S21 of the Si MZM are in Fig. 2.

A. S Parameter Analysis

Electrically, the flip-chip bonded assembly can be separated into: 1) the input pads, lines, and solder bump, 2) the EIC, 3) the output solder bump, lines, and output pads, and 4) Si MZM with an on-chip termination. Although [24] and [25] show the aggregate performance of the EO transmitter, the modelling of the RF characteristics of the assembly has not been previously reported. Here, the *S* parameters of the input pads, lines and solder bumps, and the output solder bumps, lines and output pads were simulated using ANSYS HFSS. The results were cascaded with the measured *S* parameters of the EIC and Si MZM.

Fig. 4(a) shows the simulated and measured S11 and S21 of the solder bumps and EIC under large signal conditions. In this figure, the S21 of the EIC was shifted down to 0 dB to emphasize its bandwidth and facilitate comparison with the EO S21 and bandwidth. The input RF signal power of the EIC measurement was -20 dBm. The EIC operated in switching mode under large signal conditions and not in linear mode. Cascading these results with the measured *S* parameters of the Si MZM, the S11 and EO S21 of the bonded assembly are computed and shown in Fig. 4(b). The RF reflection of the bonded assembly was mainly dictated by the input pads and lines on the photonic die, the solder bump, and the EIC. The measured small signal S11 of the EIC was better than the large-signal value [26]. However, the large-signal input more closely matches the conditions of the eye diagram measurements. Fig. 4(b) shows good agreement between simulations and measurements. Both the simulations and measurements show an EO S21 -3 dB bandwidth around 24 GHz, which is only slightly degraded compared to the bandwidth of the standalone Si MZM in Fig. 2. The electrical S21 -3 dB bandwidth is 19.5 GHz.

B. Eye Diagrams

Eye diagrams of the bonded assembly were measured using a pattern generator (SHF 78210D, 12104A) and a digital communication analyzer (DCA, Agilent 86100D with 86116C module). The assembly was placed onto a temperature controlled chip-holder held at 24 °C. The signal from the pattern generator was applied to the module through a 60 cm long cable and 40 GHz Ground-Signal (GS) GGB probe with 100 μm pitch. The signal loss at the input of the setup is frequency dependent and exceeds 4 dB at 25 GHz. The modulated optical output from the MZM was amplified using an erbium doped fiber amplifier (EDFA) and then filtered by a tunable bandpass filter (with a 0.8 nm bandwidth in the C band).

Fig. 5 shows the measured eye diagrams using a $2^{31}-1$ pseudo-random bit sequence (PRBS) at 44, 48, and 50 Gb/s respectively. The input laser wavelength was set to 1549.3 nm, corresponding to the MZM quadrature point. Lower noise and wide-open eye diagrams at 36 Gb/s and 40 Gb/s for another integrated assembly have been reported in [24], [25]. For the assembly in Fig. 5, the coupling loss of the edge couplers in the photonic chip was abnormally high at about 17 dB for the two facets. The facet quality may have been compromised during the dicing or the assembly process. The total insertion loss of the MZM (including input and output coupling loss) at the quadrature point was between 27 and 28 dB. The average optical power entering the EDFA was about -19 to -20 dBm, necessitating a high gain from the EDFA. The noisier top rail compared to the bottom rail in the eye patterns was likely due to the higher amplified spontaneous emission (ASE)-signal beat noise from the EDFA. The signal swing at the output of the pattern generator was 0.8 V for Fig. 5(a) and (b), and 1 V for Fig. 5(c) to compensate for the input setup loss and saturate the gain of the EIC. The DC pad of the MZM was held at ground. The DC voltages at the output stage of the EIC, $\mathrm{V_{DD\_Driver}}$, and transimpedance amplifier (TIA) stage of the EIC, $\mathrm{V_{DD\_TIA}}$, are designed to be around 6 V and 1 V, respectively.

In Fig. 5(c), at 50 Gb/s, the $\mathrm{V_{DD\_TIA}}$ and $\mathrm{V_{DD\_Driver}}$ pads were biased from 1.5 V and 6.6 V supplies, respectively. Based on the measured DC currents of 52.69 mA and 71.78 mA drawn from the 1.5 V and 6.6 V supplies, respectively, the worst case power consumption was 553 mW which includes setup losses and modulator load resistance. By matching the measured currents with the simulation of an equivalent circuit model for the bonded assembly that includes 3 to 5 Ω of series resistances between the power supplies and the $\mathrm{V_{DD\_TIA}}$, $\mathrm{V_{DD\_Driver}}$, and ground pads, the actual voltages on the EIC $\mathrm{V_{DD\_TIA}}$ and $\mathrm{V_{DD\_Driver}}$ pads are estimated to be 1 V and 5.1 V, respectively, within the acceptable operation range for the CMOS technology. However, at 5.1 V, the driver output stage does not operate with maximum voltage swing. In [26], the measured output swing when $\mathrm{V_{DD\_Driver}} = 5.1\,\mathrm{V}$ was $4\,\mathrm{V_{pp}}$, less than the maximum possible output swing. The bias supply voltages of the EIC used for the 44 and 48 Gb/s were lower than those at 50 Gb/s.

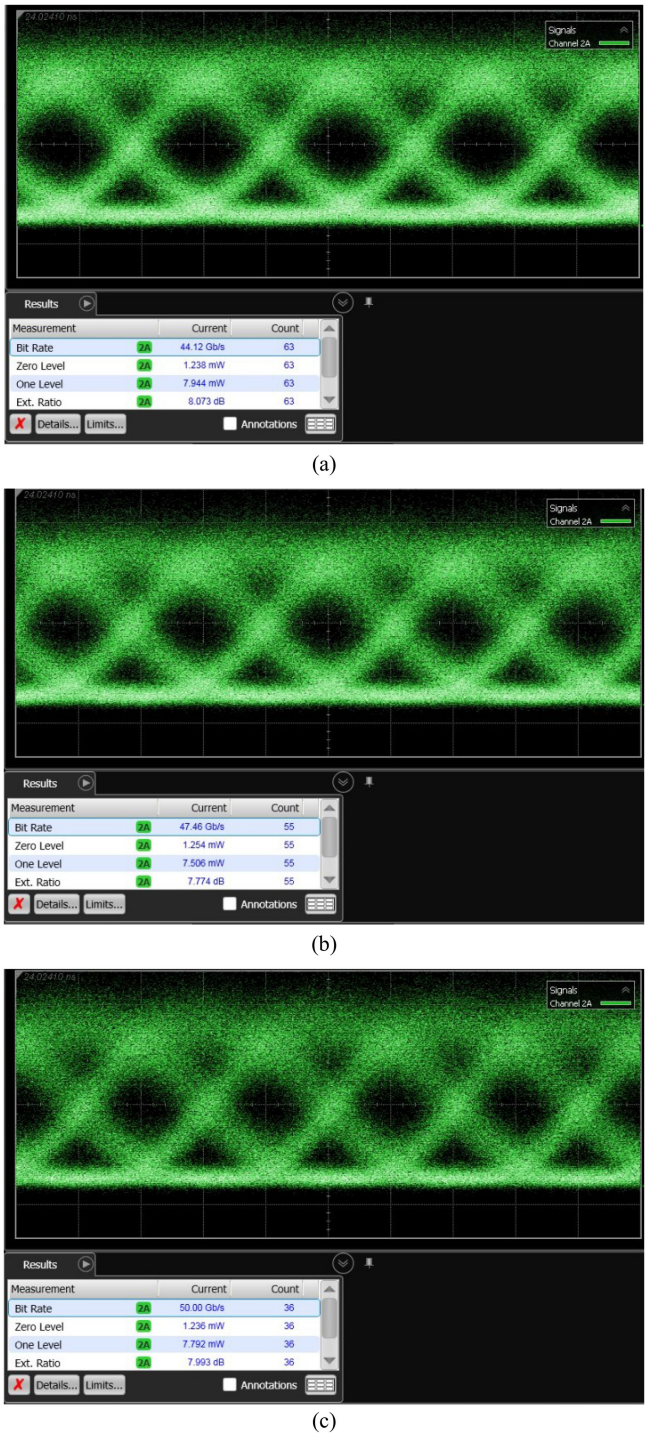

Fig. 5. Measured output eye diagrams of the integrated assembly for a PRBS31 pattern at (a) 44, (b) 48, and (c) 50 Gb/s when the wavelength was set to the −3 dB transmission point of the MZM. The ER in all three cases was about 8 dB.

Compared to the standalone EIC, the total power consumption at 50 Gb/s was roughly 1.84 times higher [26]. Because the output signal from the EIC was DC-coupled, an additional current path from the MZM signal pad to the ground pad was formed through the 50 Ω termination resistor. Based on the equivalent circuit simulations, the DC voltage and

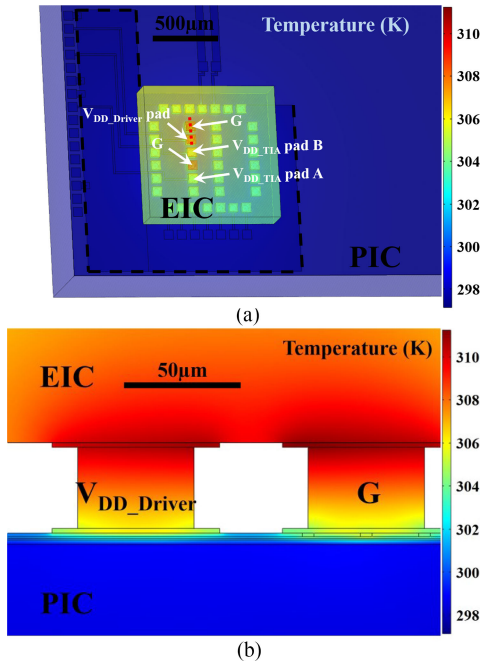

Fig. 6. (a) The simulated 3D temperature profile of the bonded assembly with 345 mW dissipated as heat to the EIC DC pads. (b) The cross-section temperature profile along the red dashed line in (a).

current on the MZM termination resistor are estimated to be 2.6 V and 49.2 mA, resulting in a DC power consumption of 128 mW by the termination resistor. If the MZM was operated in true single-drive push-pull mode using an AC-coupled voltage instead, the termination resistor would not dissipate any DC power, leading to a more power efficient design. For an AC-coupled, 4 V_{pp} square wave pattern, the RF power dissipated by the 50 Ω termination resistor is 80 mW. Therefore, the maximum power dissipated as heat by the EIC was about 345 mW = (553 mW − 128 mW − 80 mW), but at least 10% of it is dissipated on the parasitic series resistances of the setup and assembly. As mentioned in Section II, future improvement of the EO module will focus on using differential drive signals to eliminate the DC current through the MZM and thus reduce the power consumption of the bonded assembly.

IV. Thermal Modelling

A major concern with 3D integration is heat dissipation. To investigate the temperature distribution of our 3D EO transmitter, we conducted thermal simulations of the assembly using COMSOL Multiphysics. The heat source was modelled as $Q_0 = P_0/V$, where P_0 is the power dissipated by the EIC as heat and V is the volume of the source. We consider the worst-case scenario, where $P_0 = 345$ mW. In the simulation, the assembly is placed on a heat sink held at 24 °C. Heat dissipation from the EIC to the PIC is through conduction, while heat dissipation into the surrounding air is through convection.

Fig. 6 shows the simulated temperature of the bonded assembly when 345 mW of power was dissipated as heat on the top surfaces of the EIC Si layer near the V_{DD_Driver}, V_{DD_TIA},

and ground pads. The pads of the EIC are labeled. The temperature of the bottom surface of PIC was fixed to 24 °C. The exposed surfaces were set to have a heat transfer coefficient of 5 W/(m^2·K). The EIC had a 7 nm thick Si layer on the top surface and a 25 nm thick buried oxide (BOX) layer [26], whereas the PIC had a 2.94 μm SiO_2 layer on the top surface (top waveguide cladding) and 2 μm BOX layer. Due to the thin BOX in the EIC, heat can be transferred easily within the EIC. The highest temperature regions were at the top side of the solder bumps due to the low thermal conductivity of air.

In the PIC, a ground plane in the lower metal layer in the Si photonics process under the EIC helped to increase the heat dissipation through the PIC. The ground plane was roughly 2.4 mm^2 in area and is marked by black dashed lines in Fig. 6(a). In the assembly, all of the ground pads for the EIC and on the PIC were connected to this plane through the vias between the two metal layers. With the ground plane, the simulation shows that the hottest part near the bond region under stationary conditions is near the V_{DD_Driver} pad of the EIC, which is at a temperature of about 38 °C, 2 °C lower than in the case without the ground plane. The highest temperature on the PIC in the bond region is about 33 °C, near the pad connected to the V_{DD_Driver} pad. The temperature rise in the PIC is localized. At a distance of 250 μm away from the bond pads, the temperature on the photonic die is already returned to 24 °C.

Due to the DC-coupled output of the EIC in this demonstration, the worst-case power dissipation in the MZM termination resistor, including both the DC and RF powers, is 208 mW (128 mW + 80 mW), leading to a local temperature of 164 °C in the termination. Although this temperature can be tolerated by Si waveguides, a differential driver topology with 4 to 5 V_{pp} differential output swing DC-coupled to a differentially driven push-pull MZM will eliminate the parasitic DC current and reduce the temperature in the termination to 78 °C. A larger area resistor would also reduce this temperature increase and improve the linearity of the termination resistance [15].

The thermal simulations show that in this type of 3D integrated EO electronic-photonic assembly, heat can be dissipated from the bottom (the bottom of the Si photonic chip) with a heat sink. Even with a high power density EIC in close proximity, the maximum temperature increase on the Si photonic chip near the EIC is only about 9 °C, and the maximum temperature difference in the bond region between the EIC and PIC is 14 °C. These temperature variations can be readily managed.

V. Conclusion

We have presented extended RF and thermal analyses of a flip-chip bonded transmitter comprised of Si MZM and FD-SOI CMOS driver. The transmitter performance has been improved compared to [24] and [25], and operation at up to 50 Gb/s with a record-high ER of 8 dB was demonstrated with a power consumption (excluding a laser) of 553 mW (equivalent to 11 pJ/bit). Implementing a more efficient junction geometry, such as a vertical junction [8], interdigitated junction [9], [10], or U-shaped junction [13], [14], would further reduce the power consumption by reducing the drive signal swing. The RF simulation of the Si MZM and bonded assembly shows the RF reflection is mostly dominated by the input pads, electrical lines, bumps on the Si photonic die, and EIC, and the EO S21 was mostly determined by the EIC output and Si MZM. The temperature distribution of the assembly shows that despite the high power consumption, heat can be effectively sunk away from the bottom of the photonic die, which suggests 3D integration can be reliable even with EICs operating at high power densities in excess of 500 mW/mm^2. Future improvement is to implement a differential drive push-pull MZM (Si MZM 2 in Fig. 1(c)) bonded with a differential driver to reduce the power consumption and alleviate heating in the termination.

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