165-GHz Transceiver in SiGe Technology

Ekaterina Laskin, *Student Member, IEEE*, Pascal Chevalier, *Member, IEEE*, Alain Chantre, *Senior Member, IEEE*, Bernard Sautreuil, and Sorin P. Voinigescu, *Senior Member, IEEE*

***Abstract*—Two D-band transceivers, with and without amplifiers and static frequency divider, transmitting simultaneously in the 80-GHz and 160-GHz bands, are fabricated in SiGe HBT technology. The transceivers feature an 80-GHz quadrature Colpitts oscillator with differential outputs at 160 GHz, a double-balanced Gilbert-cell mixer, 170-GHz amplifiers and broadband 70-GHz to 180-GHz vertically stacked transformers for single-ended to differential conversion. For the transceiver with amplifiers and static frequency divider, which marks the highest level of integration above 100 GHz in silicon, the peak differential down-conversion gain is −3 dB for RF inputs at 165 GHz. The single-ended, 165-GHz transmitter output generates −3.5 dBm, while the 82.5-GHz differential output power is +2.5 dBm. This transceiver occupies 840 μm × 1365 μm, is biased from 3.3 V, and consumes 0.9 W. Two stand-alone 5-stage amplifiers, centered at 140 GHz and 170 GHz, were also fabricated showing 17 dB and 15 dB gain at 140 GHz and 170 GHz, respectively. The saturated output power of the amplifiers is +1 dBm at 130 GHz and 0 dBm at 165 GHz. All circuits were characterized over temperature up to 125 °C. These results demonstrate for the first time the feasibility of SiGe BiCMOS technology for circuits in the 100–180-GHz range.**

***Index Terms*—D-band SiGe HBT amplifier, 80-GHz quadrature oscillator, millimeter-wave imaging, 165-GHz transceiver, 180-GHz transformer.**

I. Introduction

As THE electronics industry continues to make progress, higher bandwidth communication is needed to satisfy the requirements of consumer applications. Inevitably, to meet this demand for bandwidth, the front-end radio circuits have to operate at increasingly higher frequencies. Operation at higher frequencies is also beneficial in imaging applications because it enhances image resolution. Furthermore, by employing two widely different frequencies, such as 80 GHz and 160 GHz, an imager can provide more detailed information about the electromagnetic radiation absorption rates and the composition of the materials inside the object being imaged [1]. Along with the higher resolution, 160-GHz transceivers enjoy the advantage of being easily integrated with antennas, whose area becomes sufficiently small to be economically implemented on chip, and formed into arrays. These arrays can be used for active imaging in security and medical applications. In the work presented here, the 160-GHz range was selected due to the relatively low atmospheric absorption at this frequency and because of the prospect of re-using many circuit blocks, such as an 80-GHz PLL, developed for automotive radar transceivers operating at 77 to 79 GHz.

The millimeter-wave (mm-wave) spectrum above 100 GHz has previously been the exclusive domain of III-V MMICs [2]. However, this situation is rapidly changing as some basic circuit blocks have recently been implemented in silicon. For example, mm-wave VCOs operating above 140 GHz have been previously realized in CMOS [3], SiGe HBT [4], and InP [5] technologies. However, amplification and integration at the receiver or transmitter level have not been achieved in silicon at frequencies beyond 110 GHz. This work demonstrates that, thanks to advances in transistor and passive device performance, and by scaling traditional circuit topologies, lumped inductors and transformers, radio transceiver integration is possible in silicon up to at least 180 GHz.

This paper describes in detail the architecture, building blocks, and design methodology employed in the first dual-band 80/160-GHz transceiver and the first 140-GHz amplifier fabricated in silicon technology [6], and presents a new 160–180-GHz transceiver with integrated amplifiers and static frequency divider with significantly improved performance. Furthermore, the oscillator at the core of the two transceivers is the first capable of generating differential signals at 160 GHz, while simultaneously providing quadrature outputs at 80 GHz. As will be shown, employing this oscillator in a system simplifies the clock distribution circuitry and reduces its power dissipation.

II. Transceiver Architecture

To increase the image resolution in active imaging applications, it is customary to employ several receivers and transmitters in an array configuration [7]. Integrating such an array at frequencies above 100 GHz poses a significant challenge in terms of LO distribution, power, and area. One possible system architecture, shown in Fig. 1, relies on generating four quadrature signals at the fundamental frequency (80 GHz) together with a differential signal at the second harmonic (160 GHz). Since only one VCO is involved, all its six outputs can be locked to a single 80-GHz PLL, thus saving power and area. Additional power can be saved by distributing the multiple signals from the VCO passively using transformers. Transformers are very effective at mm-wave frequencies thanks to their small area and efficient conversion of single-ended signals to differential-mode signals. Furthermore, they can be designed to have low loss even in technologies with a "digital" backend.

Recently, our group reported a SiGe HBT transceiver [8], [9] with 4 dB DSB noise figure, 38 dB downconversion gain, and

Manuscript received September 15, 2007; revised January 20, 2008. This work was supported by CITO and NSERC. Fabrication was provided by ST-Microelectronics.

E. Laskin and S. P. Voinigescu are with the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, M5S 3G4 Canada (e-mail: laskin@eecg.utoronto.ca; sorinv@eecg.toronto.edu).

P. Chevalier, A. Chantre, and B. Sautreuil are with STMicroelectronics, 38926 Crolles Cedex, France (e-mail: pascal.chevalier@st.com; alain.chantre@st.com; bernard.sautreuil@st.com).

Digital Object Identifier 10.1109/JSSC.2008.920336

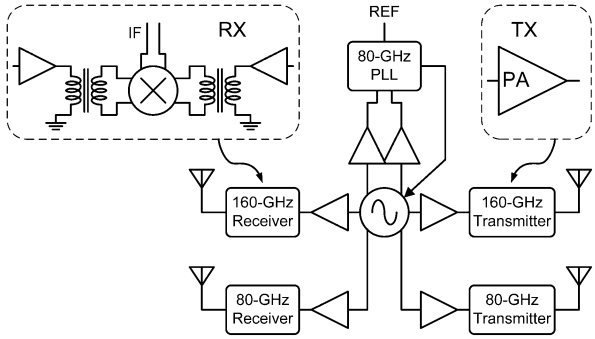

Fig. 1. Dual-frequency transceiver array block diagram.

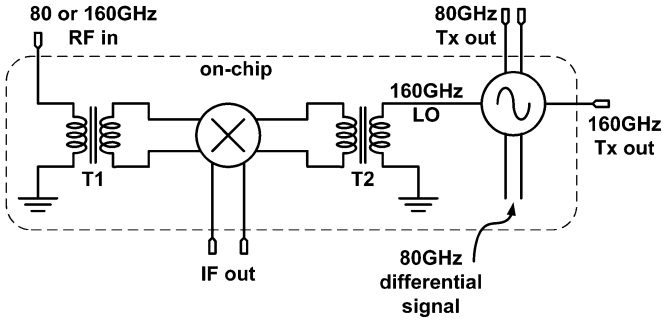

Fig. 2. Top-level 80/160-GHz transceiver schematic (transceiver 1).

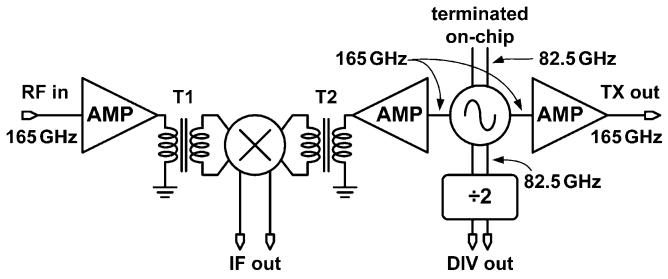

Fig. 3. Top-level schematic of the 165-GHz transceiver with transmit, receive, and LO amplifiers and static frequency divider (transceiver 2).

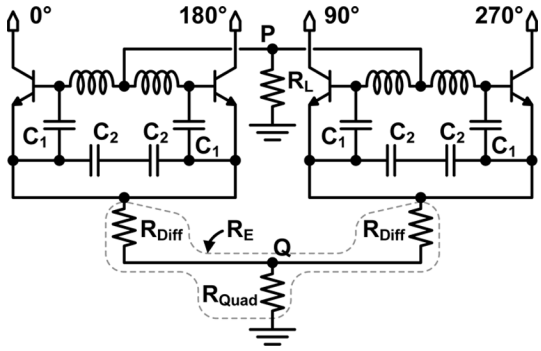

Fig. 4. A model of a quadrature oscillator, composed of two coupled differential Colpitts oscillators.

+11 dBm output power, that can be employed as the 80-GHz part of the system in Fig. 1. This paper focuses on the design of the 160-GHz part of the system and describes two transceivers. The first is a proof-of-concept single-chip transceiver with reduced integration level, whose schematic is illustrated in Fig. 2, and which will be henceforth referred to as transceiver 1 [6]. The second single-chip transceiver, referred to as transceiver 2, builds on the first, and also includes three 165-GHz amplifiers and an 80-GHz static frequency divider, as illustrated in Fig. 3. It marks the highest level of integration in silicon above 100 GHz. In this transceiver, the single-ended input is amplified by the receive-amplifier and is converted to a differential signal by transformer T1 before reaching the mixer. A differential 165-GHz LO signal is generated using the 82.5-GHz quadrature oscillator. This 165-GHz differential LO is treated as two single-ended signals, each of which is amplified separately. Transformer T2 connects the amplified LO signal to the mixer, while the second amplified LO signal is used as the 165-GHz transmitter output. The quadrature oscillator also produces two differential 82.5-GHz signals. One of the 82.5-GHz differential outputs drives the static frequency divider [10], while the other is terminated with 50-Ω resistors on-chip. However, in a future version of this chip, the latter can also be used to integrate an 80-GHz transceiver on the same die. The mixer, oscillator and transformers are identical in both transceivers.

III. Circuit Building Blocks

A. 80-GHz Quadrature Oscillator

In this work, we have employed a quadrature oscillator to demonstrate that such a topology simplifies the LO distribution among transceiver arrays. However, it should be noted that in the transceiver topologies discussed here, the quadrature phase relationship between the two 80-GHz differential outputs of the oscillator is not critical for correct operation. In the past, quadruple-push oscillators were designed for the purpose of efficiently generating a fourth-harmonic signal [11] using delay lines. By far the most common quadrature oscillator topology consists of two inter-locked cross-coupled *LC* oscillators [12]. However, experimental data have shown that differential Colpitts oscillators exhibit superior performance in terms of phase noise, tuning range, temperature stability, and operation at mm-wave frequencies [13]–[15]. To date, quadrature Colpitts oscillators have been implemented by injection locking two differential oscillators [16], [17], as opposed to a quadruple-push oscillator, and at lower frequency than the oscillator presented here.

Taking advantage of the Colpitts topology, and expanding on a 3-push oscillator concept [18], we are proposing the quadrature oscillator topology illustrated in Fig. 4. It consists of two coupled differential Colpitts oscillators. In each differential oscillator, a common-mode resistor $R_{\rm Diff}$ ensures that its two outputs are 180° out of phase [19]. By a similar approach, resistor $R_{\rm Quad}$, common to both differential oscillators, i.e., shared by all four Colpitts sub-oscillators, will help to establish 90° phase difference between the two differential halves of the quadrature oscillator. The common-mode resistors, along with the star-connection of the tank inductors at node P, ensure that the four oscillator outputs can be locked in quadrature, as will be shown next. The proposed oscillator can be analyzed using modal analysis by extending the theory previously developed for push-push and triple-push oscillators [18], [20], and power amplifiers [21], to a quadruple-push oscillator. Note that, in this paper the terms

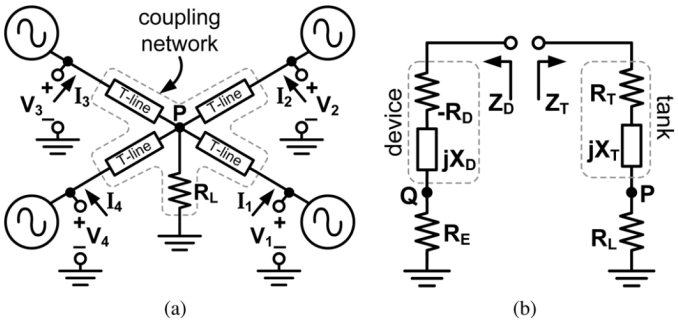

Fig. 5. (a) Block diagram and port definitions for a quadruple-push oscillator. (b) Equivalent circuit for one of the sub-oscillators.

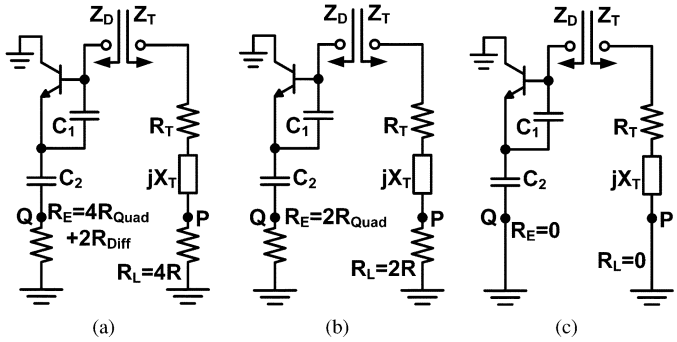

Fig. 6. Equivalent circuit models for each oscillator mode. (a) Even mode. (b) Odd mode. (c) Quadrature mode.

TABLE I
EIGENVECTORS AND EIGENVALUES FOR EACH OSCILLATION MODE

Mode	Eigenvector	Eigenvalue
Even	$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix}$	$Z_e = Z_{11} + 2Z_{12} + Z_{13}$
Odd	$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} 1 \\ -1 \\ 1 \\ -1 \end{bmatrix}$	$Z_o = Z_{11} - 2Z_{12} + Z_{13}$
Quadrature	$I_1 + I_2 + I_3 + I_4 = 0$	$Z_q = Z_{11} - Z_{13}$ (double root)

"even mode" and "common mode" are used interchangeably to mean the same thing. Similarly, "odd mode" and "differential mode" refer to the same circuit condition.

To start the analysis, the oscillator is represented as the four-port circuit of Fig. 5(a). Each of the four Colpitts circuits, including their common-mode resistors, is modeled as a separate sub-oscillator. All four sub-oscillators are coupled with a network that consists of transmission lines and a load resistor R_L. The voltage, current, and impedance phasors of the 4-push oscillator topology are related by the following matrix equation: $[\mathbf{Z}][\mathrm{I}] = [\mathbf{V}]$. Taking into account the symmetries that exist in the circuit, i.e., $Z_{ij} = Z_{ji}$ for $i, j = 1 \ldots 4$ and $Z_{12} = Z_{14} = Z_{23} = Z_{34}$, $Z_{13} = Z_{24}$, the matrix equation can be recast as

$$\begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{12} \\ Z_{12} & Z_{11} & Z_{12} & Z_{13} \\ Z_{13} & Z_{12} & Z_{11} & Z_{12} \\ Z_{12} & Z_{13} & Z_{12} & Z_{11} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \tag{1}$$

The eigenvectors and eigenvalues of (1) represent all the oscillation modes of the circuit. The eigenvalues and eigenvectors obtained by solving (1) are given in Table I. In each oscillation mode (i.e., even, odd, or quadrature), the phases and relative amplitudes of the signals produced by the sub-oscillators are represented by the elements of the eigenvector that describes that mode. For example, the values of $I_1 = 1$ and $I_2 = -1$ in the odd mode, illustrate that sub-oscillators 1 and 2 produce signals of equal amplitude which are 180° out of phase. The impedance seen at the ports of the oscillator in a particular mode is given by the eigenvalue corresponding to that mode.

The quadrature oscillation mode is described by two eigenvectors which satisfy the equation $I_1 + I_2 + I_3 + I_4 = 0$ and, at the same time, comply with the symmetry of the circuit. The symmetry requires having equal-amplitude oscillations in all four sub-circuits. The two eigenvectors are

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} 1 \\ e^{j\frac{\pi}{2}} \\ e^{j\pi} \\ e^{j\frac{3\pi}{2}} \end{bmatrix}, \quad \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} 1 \\ e^{-j\frac{\pi}{2}} \\ e^{-j\pi} \\ e^{-j\frac{3\pi}{2}} \end{bmatrix} \tag{2}$$

To establish correct circuit operation, the even- and odd-mode oscillations must be suppressed and the quadrature oscillation mode must be amplified. The conditions for quadrature oscillation can be derived by inspecting any of the quarter-circuits separately. In Fig. 5(b) the quarter-oscillator is modeled as a single-port. Looking to the left, the impedance Z_D of the negative resistance device appears in series with R_E, which represents the combination of R_{Diff} and R_{Quad}, shown earlier in Fig. 4. To the right, one sees Z_T, which represents the oscillator tank, in series with the load R_L.

The single-port sub-oscillator schematic of Fig. 5(b) is redrawn for each of the oscillation modes in Fig. 6, indicating the values of the various common-mode resistors seen in each case. Note that both nodes $\mathbf{Q}$ and $\mathbf{P}$ are common to all four sub-oscillators. In the quadrature oscillation mode, $R_E = R_L = 0$ because nodes $\mathbf{Q}$ and $\mathbf{P}$ appear as virtual grounds. In the odd mode of oscillation, $R_E = 2R_{\mathrm{Quad}}$ and $R_L = 2R$, because the resistors R_{Diff} cancel in differential mode. Since two waveforms add in phase across R_{Quad} and across R_L their values double in the odd mode of oscillation. Similarly, in the even oscillation mode, where all sub-oscillators are in phase, the common-mode resistors at nodes $\mathbf{Q}$ and $\mathbf{P}$ become $R_E = 4R_{\mathrm{Quad}} + 2R_{\mathrm{Diff}}$ and $R_L = 4R$, respectively.

By writing the conditions for suppressing even- and odd-mode, and enhancing the quadrature-mode oscillations, and after substituting the impedances from Fig. 6, the following equations are obtained:

Even mode:

$$\begin{aligned} &\Re\{Z_{eD} + Z_{eT}\} > 0 \\ &\Re\{-R_D + jX_D + 4R_{\mathrm{Quad}} \\ &\quad + 2R_{\mathrm{Diff}} + R_T + jX_T + 4R\} > 0 \\ &\quad - R_D + 4R_{\mathrm{Quad}} + 2R_{\mathrm{Diff}} + R_T + 4R > 0; \end{aligned} \tag{3}$$

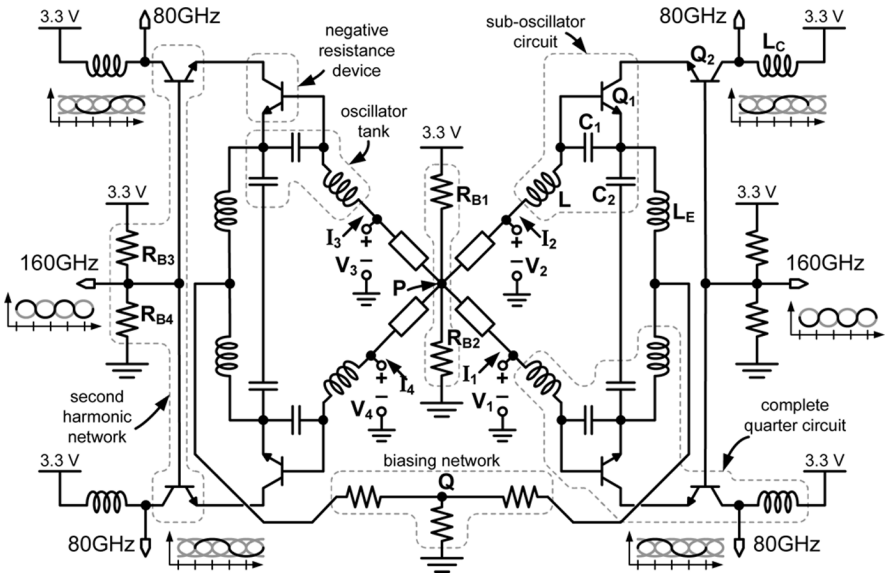

Fig. 7. Quadrature oscillator schematic.

Odd mode:

$$\begin{aligned}&\Re\{Z_{oD}+Z_{oT}\}>0\\&\Re\{-R_D+jX_D+2R_{\rm Quad}\\&\quad+R_T+jX_T+2R\}>0\\&\quad-R_D+2R_{\rm Quad}+R_T+2R>0;\end{aligned}\tag{4}$$

Quadrature mode:

$$\begin{aligned}&\Re\{Z_{qD}+Z_{qT}\}<0\\&\Re\{-R_D+jX_D+R_T+jX_T\}<0\\&-R_D+R_T<0;\end{aligned}\tag{5}$$

$$\begin{aligned}&\Im\{Z_{qD}+Z_{qT}\}=0\\&\Im\{-R_D+jX_D+R_T+jX_T\}=0\\&jX_D+jX_T=0.\end{aligned}\tag{6}$$

Finally, (7) describes the quadrature oscillation condition and is obtained from inequalities (3), (4), and (5) and from (6), where $-R_D$ is the negative resistance of the active device.

$$\begin{aligned}R_T\ &<|-R_D|<R_T+2R+2R_{\rm Quad}\\jX_D\ &+jX_T=0\end{aligned}\tag{7}$$

It should be noted that, although the roles of $R_{\rm Diff}$ and $R_{\rm Quad}$ are not immediately apparent from the model of Fig. 5(a), they are critical in determining the phases of the oscillator outputs in a circuit implementation. Since the order of the entries of the quadrature-mode eigenvectors of (2) can be interchanged without affecting the solution, $R_{\rm Diff}$ and $R_{\rm Quad}$ are responsible for establishing the exact phase relationships of the four outputs (i.e., which output is 0°, which is 90°, etc.). Furthermore, $R_{\rm Diff}$ and $R_{\rm Quad}$ help with suppressing the odd and even oscillation modes by significantly degrading the Q of the capacitor C_2 in Fig. 6(a) and (b).

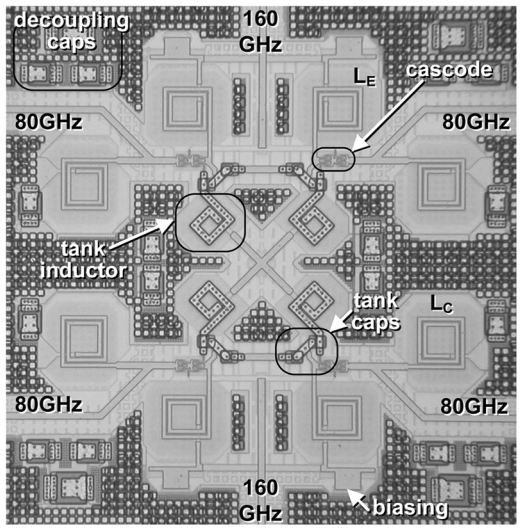

Fig. 8. Layout detail of the quadrature oscillator.

Based on the concepts described above, the oscillator shown in Fig. 7 was designed for quadrature operation at a fundamental frequency of 80 GHz. Since AMOS varactors were not available in this technology, the oscillator was designed to operate at a constant frequency. However, more recent work in CMOS [15] illustrates that it is straightforward to extend this oscillator to a voltage-tunable version. In this design, the load resistor R_L (of Fig. 5(a), where the fourth-harmonic signal is produced, is implemented with the bias resistors R_{B1} and R_{B2}. Cascode transistors are employed to adequately isolate the quadrature outputs from the tank. They also allow combining the two differential 80-GHz signals into two second-harmonic signals at 160 GHz that are 180° out of phase.

All transistors in the oscillator are biased at the peak-f_T current density of 14 mA/μm^2 to obtain the maximum output swing. Particular attention was paid to the symmetry of the oscillator layout, both for differential and for quadrature signals, as is illustrated in Fig. 8. The oscillator operates from 3.3 V, and

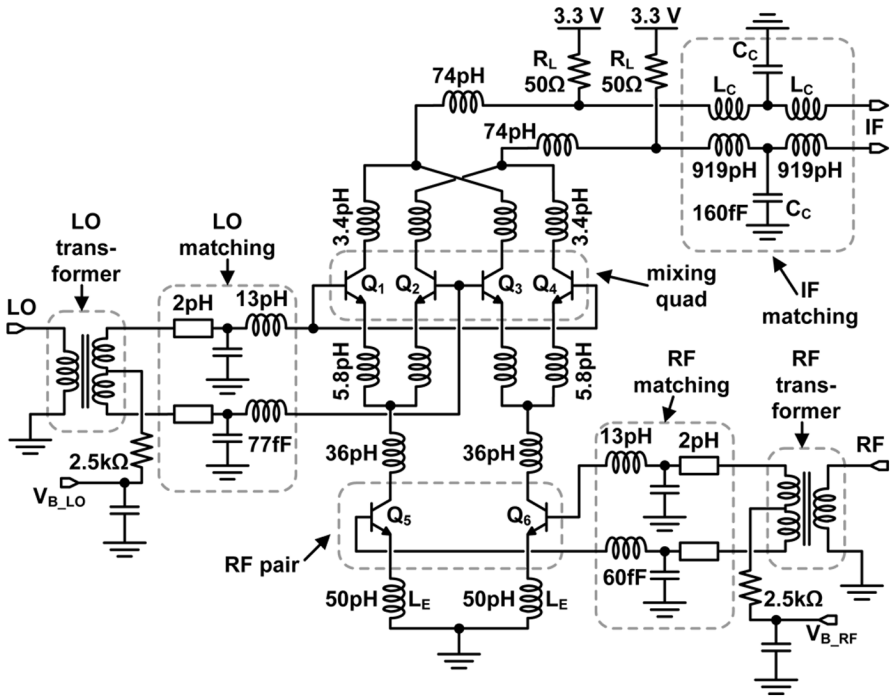

Fig. 9. Down-converter mixer schematic.

consumes a total of 70 mA. To the best of our knowledge, this is the first quadrature oscillator at 80 GHz and the first differential oscillator at 160 GHz designed in a SiGe HBT technology.

B. 160-GHz Gilbert-Cell Down-Convert Mixer

A double-balanced Gilbert cell topology [22] mixer with on-chip RF and LO baluns is employed in the receiver. Its schematic is shown in Fig. 9. The baluns, described in detail in the next section, perform single-ended to differential conversion. The bias for the RF diff-pair and for the LO quad is applied to the center tap of the secondary coil of each transformer. Inductors L_E are used instead of a current source to achieve larger voltage headroom, better linearity, and help to match the RF input to 50 Ω at 160 GHz. Series 36-pH inductors are inserted between the collectors of the RF pair transistors and the emitters of the mixing quad to suppress the second harmonic (320 GHz) of the RF and LO signals over a broad band. The reactance of the LO and RF inputs is tuned out by employing shunt capacitors and series inductive transmission lines, which are part of the interconnect. The mixer schematic includes several inductors that model every piece of interconnect line in the mixer. Lines over the silicon substrate are modeled using the inductor 2-π model, while interconnect that passes over metal is described as transmission lines. Furthermore, all metal-to-metal overlap capacitances are extracted using ASITIC and are included in the simulation schematic. They are not shown here for clarity.

There is no IF amplifier at the mixer output. Instead, the differential IF output is matched to 50 Ω at each side over a broad bandwidth (DC to 10 GHz) with the help of a network of inductors, capacitors (L_C and C_C) and on-chip 50-Ω resistors. A

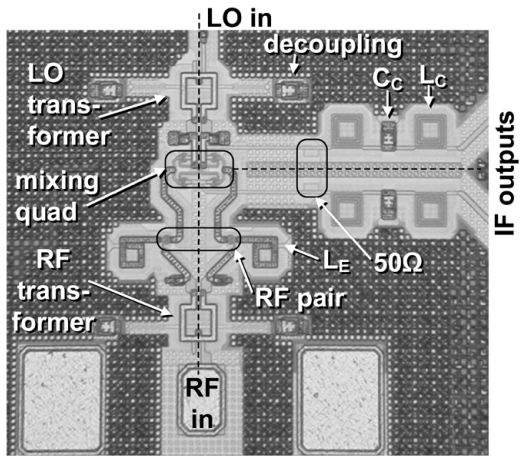

Fig. 10. Layout snapshot of the down-converter mixer.

broad IF bandwidth is required for communications at data rates above 10 Gb/s and for applications such as radio astronomy and imaging. In each IF matching network two identical inductors, L_C, are employed instead of a single large inductor, to increase the self-resonance frequency of those inductors beyond 50 GHz. Shunt capacitors C_C tune the impedance to 50 Ω.

The mixer layout (illustrated in Fig. 10) is fully symmetric with respect to the LO-to-RF line. Symmetry is essential for proper double-balanced mixing operation, for impedance matching, and for achieving high isolation at mm-wave frequencies. The mixer operates from 3.3 V and consumes 15 mA. All transistors have the same size ($l_E = 4\,\mu$m, $w_E = 0.13\,\mu$m) and are biased at the peak-f_T current density of 14 mA/μm^2. Thanks to its balanced multiplier structure, this mixer works up to a record 180 GHz.

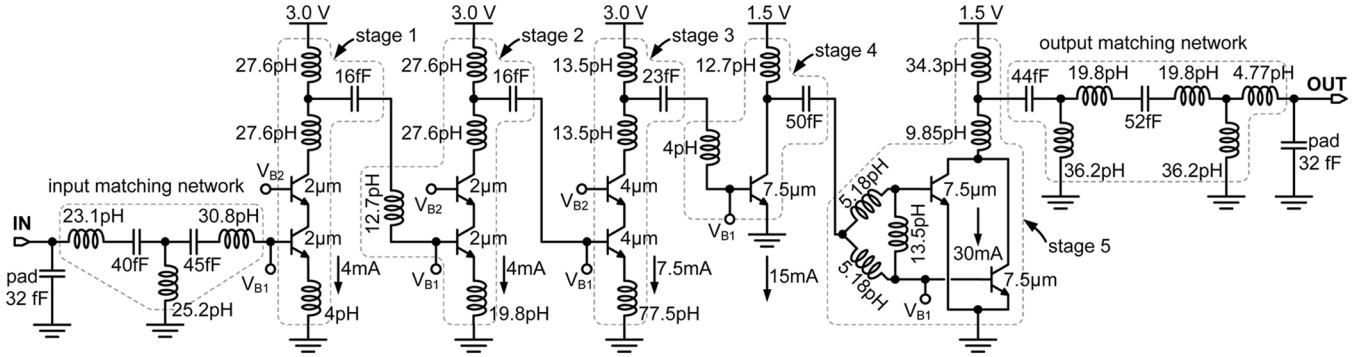

Fig. 11. Five-stage 140-GHz amplifier schematic.

C. 5-Stage D-Band Amplifiers

A tuned, 5-stage 160-GHz amplifier was designed at the same time as transceiver 1 [6]. Its schematic is illustrated in Fig. 11. However, since the transistor models were extracted from measurements below 110 GHz and on transistors with different vertical doping profiles, it was considered risky to integrate the amplifier in the transceiver. Indeed, although the 160-GHz oscillator frequency was within 1%–3% of simulation, the measured center frequency of the amplifier, which, unlike that of the oscillator, is sensitive to the transistor capacitances, was 13% lower, at 140 GHz, accentuating the difficulty of designing at this frequency. A second amplifier was next re-tuned to 180 GHz and its center frequency was measured to be 170 GHz. Three 170-GHz amplifiers were integrated in transceiver 2. Each of the three had different input and/or output matching networks, depending on its location in the transceiver. Both amplifiers were designed using the same methodology, described next.

The amplifier design begins at the last stage and steps backwards towards the input. The bias current and size of transistors in each stage are progressively scaled (increased) from the input to the output. Interstage matching is employed to maximize the power gain. The last two stages of the amplifier employ a common-emitter topology for higher output power, while the first 3 stages are implemented with cascodes to obtain larger gain. Each of the inductors shown in the amplifier schematic was simulated in ASITIC and described by its corresponding 2-π equivalent circuit in simulation.

The last stage consists of a CE transistor biased at 30 mA to obtain a $+2$ dBm (0.8 $V_{\rm PP}$) signal in a 50-Ω load. Due to the large current that has to flow through this device and its metallization, it was implemented as two transistors connected in parallel, each with an emitter length of 7.5 μm. The pieces of interconnect leading to the parallel-connected devices are shown in the schematic as 5.18-pH inductors. The load of the fifth stage is split in two to provide space in the layout for the load and for the output matching network. The last stage has an input impedance of $7\,\Omega - j2.2\,\Omega$, which is conjugately matched to the output of the fourth stage. It, too, uses a CE transistor with inductive load, whose emitter length and bias current are scaled down by a factor of 2 compared to the last stage, and presents an impedance of $13\,\Omega - j4.3\,\Omega$ to the third stage.

In each cascode stage, the output matching network consists of series and shunt inductors, and a series capacitor. The analysis and design of each of the amplifier stages can be carried out either in the traditional microwave way with the Smith Chart [1], or analytically, employing a lumped high-frequency equivalent circuit for the transistor, which includes the parasitic emitter and base resistances R_E and R_B. To improve the accuracy of this simplified equivalent circuit at mm-wave frequencies, we rely on the measured or simulated effective cutoff frequency $f_{T,\rm eff}$ and transconductance $g_{m,\rm eff}$, where $g_{,\rm eff} = g_m/(1 + g_m R_E)$. Note that in Fig. 12(a) and (b), the input capacitance of the transistor or of the cascode stage is described by $g_{m,\rm eff}/\omega_{T,\rm eff}$, and includes the Miller effect. The reverse isolation is not captured by this circuit. However, it remains very low because $C_{bc}/C_\pi < 10$.

$$Z_{\rm in} = R_B + R_E + \frac{\omega_{T,\rm eff}}{j\omega g_{m,\rm eff}} \tag{8}$$

$$A_I = \frac{i_{sc}}{i_{\rm in}} = -\frac{f_T}{jf} \tag{9}$$

When inductive degeneration is used, as in the amplifier stage under consideration, the input impedance can be derived by looking at the equivalent circuit in Fig. 12(b) and is given by

$$Z_{\rm in} = R_B + R_E + \omega_{T,\rm eff} L_E + \frac{\omega_{T,\rm eff}}{j\omega g_{\rm m,\ eff}} + j\omega L_E. \tag{10}$$

For conjugate matching at the input, first, L_E is chosen such that the real part of $Z_{\rm in}$ is equal to Z_0. Then, a base inductor L_B is added to cancel the imaginary part of $Z_{\rm in}$. From (10), its value must be $L_B = (\omega_{T,\rm eff}/\omega^2 g_{m,\rm eff}) - L_E$.

To find the gain of the stage, its model is redrawn in Fig. 12(c) assuming that it is conjugately matched, so that $Z_{\rm in} = Z_0$. The losses at the output of the amplifier stage, including the transistor and the output matching network, are represented by a parallel resistor R_P at resonance. The available power gain in a matched load (to R_P), is given by

$$\begin{aligned} G = A_V A_I^* &= \left(\frac{-\frac{f_T}{jf} i_{\rm in} R_P}{(Z_0 + Z_{\rm in}) i_{\rm in}}\right)^* \left(\frac{i_{sc}}{2 i_{\rm in}}\right) \\ &= \left(-\frac{1}{4}\frac{f_T}{jf}\frac{R_P}{Z_0}\right)\left(-\frac{f_T}{jf}\right)^* \\ &= \frac{1}{4}\frac{R_P}{Z_0}\left(\frac{f_T}{f}\right)^2. \end{aligned} \tag{11}$$

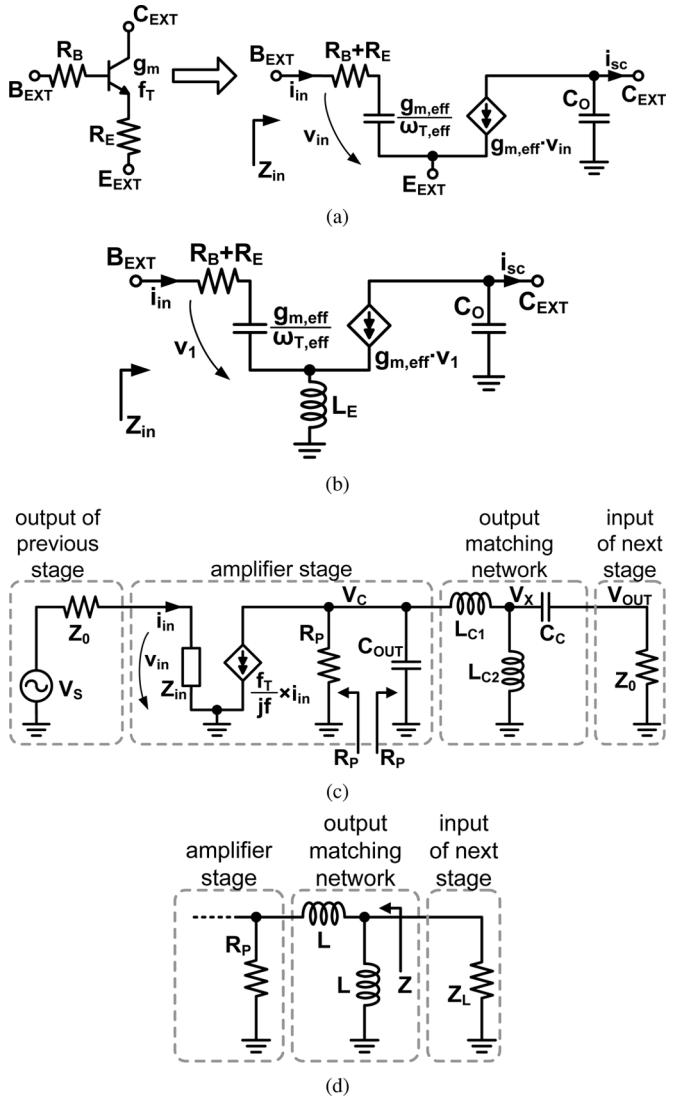

Fig. 12. (a) Transistor small-signal model. (b) Transistor small-signal model with inductive degeneration. (c) Small-signal model of an amplifier stage. (d) Impedance transformation using split inductor load.

To evaluate the accuracy of the hand-design (8)–(11) and of the simplified equivalent circuit of the transistor, an HBT test structure with 5.74 μm emitter length was measured on the same wafer with the amplifier. Its extracted small signal model parameters were scaled for transistors with emitter lengths of 4 μm and 7.5 μm and listed in Table II. The accuracy of the input capacitance prediction for a CE stage using the simplified equivalent circuit was estimated by comparing the measured $C_\pi + C_{bc}$ with $g_{m,\mathrm{eff}}/\omega_{T,\mathrm{eff}}$ for the 7.5-μm device. Less than 10% error was found. By substituting the values of Table II into (10), the input impedance of stage 3 of the amplifier can be calculated as $Z_{\mathrm{in}} = 135 + j56.8\,\Omega$ at 140 GHz. The 16-fF series capacitor in front of stage 3 cancels the imaginary part of this impedance, thus presenting a load of $Z_L = 135\,\Omega$ to stage 2. Similarly the input impedance of stage 2 can be calculated as $70.2 + j3.8\,\Omega$, leading to $Z_0 = 70.2\,\Omega$ for stage 2. The two 27.6-pH inductive loads of stage 2, along with C_{out} that consists of transistor and inductor parasitics, transform Z_L to $264 + j274\Omega$. These values, together with $f_{T,\mathrm{eff}} = 236$ GHz can now be substituted into (11) to obtain the gain for stage 2 as 4.3 dB. This value is close to the simulated gain of 3 dB to 4 dB per stage, leading to a total gain of 20 dB for the five amplifier stages

$$Z = \frac{R_P\omega^2L^2}{R_P^2 + 4\omega^2L^2} + \frac{j\omega L\left(R_P^2 - 2\omega^2L^2\right)}{R_P^2 + 4\omega^2L^2}. \qquad (12)$$

The impedance transformation that occurs in the split load of an amplifier stage can be explained by (12), which gives the impedance looking from the input of a following stage towards the R_P of a preceding stage, as shown in Fig. 12(d). From (12) it is apparent that to cancel the imaginary part of Z, R_P^2 must be equal to $2\omega^2L^2$. In this case the real part of Z becomes $\Re(Z) = R_P/6$. Thus, by employing split inductor loads, R_P, which is seen at the collector, can be transformed to a much lower impedance that exists at the input of the next amplifier stage.

All transistors are biased at the peak-f_T current density of 14 mA/μm^2. This choice of biasing and transistor sizing helps to maximize the power transfer between stages because the Z_{IN} of each stage (10) is approximately equal to the Z^*_{OUT} of the previous stage. The imaginary part (which is approximately equal to 1/3 of the real part) is canceled using interstage series capacitors and/or inductors. In a similar manner, the first stage is matched to 50 Ω by $R_B + R_E \approx 41\Omega$ and impedance transformation in the the input matching network.

All bias voltages, supply and ground are distributed on metal mesh planes with ample substrate contacts everywhere on chip. The metal mesh adds capacitance between the bias planes and ground [23]. For additional de-coupling, MiM capacitors of 0.5 pF (that are divided into 250-fF capacitors in parallel to avoid resonance) are positioned near each DC node of the circuit. The amplifier is AC-coupled for simpler testing.

TABLE II
MEASURED SMALL SIGNAL MODEL PARAMETERS OF AMPLIFIER TRANSISTORS

	$l_E = 4\mu m$	$l_E = 7.5\mu m$
$g_{m,eff}$	148 mS	278 mS
$f_{T,eff}$	236 GHz	237 GHz
$f_{T,eff}$ (Cascode)	218 GHz	218 GHz
τ_F	0.52 ps	0.52 ps
R_B	17.9Ω	9.57Ω
R_E	2.51Ω	1.34Ω
R_C	28.7Ω	15.3Ω
C_{cs}	5.92 fF	11.1 fF
C_{be}	17.0 fF	31.8 fF
C_{bc}	8.36 fF	15.7 fF
$C_{diff} = \tau_F \times g_{m,eff}$	74.3 fF	139 fF
$C_\pi = C_{be} + C_{diff}$	91.3 fF	171 fF

D. Passive Components

1) 1-to-1 160-GHz Transformer: Identical transformers were employed at the RF and LO ports of the mixer for single-ended to differential signal conversion. Passive transformers are preferred to other methods of single-ended to differential conversion, such as differential pairs, since they do not consume any DC power. Furthermore, due to their symmetry, transformers have better common mode rejection than differential pairs at mm-wave frequencies. In this transceiver,

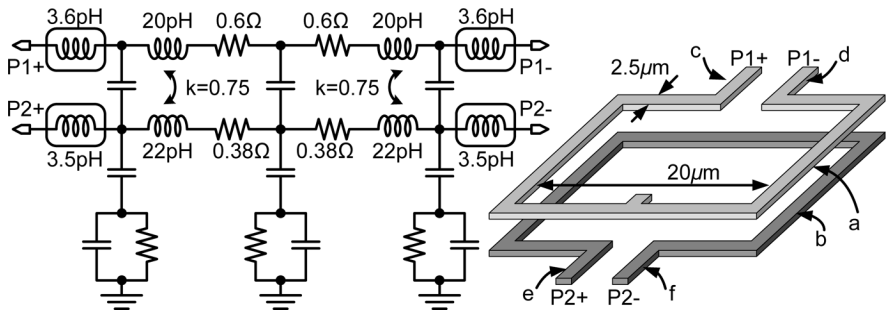

Fig. 13. Transformer 2-π model (left) and transformer geometry (right).

transformers are also used to AC-couple the RF and LO inputs to the mixer because they facilitate biasing of the mixer through the transformer center tap.

The transformer geometry and its model are shown in Fig. 13. The primary and the secondary coils consist of one square turn with an inner diameter of 20 μm and with 2.5 μm metal width. The transformer coils are placed directly above the silicon substrate, with the top coil implemented in the top aluminum (Alucap) layer, and the lower coil in Metal 6, which is made of copper. The top coil has a center tap for biasing circuits connected to the transformer. The ASITIC [24] program (version 3.19.00) was employed to simulate the transformer geometry and to optimize it for lowest loss around 160 GHz. A list of ASITIC commands used to define the transformer structure is given in the Appendix. Because of the small transformer footprint, the simulated silicon area below and around the transformer was reduced to 64 μm $\times$ 64 μm to produce a sufficiently fine grid in the metal windings, as required to ensure good accuracy.

A lumped equivalent circuit, consisting of frequency-independent circuit elements, was extracted for the transformer (Fig. 13) and was employed in all circuit simulations. It comprises a 2-π model for the coils and 2-π models for each of the short wires connected to the transformer coils. The 2-π models were obtained by following the procedure outlined in [25]. The simulated self-resonance frequency of the transformer is approximately 400 GHz. Fig. 14 compares the transformer S-parameters simulated with ASITIC, those obtained with the 2-π model in SpectreRF, and the measured S_{21} and MAG (essentially the transformer loss) in the 1–70-GHz, 57–94-GHz, and 116–184-GHz frequency ranges. Good agreement of both S_{21} and MAG is achieved, within the measurement accuracy. Although S_{21} shows a loss of approximately 4 dB, MAG represents the transformer loss as it is used in the circuit, when all ports are matched. Thus, the true transformer loss is below 2 dB. For measurements below 94 GHz, LRM calibration and T-line de-embedding were employed, as described in [26]. The scatter in the measured S_{11} and S_{22} data is due to the difficulty of accurately measuring and de-embedding parasitic capacitances (below 1 fF), resistances (below 0.1 Ω) and inductances (below 1 pH). For example, errors or uncertainty in the probe-pad contact resistance of 0.1 Ω, parasitic inductance of 1 pH, and error in pad capacitance of 2 fF, can change the measured S_{21}, S_{11}, and S_{22} by as much as 1 dB in either direction for the small inductors and transformers discussed

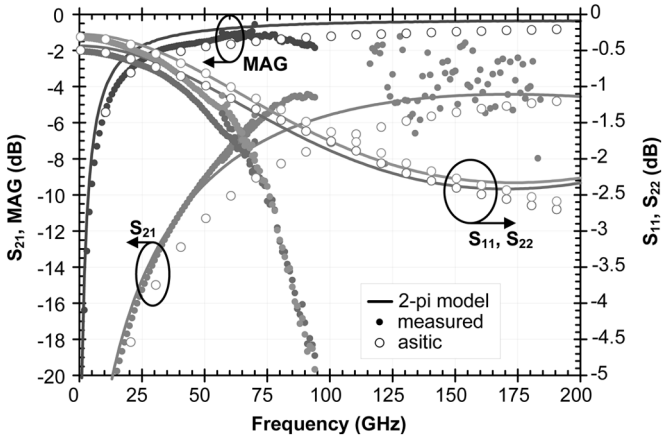

Fig. 14. Comparison of transformer $S_{11}S_{21}S_{22}$ and MAG simulated using ASITIC (open circles), modeled with 2-π model in SpectreRF (lines), and measured in three frequency ranges (dots) using two VNAs and power insertion loss measurements beyond 110 GHz.

in this paper. Above 100 GHz, the transmission loss (S_{21}) of the transformer was measured using a scalar transmission measurement as described in Section V.

2) 50-pH Oscillator Tank Inductor: To minimize the phase noise of the Colpitts oscillator, the quality factor Q of the tank must be maximized. For this purpose, the loss of the tank inductor was reduced by implementing the inductor coil with two metals shunted together (Alucap and Metal 6), and with a Metal 5 underpass (Fig. 15). An inductor geometry with 2.8-μm metal width, 2-μm spacing, and an inner diameter of 9 μm was chosen to push the self-resonance frequency above 400 GHz. The inductor coil was placed directly over the silicon substrate, without any polysilicon or metal shield. Microstrip transmission lines (3.6-μm-wide Metal 6 signal line over Metal 1 and Metal 2 ground plane) were employed to symmetrically connect the four tank inductors of the oscillator together.

Just as in the transformer case, a 2-π model was extracted from the ASITIC simulated Y-parameters, as shown in Fig. 15. Fig. 16 compares the measured L, R and effective Q of the inductor to those simulated using ASITIC and modeled with the 2-π model. The measurement was performed using two network analyzers covering the 1–70-GHz and the 57–94-GHz frequency ranges. Effective Q is defined as $Q_{\text{eff}} = (\Im(-Y_{11})/\Re(Y_{11}))$. The measured inductance value increases below 10 GHz due to imperfect probes and contact resistance. Except for the scatter in the measured Q data in the

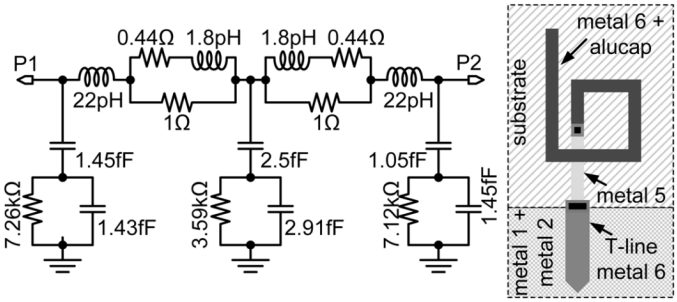

Fig. 15. Inductor 2-π model (left) and inductor geometry (right).

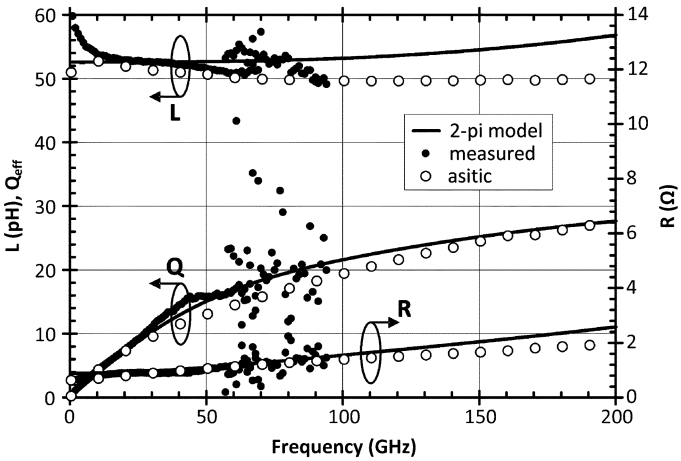

Fig. 16. Comparison of inductor L, R, and Q simulated using ASITIC, modeled with 2-π model, and measured over two frequency ranges using two different VNAs.

57–94-GHz range due to the difficulty of measuring resistance with less than 0.1-Ω accuracy, the agreement between simulations and measurements is very good.

IV. Fabrication

Transceiver 1 (Fig. 2) and the 140-GHz amplifier were fabricated in a SiGe HBT technology with nominal $f_{\rm MAX}$ of 300 GHz and f_T of 230 GHz [27]. Transceiver 2 (Fig. 3) and the 170-GHz amplifier were fabricated in a different run of the SiGe HBT technology, with the same backend, but where the $f_{\rm MAX}$ was 340 GHz and f_T was 270 GHz. The measured $f_{\rm MAX}$ and f_T curves for a nominal device in each run are shown in Fig. 17. Since the technology is still under development, the 140-GHz amplifier was also fabricated in several different process splits where the HBT profile was intentionally varied, to determine which structure results in the best circuit performance at frequencies above 100 GHz. The wafer splits cover SiGe HBTs with $f_T/f_{\rm MAX}$ values which vary in a correlated manner between 230/240 GHz and 280/290 GHz, respectively. The collector doping, the emitter width, or the emitter-base junction parameters were intentionally modified from wafer to wafer in order to produce the f_T and $f_{\rm MAX}$ variations. The rest of the SiGe BiCMOS process steps are identical for all wafer splits.

The process features a digital CMOS backend with 6 copper layers and a regular thickness, top aluminum metal layer. MiM capacitors and polysilicon resistors are also available.

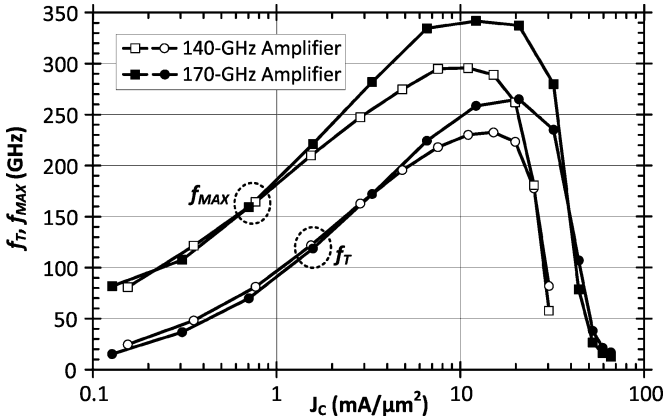

Fig. 17. Plot of measured f_T and $f_{\rm MAX}$ versus current density. The two sets of curves correspond to two different fab runs: the 140-GHz amplifier and transceiver 1 were fabricated in the first run. The 170-GHz amplifier and transceiver 2 were fabricated in the second run.

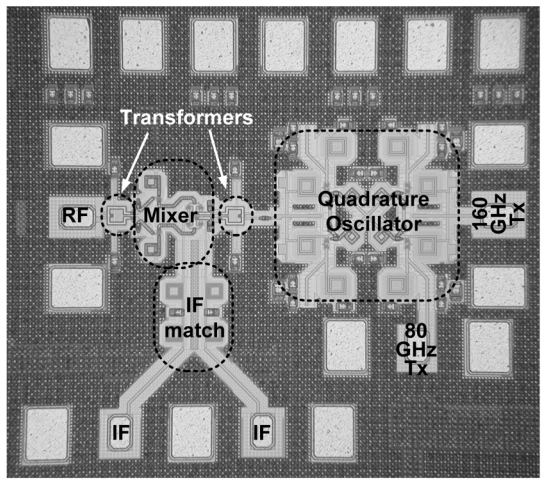

Fig. 18. Die photo of transceiver 1. The total area including pads is 650 μm $\times$ 700 μm.

Die photos of transceiver 1 and transceiver 2 are reproduced in Figs. 18 and 19, respectively. A die photo of the 140-GHz amplifier is illustrated in Fig. 20.

V. Measurement Results

Measurements were conducted on wafer using 110–170-GHz waveguide probes. A 110–170-GHz OLM $\times$12 multiplier signal source, an Agilent E4448A power spectrum analyzer (PSA) in conjunction with a Farran 110–170-GHz down-convert mixer, and an ELVA 110–170-GHz power sensor were employed for signal generation, spectral, and power measurements. The setup with power sensor is illustrated in Fig. 21. A 0–30-dB variable attenuator was used in the linearity measurements.

Since no network analyzer was available in the 110–170-GHz range, the amplifier gain and the transformer loss (S_{21} in Fig. 14) in this frequency band were obtained with transmission measurements by following a two-step procedure. In the first step a signal source was connected to the DUT (amplifier or transformer) input and either the spectrum analyzer or the power sensor was connected at the output. The output power

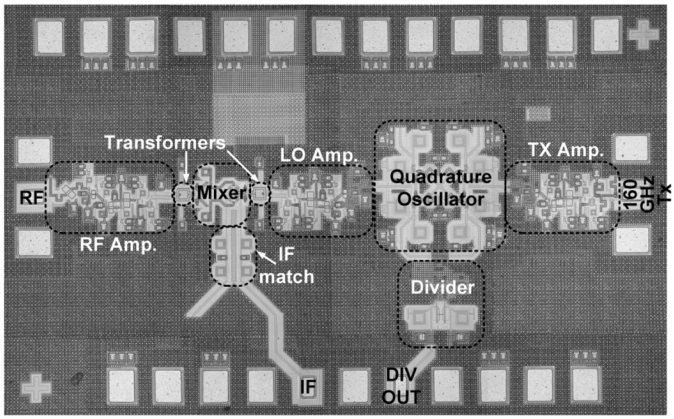

Fig. 19. Die photo of transceiver 2 with integrated amplifiers and static frequency divider. The total area including pads is 840 μm $\times$ 1365 μm.

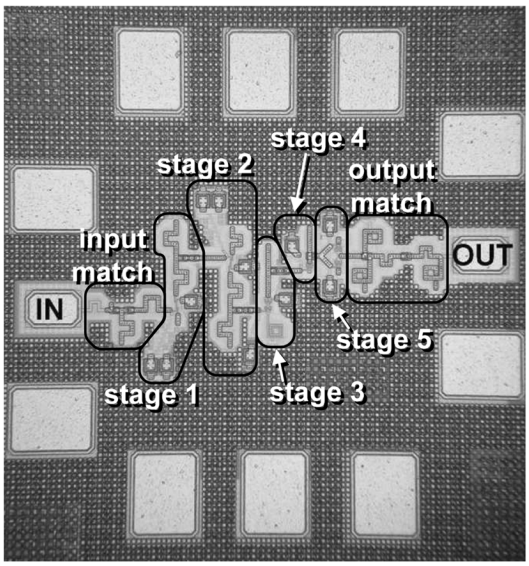

Fig. 20. Die photo of the 140-GHz. The active circuit area is 200 μm $\times$ 400 μm.

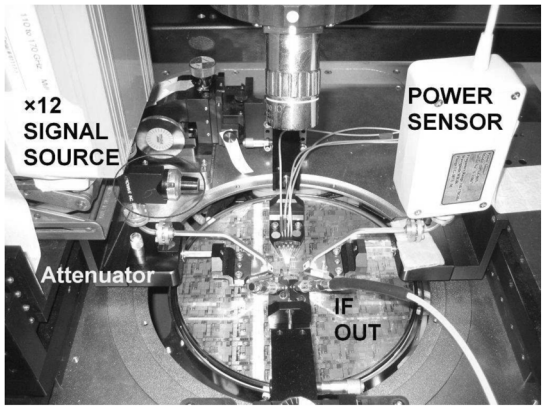

Fig. 21. On-wafer 160-GHz test setup for transmitter output power measurements showing the signal source on the left, applied at the receiver input through 110–170-GHz waveguide probes. The 110–170-GHz power sensor is at the right. The IF output is collected at the bottom with differential probes.

was recorded at each frequency. In the second step, the output power was recorded again, after replacing the DUT by a "thru" located on a standard 110-GHz Cascade Microtech calibration

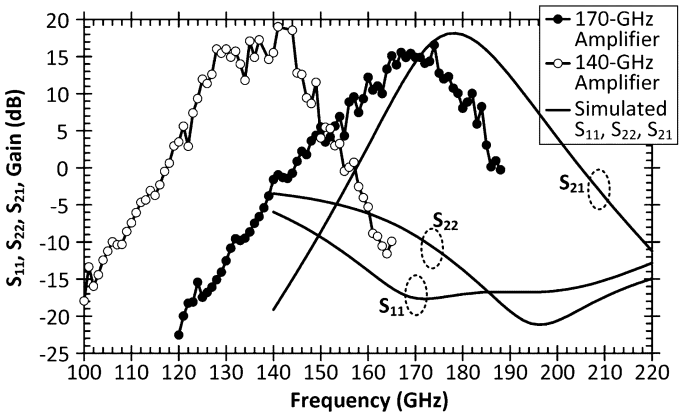

Fig. 22. Measured gain (symbols) at 25 °C of the 140-GHz amplifier and the 170-GHz amplifier. Simulated S-parameters (lines) of the 170-GHz amplifier.

substrate and keeping the rest of the setup unchanged. The power measured with the "thru" was subtracted from the power measured with the DUT in place to obtain the gain. Thus, all power gain measurements include the on-wafer pads, which have not been de-embedded.

A. D-Band Amplifiers

The measured gains of the 140-GHz amplifier and the 170-GHz amplifier at 25 °C are reproduced in Fig. 22. For the 140-GHz amplifier, the gain remains above 15 dB from 126 to 144 GHz. The measured gain of the 170-GHz amplifier is 15 dB, with 3-dB bandwidth from 164 to 175 GHz. Fig. 22 also includes the simulated S-parameters of the 170-GHz amplifier. There is less than 7% reduction in the center frequency between measurements and simulation, which may be explained by the fact that the technology employed is still under development [27] and the models, which were extracted from S-parameter measurements below 110 GHz, do not reflect current device performance accurately. The S_{12} of the amplifiers could not be measured due to insufficient sensitivity in the measurement setup.

Fig. 23 reproduces the measured gain of the 140-GHz amplifier as a function of temperature. At 140 GHz, the gain decreases from 17 dB at 25 °C to 4 dB at 125 °C while in the 125–135-GHz range it remains above 10 dB for all temperatures. The gain variation is small at the lower end and increases at the upper end of the bandwidth, where the effect of temperature and process variation is more pronounced. This behavior is similar to that observed in tuned SiGe HBT and CMOS amplifiers operating at 80 and 60 GHz. The power gain at the higher frequencies depends on the transistor f_{MAX} and on the Q of the load inductor, and rapidly degrades with increasing temperature, whereas, at the lower end of the amplifier bandwidth, the gain is primarily controlled by the ratio of the collector load and emitter degeneration inductors.

To correlate the effect of the HBT f_T and f_{MAX} with the amplifier performance, several wafer splits were selected where only one HBT profile parameter, the collector doping, is varied. The f_T and f_{MAX} of devices in those splits, which have opposite trends, are plotted versus the relative collector doping in

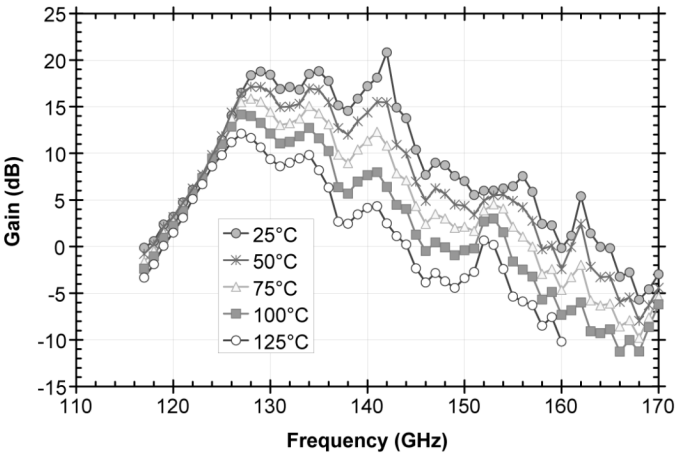

Fig. 23. 140-GHz amplifier gain over temperature measured using a D-band power sensor.

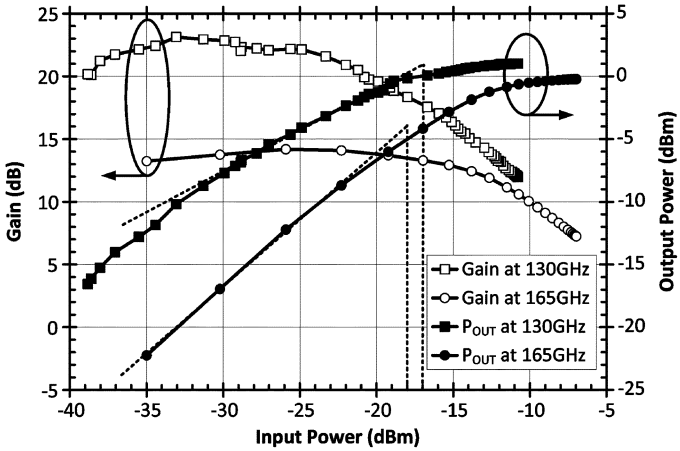

Fig. 25. Measured linearity of the 140-GHz amplifier at 130 GHz and measured linearity of the 170-GHz amplifier at 165 GHz.

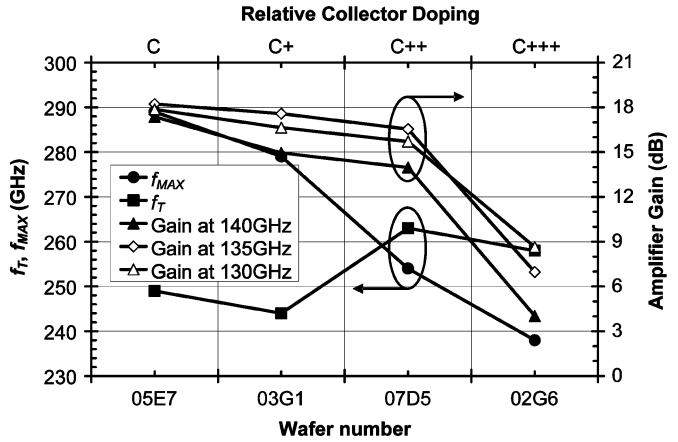

Fig. 24. Measured $f_T f_{\mathrm{MAX}}$, and amplifier gain at 130, 135, and 140 GHz plotted for four process splits where only the HBT collector doping is varied.

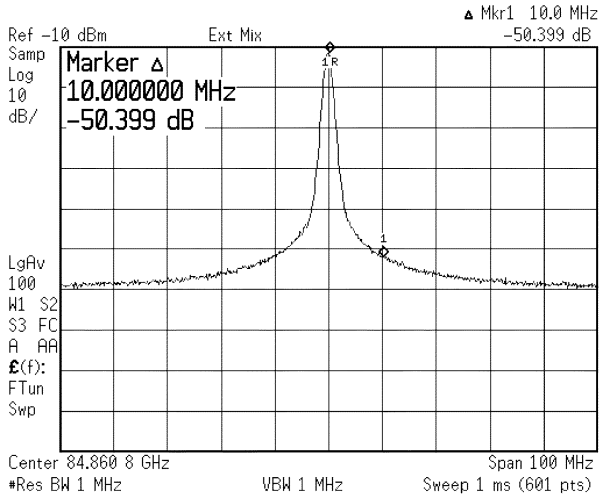

Fig. 26. Measured phase noise of transceiver 1 at the 80-GHz transmitter output.

Fig. 24, along with 140-GHz amplifier power gain at three frequencies, 130, 135, and 140 GHz. As can be observed, the amplifier gain and the f_{MAX} are both decreasing with increasing collector doping, thus the gain is correlated with the f_{MAX} of the SiGe HBT, but not with the f_T.

Linearity measurements were conducted using a $\times 12$ multiplier signal source, a 0–30 dB D-band attenuator, and a D-band power sensor. The power sensor allows measurements of absolute power that are necessary for obtaining the $\mathrm{P_{1dB}}$. The linearity measurements for both amplifiers are illustrated in Fig. 25. The measured input $\mathrm{P_{1dB}}$ is -17 dBm and the saturated output power is $+1$ dBm at 130 GHz for the 140-GHz amplifier. The 170-GHz amplifier achieves an input $\mathrm{P_{1dB}}$ of -18 dBm and saturated output power of 0 dBm at 165 GHz.

B. Transceivers

The close-in spectrum for phase-noise measurement of transceiver 1 at the 80-GHz transmitter output is shown in Fig. 26. The measured power difference is -50.4 dB at 10 MHz offset with respect to the carrier. Since this measurement was made with 1 MHz resolution bandwidth, the resulting phase noise is less than -110 dBc/Hz at 10 MHz offset. This phase noise is larger than what was demonstrated previously in this technology [23]. The degradation can be attributed to the quadrature operation of the oscillator, where the sub-circuits affect each other's phase, thus increasing the phase noise [20].

The signal power and frequency at the 160-GHz transmitter outputs of both transceivers are plotted in Fig. 27 as a function of the oscillator supply voltage. After de-embedding cable and probe losses, the single-ended transmitted power of transceiver 1 is -10 dBm at 160 GHz. Transceiver 2 achieves a maximum output power of -3.5 dBm at 165 GHz.

The measured differential down-conversion receiver gain in the 160-GHz band is shown in Fig. 28 for both transceivers at 25 °C. All receiver down-conversion measurements were done with a fixed LO signal by sweeping the RF. The measurements were performed with a spectrum analyzer and de-embedded by subtracting the cable and probe losses from the measured input RF power and output IF power. The circuit pads were not de-embedded. The conversion gain of transceiver 1 is -24 dB, with 13-GHz bandwidth. The gain is low due to insufficient LO power produced by the oscillator in transceiver 1. For transceiver 2 the gain in the 160-GHz band is improved to -3 dB,

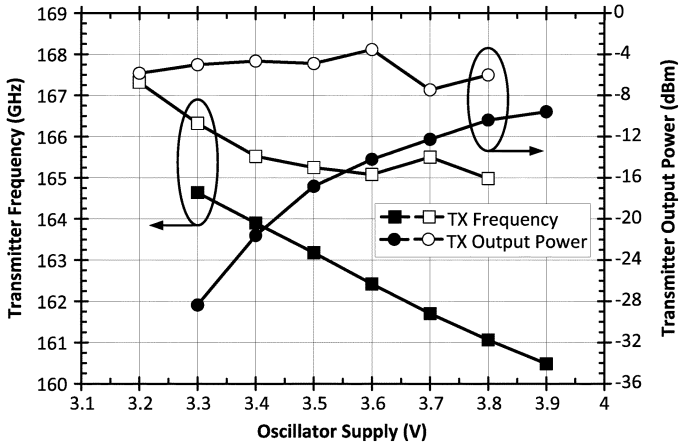

Fig. 27. Single-ended power and frequency at the 160-GHz transmitter outputs of transceiver 1 (filled symbols) and transceiver 2 (open symbols) versus the oscillator power supply voltage.

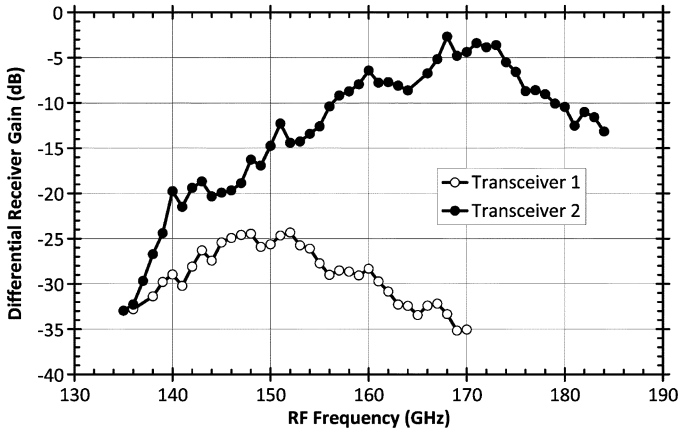

Fig. 28. Measured differential down-conversion gain of the receivers in transceiver 1 and transceiver 2 at 25 °C.

thanks to the integrated 170-GHz amplifiers. However more amplification of the LO might be needed to bring the LO power at the mixer to the optimal 0-dBm to +2-dBm level. Even though the mixer is the same in both transceivers, the 3-dB bandwidth of transceiver 2 is limited to 9 GHz by the RF amplifier. Note that IF amplifiers are not integrated on-chip, thus all the gain is achieved at the RF frequency of 160 GHz.

The receiver gain of transceiver 2 is summarized in Fig. 29 as a function of temperature. The gain is reduced to −11 dB at 75 °C, and to −25 dB at 125 °C, but the transceiver is still functional. Fig. 30 illustrates the receiver linearity of transceiver 2 from 25 °C to 125 °C. At 25 °C, the input $P_{1\ \mathrm{dB}}$ of the receiver is −20 dBm. The linearity, like the receiver gain, degrades significantly above 100 °C.

The measured total DC power consumption of the 165-GHz transceiver with amplifiers and divider is 0.9 W. Out of that, 340 mW are consumed by the oscillator, 100 mW by the static frequency divider and its output buffer, 32 mW are dissipated by the mixer, and each of the amplifiers requires 145 mW.

The performance of both transceivers, the 140-GHz amplifier, and the 170-GHz amplifier is summarized in Table III.

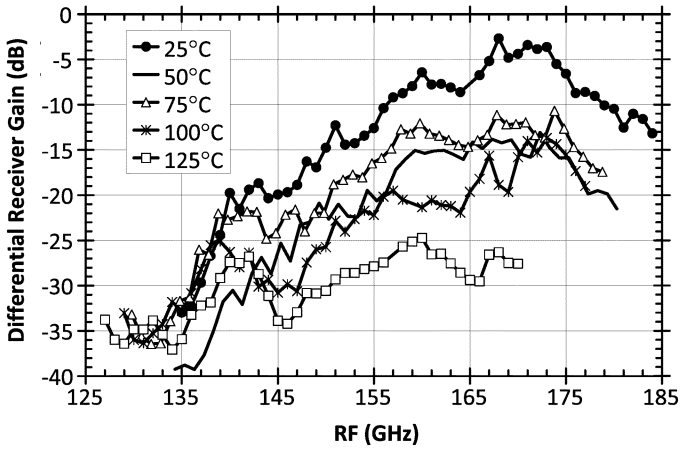

Fig. 29. Measured differential down-conversion receiver gain of transceiver 2 versus temperature.

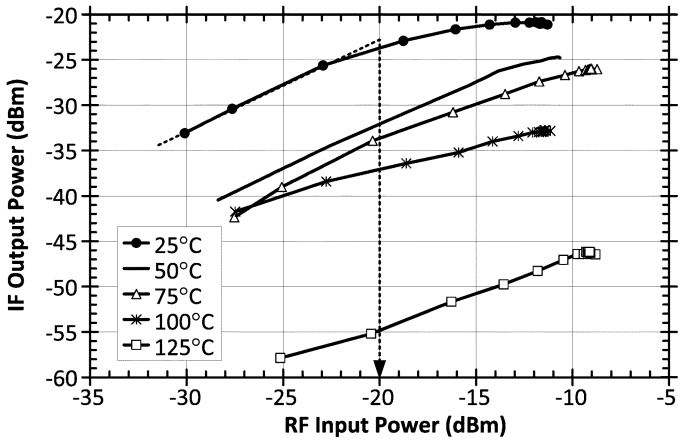

Fig. 30. Measured linearity at 168 GHz of transceiver 2.

TABLE III
SUMMARY OF SIMULATION AND MEASUREMENT RESULTS FOR THE TRANSCEIVERS AND AMPLIFIERS

Transceiver 1 (without amplifiers)	**Measured**	**Simulated**
Transceiver DC power	295 mW	280 mW
Tx power at 80 GHz (single-ended)	-0.5 dBm	+6 dBm
Tx power at 160 GHz (single-ended)	-10 dBm	-3.9 dBm
Down-conversion gain at 160 GHz (diff.)	-24 dB	-22 dB
Phase noise at 84 GHz, 10 MHz offset	-110 dBc/Hz	N/A
Transceiver 2 (with amplifiers and div.)	**Measured**	**Simulated**
Transceiver DC power	0.9 W	0.8 W
Tx power at 80 GHz (diff.)	+2.5 dBm	+9 dBm
Tx power at 160 GHz (single-ended)	-3.5 dBm	+9.4 dBm
Down-conversion gain at 160 GHz (diff.)	-3 dB	-7.8 dB
Phase noise at 84 GHz, 10 MHz offset	-110 dBc/Hz	N/A
140-GHz Amplifier	**Measured**	**Simulated**
Amplifier DC power	112 mW	112 mW
Amplifier gain (at 140/156 GHz)	17 dB	20 dB
170-GHz Amplifier	**Measured**	**Simulated**
Amplifier DC power	145 mW	135 mW
Amplifier gain (at 170/180 GHz)	15 dB	18 dB

VI. CONCLUSION

This paper is the first to report highly integrated radio transceivers in silicon at frequencies above 100 GHz. Most importantly, good performance is achieved up to 180 GHz, a factor of two larger than in any other silicon transceiver of

comparable complexity, using design methodologies, circuit topologies, lumped inductors and transformers commonly employed below 10 GHz. Two 160-GHz transceivers and two stand-alone D-band amplifiers were designed and fabricated. The first transceiver, which consists of an 80-GHz quadrature oscillator with differential 160-GHz outputs, 160-GHz Gilbert-cell mixer, and 70–180-GHz transformers, proved the feasibility of a push-push differential oscillator capable of driving a double-balanced mixer differentially at 160 GHz while simultaneously transmitting at 80 and 160 GHz. The second transceiver employs the same oscillator and mixer, but also includes 170-GHz amplifiers on the receive, transmit, and LO paths, and a static frequency divider. The D-band amplifiers increased the downconversion gain and transmitter output power of the second transceiver from -23.5 dB to -3 dB, and from -10 dBm to -3.5 dBm, respectively, when compared to the transceiver without amplifiers. Furthermore, its oscillator simultaneously drives two amplifiers at 165 GHz and a static frequency divider at 82.5 GHz, demonstrating an efficient solution to the LO distribution problem in 80+ GHz transceiver arrays. The Gilbert-cell mixer, the stand-alone amplifiers at 140 and 170 GHz with 17 and 15 dB gain, respectively, achieve record performance for silicon mixers and amplifiers. The circuits presented in this paper pave the way for future SoCs operating in the 100–200-GHz range.

APPENDIX

The following code snippet gives the sequence of ASITIC commands that define the transformer geometry.

```
chip 64 64
symsq name=a:len=25:w=2.5:s=2:n=1:metal=6:metal2=5:ilen=4:
    xorg=18:yorg=18
symsq name=b:len=25:w=2.5:s=2:n=1:metal=5:metal2=4:ilen=4:
    xorg=18:yorg=18:orient=180
wire name=c:len=8:w=2.5:metal=6:xorg=10:yorg=28:orient=180
wire name=d:len=8:w=2.5:metal=6:xorg=10:yorg=34.5
wire name=e:len=8:w=2.5:metal=5:xorg=43:yorg=28:orient=180
wire name=f:len=8:w=2.5:metal=5:xorg=43:yorg=34.5
```

ACKNOWLEDGMENT

The authors wish to acknowledge CMC and J. Pristupa for CAD support, K. Yau for transistor measurement, and ECTI, OIT, CFI, and NSERC for funding.

REFERENCES

[1] D. M. Pozar, *Microwave Engineering*, 3rd ed. New York: Wiley, 2005.

[2] T. Kosugi, M. Tokumitsu, K. Murata, T. Enoki, H. Takahashi, A. Hirata, and T. Nagatsuma, "120-GHz TX/RX waveguide modules for 10-Gbit/s wireless link system," in *2006 IEEE Compound Semicond. Integrated Circuit Symp.*, San Antonio, TX, Nov. 2006, pp. 25–28.

[3] K. K. O, C. Cao, E.-Y. Seok, and S. Sankaran, "CMOS millimeter-wave signal sources and detectors," in *IEEE Int. Symp. Circuits Syst.*, New Orleans, LA, May 2007, pp. 2614–2617.

[4] P. Roux, Y. Baeyens, O. Wohlgemuth, and Y. Chen, "A monolithic integrated 180 GHz SiGe HBT push-push oscillator," in *2005 13th Eur. Gallium Arsenide Other Compound Semicond. Application Symp.*, Paris, France, Oct. 2005, pp. 341–343.

[5] Y. Baeyens, N. Weimann, V. Houtsma, J. Weiner, Y. Yang, J. Frackoviak, A. Tate, and Y. K. Chen, "High-power submicron InP D-HBT push-push oscillators operating up to 215 GHz," in *IEEE Compound Semicond. Integr. Circuit Symp. Dig.*, Oct. 2005, pp. 208–211.

[6] E. Laskin, P. Chevalier, A. Chantre, B. Sautreuil, and S. Voinigescu, "80/160-GHz transceiver and 140-GHz amplifier in SiGe technology," in *2007 IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, Honolulu, HI, Jun. 2007, pp. 153–156.

[7] S. P. Voinigescu, S. T. Nicolson, M. Khanpour, K. Tang, K. H. K. Yau, N. Seyed-fathi, A. Timonov, A. Nachman, G. Eleftheriades, P. Schvan, and M. Yang, "CMOS SOCs at 100 GHz: System architectures, device characterization, and IC design examples," in *Proc. IEEE Int. Symp. Circuits Syst.*, New Orleans, LA, May 2007, pp. 1971–1974.

[8] S. T. Nicolson, E. Laskin, M. Khanpour, R. Aroca, A. Tomkins, K. H. K. Yau, P. Chevalier, P. Garcia, A. Chantre, B. Sautreuil, and S. P. Voinigescu, "Design and modeling considerations for fully-integrated silicon W-band transceivers," in *RFIT Workshop Dig.*, Singapore, 2007, pp. 141–149.

[9] S. T. Nicolson, P. Chevalier, A. Chantre, B. Sautreuil, and S. P. Voinigescu, "A 77–79 GHz doppler radar transceiver in silicon," in *IEEE Compound Semicond. Integrated Circuits Symp. Tech. Dig.*, Portland, OR, 2007, pp. 252–255.

[10] E. Laskin, S. T. Nicolson, P. Chevalier, A. Chantre, B. Sautreuil, and S. P. Voinigescu, "Low-power, low-phase noise SiGe HBT static frequency divider topologies up to 100 GHz," in *Proc. Bipolar/BiCMOS Circuits Technol. Meeting*, Maastricht, Holland, Oct. 2006, pp. 235–238.

[11] H. Xiao, T. Tanaka, and M. Aikawa, "A Ka-band quadruple-push oscillator," in *IEEE MTT-S Int. Microwave Symp. (IMS 2003)*, Philadelphia, PA, 2003, vol. 2, pp. 889–892.

[12] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001.

[13] K. W. Tang, S. Leung, N. Tieu, P. Schvan, and S. P. Voinigescu, "Frequency scaling and topology comparison of millimeter-wave CMOS vcos," in *2006 IEEE Compound Semicond. Integrated Circuit Symp.*, San Antonio, TX, Nov. 2006, pp. 55–58.

[14] C. Lee, T. Yao, A. Mangan, K. Yau, M. A. Copeland, and S. P. Voinigescu, "SiGe BiCMOS 65-GHz BPSK transmitter and 30 to 122 GHz LC-varactor VCOs with up to 21% tuning range," in *IEEE Compound Semicond. Integrated Circuits Symp. Tech. Dig.*, Monterey, CA, 2004, pp. 179–1118.

[15] E. Laskin, M. Khanpour, R. Aroca, K. W. Tang, P. Garcia, and S. P. Voinigescu, "95 GHz receiver with fundamental frequency VCO and static frequency divider in 65 nm digital CMOS," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, 2008.

[16] X. Li, S. Shekhar, and D. J. Allstot, "G_m-boosted common-gate LNA and differential Colpitts VCO/QVCO in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2609–2619, Dec. 2005.

[17] M. A. T. Sanduleanu and E. Stikvoort, "Highly linear, varactorless, 24 GHz IQ oscillator," in *Proc. RFIC Symp.*, 2005, pp. 577–580.

[18] Y.-L. Tang and H. Wang, "Triple-push oscillator approach: Theory and experiments," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1472–1479, Oct. 2001.

[19] L. Dauphinee, M. Copeland, and P. Schvan, "A balanced 1.5 GHz voltage controlled oscillator with an integrated IC resonator," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, 1997, pp. 390–391, 491.

[20] U. L. Rohde, A. K. Poddar, and G. Bock, *The Design of Modern Microwave Oscillators For Wireless Applications*. Hoboken, NJ: Wiley, 2005.

[21] R. G. Freitag, "A unified analysis of MMIC power amplifier stability," in *1992 IEEE Microwave Symp. Dig. MTT-S*, Albuquerque, NM, 1992, pp. 297–300.

[22] B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *IEEE J. Solid-State Circuits*, vol. SC-3, no. 4, pp. 365–373, Dec. 1968.

[23] S. T. Nicolson, K. Yau, P. Chevalier, A. Chantre, B. Sautreuil, K. Tang, and S. Voinigescu, "Design and scaling of W-band SiGe BiCMOS VCOs," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1821–1833, Sep. 2007.

[24] ASITIC. [Online]. Available: http://rfic.eecs.berkeley.edu/niknejad/asitic.html

[25] T. O. Dickson, M.-A. LaCroix, S. Boret, D. Gloria, R. Beerkens, and S. P. Voinigescu, "30–100-GHz inductors and transformers for millimeter-wave (Bi)CMOS integrated circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 1, pp. 123–133, Jan. 2005.

[26] A. M. Mangan, S. P. Voinigescu, M. T. Yang, and M. Tazlauanu, "De-embedding transmission line measurements for accurate modeling of IC designs," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 235–241, Feb. 2006.

[27] P. Chevalier, B. Barbalat, L. Rubaldo, B. Vandelle, D. Dutartre, P. Bouillon, T. Jagueneau, C. Richard, F. Saguin, A. Margain, and A. Chantre, "300 GHz fmax self-aligned SiGec HBT optimized towards CMOS compatiblity," in *Proc. 2005 Bipolar/BiCMOS Circuits Technol. Meeting*, Santa Barbara, CA, Oct. 2005, pp. 120–123.

Ekaterina Laskin (S'04) received the B.A.Sc. (Hons.) degree in computer engineering and the M.A.Sc. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2004 and 2006, respectively. She is currently working toward the Ph.D. degree in the Department of Electrical and Computer Engineering, University of Toronto.

Her research interests include the design of high-speed and millimeter-wave integrated circuits, with a focus on mm-wave imaging systems. In 2006, she was on a 6-month internship with the IBM T. J. Watson Research Center, Yorktown Heights, NY.

Ms. Laskin was a University of Toronto Scholar from 2000 to 2004. She received the National Science and Engineering Research Counsel of Canada (NSERC) undergraduate student research award in industry and university in 2002 and 2003. She was the recipient of the NSERC Postgraduate Scholarship and currently holds the NSERC Canada Graduate Scholarship. At the 2008 IEEE ISSCC, she received the Beatrice Winner award for editorial excellence.

Pascal Chevalier (M'06) received the engineering degree in science of materials from the University School of Engineers of Lille (Polytech'Lille), France, in 1994 and the Ph.D. degree in electronics from the University of Lille in 1998. His doctoral research, done at the Institute of Electronics, Microelectronics and Nanotechnologies, Villeneuve d'Ascq (France), dealt with the development of 100-nm AlInAs/GaInAs InP-based HEMT technologies for low-noise and power millimeter-wave amplification.

In 1999, he joined the Technology R&D department of Alcatel Microelectronics, Oudenaarde (Belgian Flanders) as Device and Integration Engineer on 0.35-μm Si BiCMOS technology. He was Project Leader for the development of 0.35-μm SiGe BiCMOS technologies, developed in cooperation with the Interuniversity MicroElectronics Center, Leuven, Belgium. In 2002, he joined the Analog & RF Process Technology Development Group of STMicroelectronics, Crolles, France, to develop high-speed self-aligned Si/SiGe:C HBTs for 130-nm millimeter-wave BiCMOS technology. He is currently in charge of the development of advanced devices for RF and millimeter-wave applications. He has authored or co-authored more than 80 technical papers and holds several patents.

Dr. Chevalier belongs to the wireless working group of the International Technology Roadmap for Semiconductors and is the process technology subcommittee chair for the IEEE Bipolar/BiCMOS Circuits and Technology Meeting.

Alain Chantre (M'91–SM'97) was born in Reims, France, in 1953. He received the engineering degree in physics from the Institut National des Sciences Appliquées de Lyon, France, in 1976, and the Ph.D. degree from the Université Scientifique et Médicale de Grenoble, France, in 1979. His doctoral research concerned deep-level optical spectroscopy (DLOS) in GaAs.

He joined the Centre National d'Etudes des Télécommunications (CNET), Grenoble, in 1979. He worked from 1979 to 1985 at the CNET Grenoble laboratory and during 1985–1986 at AT&T Bell Laboratories, Murray Hill, NJ, on deep level defects in silicon. From 1986 to 1992, he was in charge of a group working on the characterization of advanced silicon processes and devices. From 1993 to 1999, he has been working within the GRESSI consortium between France Telecom CNET and CEA-LETI, as head of a group involved in the development of advanced bipolar devices for submicron BiCMOS technologies. He joined STMicroelectronics, Crolles, in 2000, where he is currently managing the development of advanced SiGe bipolar devices and technology for RF and optical communications applications. He has published over 130 technical papers related to his research, and holds 20 patents.

Bernard Sautreuil received the Engineer degree in material physics from INSA Lyon, France, in 1979. He completed his thesis on Ge solar cells for multicolor systems in 1982.

In 1985, he joined Thomson Semiconductor (which became STMicroelectronics in 1987), in St. Egreve, France, where he acted successively as a process, maintenance, and device engineer. In 1991, he joined the STMicroelectronics Crolles metallization process group and then moved to Metal-Implant management, followed by the photo and etch group, including R&D. In 1999, he joined the R&D analog and RF technology group as Assistant Manager for BiCMOS Technology and Passive components development. Since 2004, he has worked as an interface for STMicroelectronics BiCMOS RF and mixed-signal customers.

Sorin P. Voinigescu (M'90–SM'02) received the M.Sc. degree in electronics from the Polytechnic Institute of Bucharest, Romania, in 1984, and the Ph.D. degree in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 1994.

From 1984 to 1991, he worked in R&D and academia in Bucharest, where he designed and lectured on microwave semiconductor devices and integrated circuits. Between 1994 and 2002, he was with Nortel Networks and Quake Technologies in Ottawa, Canada, where he was responsible for projects in high-frequency characterization and statistical scalable compact model development for Si, SiGe, and III-V devices. He later conducted research on wireless and optical fiber building blocks and transceivers in these technologies. In 2002 he joined the University of Toronto, where he is a full Professor. He has authored or co-authored over 100 refereed and invited technical papers spanning the simulation, modeling, design, and fabrication of high frequency semiconductor devices and circuits. His research and teaching interests focus on nanoscale semiconductor devices and their application in integrated circuits at frequencies beyond 200 GHz.

Dr. Voinigescu received NORTEL's President Award for Innovation in 1996 and is a member of the TPCs of the IEEE CSICS and BCTM. He is a co-recipient of the Best Paper Award at the 2001 IEEE CICC and at the 2005 IEEE CSICS, and of the Beatrice Winner Award at the 2008 IEEE ISSCC. His students have won Best Student Paper Awards at the 2004 IEEE VLSI Circuits Symposium, the 2006 SiRF Meeting, 2006 RFIC Symposium and 2006 BCTM.